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A Low-Cost and Low-Latency Inter-Stage Nonlinearity Error Calibration Algorithm for Pipelined ADCs

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ABSTRACT

Pipelined analogue-to-digital converters suffer from inter-stage gain errors and inter-stage nonlinearity errors due to gain variations and nonlinearity in residue amplifiers. While a polynomial-based calibration algorithm can address these errors, its conventional implementation demands excessive hardware resources and power consumption. This letter introduces a novel calibration algorithm that combines precomputation with a lookup table, achieving improved hardware efficiency while maintaining calibration accuracy and reducing latency.

1 | Introduction

Residue amplifiers (RAs) are the crucial components of pipelined analogue-to-digital converters (ADCs). The overall performance is mainly determined by the RA in the first stage, which also contributes to significant power consumption. Adopting an open-loop architecture [1–3] can reduce power consumption. However, open-loop RAs introduce gain variation and nonlinearity (dominated by HD2 and HD3). These imperfections cause inter-stage gain errors (IGE) and inter-stage nonlinearity errors (INE), thereby degrading the performance. Dither-based calibration has been widely used to correct IGE. The polynomial-based calibration [2] directly mitigates the INE through quadratic and cubic computations. The gated-LMS-based piecewise-linear (PWL) nonlinearity calibration [3] corrects IGE and INE simultaneously with reduced computation overhead. However, when calibrating HD2-induced errors, the convergence coefficients will be doubled, as the coefficients are different on the positive and negative sides, thereby significantly slowing convergence speed. Besides, the unavoidable multipliers in the critical digital paths increase the digital latency. To tackle these issues, this letter reduces the complexity of polynomial computation with a lookup table (LUT). In conjunction with a precomputation technique, the digital latency is also reduced.

2 | Correction of IGE and INE With Precomputation and LUT

To simplify the discussion, we analyse only the INE calibration of the first RA. The calibrated digital output $D_{\mathrm{RES\_cal}}$ is obtained through polynomial-based calibration, as expressed in the following equation.

$$D_{\mathrm{RES\_cal}} = \alpha_1 D_{\mathrm{RES}} + \alpha_2 D_{\mathrm{RES}}^2 + \alpha_3 D_{\mathrm{RES}}^3 \tag{1}$$

where D_{RES} represents the raw digital code of the residue stages, α_1–α_3 denote the correction coefficients of IGE, HD2- and HD3-induced errors, respectively. The problem with this method is the complexity of computing the quadratic and cubic terms of D_{RES}, which not only leads to power and area penalties but also increases latency in critical digital paths.

The conventional computation scheme of $\alpha_1 D_{\mathrm{RES}}$ for a five-stage pipelined ADC is shown in Figure 1a. Thanks to the pipelined scheme, the latency bottleneck lies between D_{raw5} and $\alpha_1 D_{\mathrm{RES}}$ in the last stage, comprising the weight adder, multipliers for the first-order coefficient, and the adder that combines the digital outputs from previous stages. The multipliers are the primary

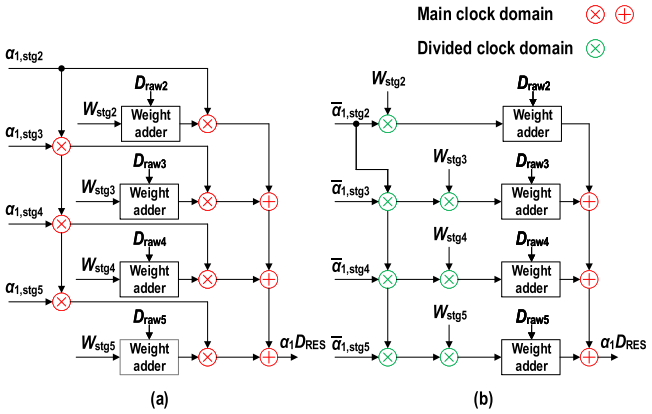

FIGURE 1 | Block diagrams of the weights computation of pipelined ADCs with (a) the conventional scheme and (b) the precomputation.

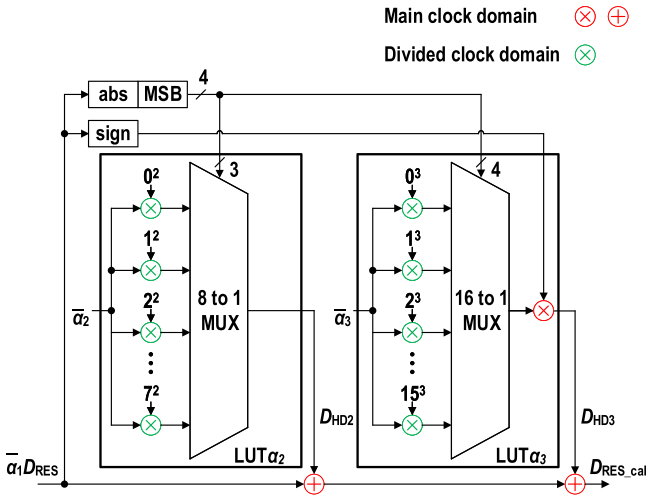

FIGURE 2 | Block diagram of the LUT-based and precomputation-based correction algorithm of INE.

source of latency. Moreover, they operate in the main clock domain, resulting in substantial power consumption. Thus, these components must be excluded from the critical path. Since all calibration coefficients will converge to stable values with negligible fluctuations, correction using previous coefficients is both accurate and fast. As shown in Figure 1b, $\bar{\alpha}_1$ is the mean value of the last N cycles and updates every N cycles. $\tilde{\alpha}_1$ of each stage can be precomputed with weights. The precomputations operate in the divided clock domain associated with the update cycles of $\bar{\alpha}_1$, reducing power consumption. With precomputation, the latency bottleneck consists of only adders.

When computing second- and third-order terms, their amplitudes remain confined within several LSBs. Consequently, the digital output is determined by the MSBs of D_{RES}. The LUT-based and precomputation-based correction algorithm is proposed. Figure 2 shows the block diagram of this algorithm. Equation (1) is revised as

$$D_{\mathrm{RES\_cal}} = \bar{\alpha}_1 D_{\mathrm{RES}} + \bar{\alpha}_2 LUT_{\alpha_2}(\tilde{\alpha}_1 D_{\mathrm{RES}}) + \bar{\alpha}_3 LUT_{\alpha_3}(\tilde{\alpha}_1 D_{\mathrm{RES}}) \quad (2)$$

By exploiting the symmetry of INE, the computation only requires the absolute values. Considering the calibration accuracy, the

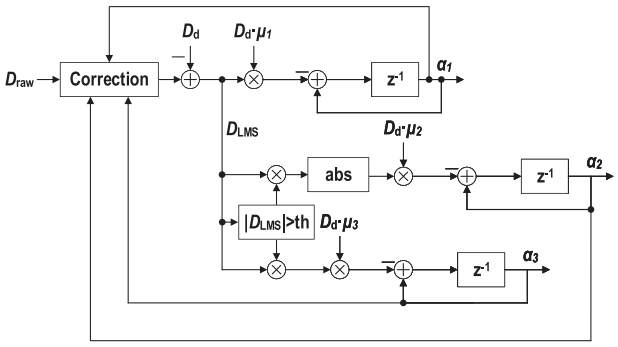

FIGURE 3 | Block diagram of the dither-based and gated-LMS-based calibration algorithm.

LUT_{α_2} and LUT_{α_3} require 3-MSBs and 4-MSBs inputs, respectively. Multipliers embedded in LUTs can also be precomputed with the mean value of α_2 and α_3 and operate in the divided clock domain. Furthermore, these multipliers are simplified to the shift-and-add operation, since one input of the multipliers are fixed integers. Consequently, both circuit overhead and latency are greatly reduced compared to the polynomial-based algorithm.

3 | Estimation of IGE and INE

The estimation of α_1–α_3 is achieved through a combined dither-based and gated-LMS-based calibration algorithm. The correction block in the estimation process is different from the critical correction path, employing updated coefficients for convergence without low-latency requirement. As illustrated in Figure 3, D_{LMS} is the error term for LMS convergence, including the errors due to $\alpha_{1\text{–}3}$. The conventional LMS algorithm [4] can be expressed as

$$\alpha[n+1] = \alpha[n] - \mu \cdot D_{\mathrm{d}}[n] \cdot D_{\mathrm{LMS}}[n] \quad (3)$$

where $\alpha[n]$ is the nth coefficient value, μ is the convergence step size and D_{d} is the sign of dither. Equation (3) proves effective for odd-symmetry errors. For even-symmetry errors, while (3) remains valid for positive D_{LMS} values, the convergence direction reverses for negative D_{LMS} values. The estimation for negative D_{LMS} values can be represented as

$$\alpha[n+1] = \alpha[n] + \mu \cdot D_{\mathrm{d}}[n] \cdot D_{\mathrm{LMS}}[n] \quad (4)$$

By combining (3) and (4), the estimation for even-symmetry errors can be processed by incorporating $|D_{\mathrm{LMS}}|$

$$\alpha[n+1] = \alpha[n] - \mu \cdot D_{\mathrm{d}}[n] \cdot |D_{\mathrm{LMS}}[n]| \quad (5)$$

(3) handles odd-symmetry errors from IGE and HD3 for α_1 and α_3 estimation. Equation (5) addresses even-symmetry errors from HD2 for α_2 estimation. Notably, α_2 and α_3 influence D_{LMS} only under large-amplitude D_{LMS} conditions. To ensure convergence accuracy, a gated-LMS-based calibration [2] selectively activates coefficient updates for α_2 and α_3 when $|D_{\mathrm{LMS}}|$ exceeds a threshold.

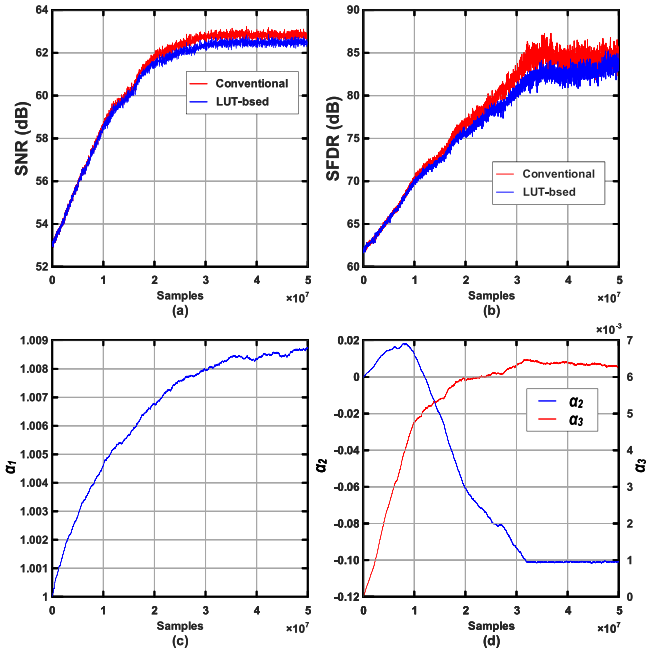

FIGURE 4 | The simulated (a) SNR and (b) SFDR versus samples and the convergence process of (c) α_1 and (d) α_2 and α_3.

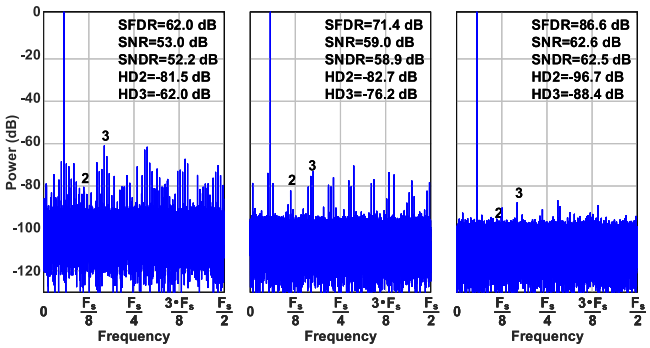

FIGURE 5 | Behavioural simulated spectra.

4 | Simulation Result

To verify the proposed algorithm, we implement behavioural-level modelling of a 12-bit pipelined ADC with a 3b-3b-3b-3b-4b stage configuration, which employs a dither weight of 128 LSBs. The HD2 and HD3 of the first RA are −50 dB. The threshold for the gated LMS is set to 256 LSBs. As shown in Figure 4a,b, the SNR and SFDR comparisons between the conventional and proposed algorithms demonstrate equivalent convergence SFDR and speeds with merely a 0.3 dB SNR degradation. Figure 4c,d presents the convergence process of α_1–α_3. Figure 5 shows the spectra before calibration, with only IGE calibration, and with IGE and INE calibration. After the IGE is corrected, the INE becomes the bottleneck for dynamic performance. Subsequently, with both calibrations enabled, the SNR is dominated by the inherent noise of the model. Figure 6 illustrates the relationship between convergence accuracy, HD2/HD3 and the required MSBs in the LUT. Improved analogue design can reduce digital circuit complexity. Figure 7 presents the conditions and results of a Monte Carlo (MC, 200 runs) behavioural simulation. The algorithm remains effective despite variations in the critical parameters of the ADC model. The relatively low SNR after calibration is limited by the low HD2 and HD3 conditions, as confirmed by the results in Figure 6.

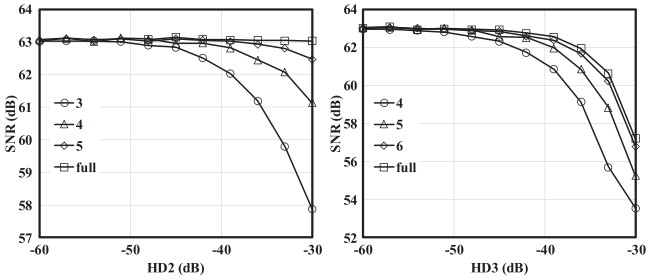

FIGURE 6 | Convergence SNR with HD2/3 and MSBs used in LUT.

Parameter	HD2/3	Inter-stage Gain	Offsets of RAs	Offsets of Comps
MC conditions	μ:-50 dB, σ:3 dB	μ:1, σ:1%	μ:0 mV, σ:2 mV	μ:0 mV, σ:2 mV

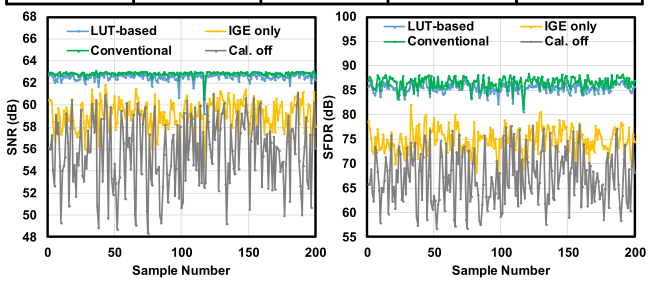

FIGURE 7 | The conditions and results of the MC behavioural simulation.

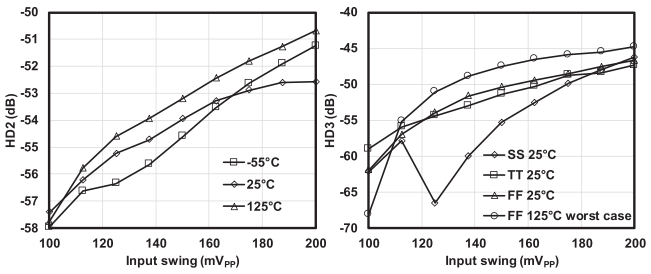

FIGURE 8 | The simulated HD2 (the worst value from 200 MC runs simulation with both process and mismatch on) and HD3 versus the input swing of RA.

The convergence analysis in this work requires 10^7 data points. Since circuit simulations cannot generate sufficient points directly, convergence is achieved by repeating the limited circuit simulation points to 10^7 points. However, behavioural modelling indicates that at least 2^{22} repetitive points are necessary to preserve convergence accuracy. Designed in a 28 nm CMOS process, the simulation is implemented with a simple pipeline-SAR architecture [3] and a more linear RA [5]. Operating at a 1.8 V supply, Figure 8 shows the linearity of RA. The input swing of the ADC is 1.2 V_{PP}, equivalent to a 150 mV_{PP} swing of RA. We ran an MC (20 runs) simulation to generate HD2. Each simulation provides 2^{17} repetitive points. The convergence performance is shown in Figure 9. Although the performance does not reach the level of the behavioural simulation due to limited repetitive points, the circuit simulation results still validate the proposed

TABLE 1 | Summary and comparison of the INE calibration algorithms.

	This work	JSSC 20 [2]	ISSCC 25 [3]
Techniques to calculate nonlinear terms	LUT	Polynomial computation	PWL
Input independent?	√	√	√
Complexity	Low	High	Low
No accuracy degradation?	×	√	×
Convergence speed[a]	3.5×10^7	3.5×10^7	7.2×10^7
Precomputation available?	√	√	×
Latency	Low (MSBs extraction, MUX, adders)	High (cubic computation, adders)	Medium (multiplier, adders)

[a]Estimate with the same initial state of Figure 4a and convergence step of first-order term.

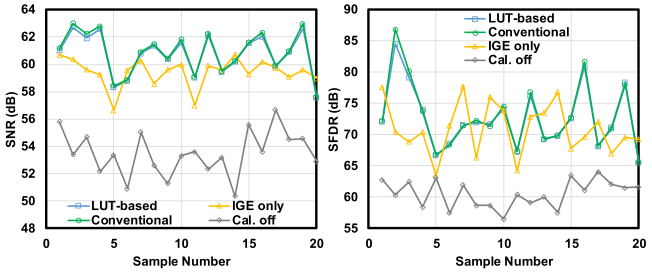

FIGURE 9 | The convergence performance of MC circuit simulation.

algorithm. Table 1 summarises and compares the INE calibration algorithms. By employing LUT and precomputation techniques, both complexity and latency are significantly reduced.

5 | Conclusion

This letter proposes a low-cost and low-latency INE calibration algorithm. Compared to the conventional methods, LUT-based correction algorithm simplifies the computation of HD2- and HD3-induced errors. Furthermore, precomputation eliminates the multipliers in the critical correction path, resulting in reduced digital latency.

Author Contributions

Qiang Yu: conceptualisation, data curation, formal analysis, investigation, methodology, validation, visualisation, writing – original draft, writing – review and editing. **Qiang Li:** formal analysis, funding acquisition, methodology, project administration, writing – review and editing.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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