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# High speed digital interfacing for a neural data acquisition system

## Enabling of live display functionality for a neural recording system

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**Abstract:** Diseases like schizophrenia and genetic epilepsy are supposed to be caused by disorders in the early development of the brain. For the further investigation of these relationships a custom designed application specific integrated circuit (ASIC) was developed that is optimized for the recording from neonatal mice [Bahr A, Abu-Saleh L, Schroeder D, Krautschneider W. 16 Channel Neural Recording Integrated Circuit with SPI Interface and Error Correction Coding. Proc. 9th BIOSTEC 2016. Biodevices: Rome, Italy, 2016; 1: 263; Bahr A, Abu-Saleh L, Schroeder D, Krautschneider W. Development of a neural recording mixed signal integrated circuit for biomedical signal acquisition. Biomed Eng Biomed Tech Abstracts 2015; 60(S1): 298–299; Bahr A, Abu-Saleh L, Schroeder D, Krautschneider WH. 16 Channel Neural Recording Mixed Signal ASIC. CDNLive EMEA 2015 Conference Proceedings, 2015.]. To enable the live display of the neural signals a multichannel neural data acquisition system with live display functionality is presented. It implements a high speed data transmission from the ASIC to a computer with a live display functionality. The system has been successfully implemented and was used in a neural recording of a head-fixed mouse.

**Keywords:** high speed digital interfacing; live display of neural data; neural data acquisition system; neural recording system.

## 1 Introduction

Disorders in the early development of the brain could lead to diseases like certain forms of schizophrenia and genetic epilepsy [1, 2]. This hypothesis of neural development from Ben-Ari et al. and Lewis et al. [1, 2] is investigated with the help of genetic mouse disease models. Recent findings of Marguet et al. [3] showed that by treatment at a critical stage of the brain development the rescue from a genetic epilepsy could be possible. To further investigate these relationships, the signals from neonatal mice have to be analysed. A custom designed application specific integrated circuit (ASIC) was developed that is optimized for recordings in neonatal mice [4–6].

For the recording of the neural signals from the head of the mouse a Neuronexus multichannel electrode [7] is placed in the cortex of the mouse. The correct placement of the electrodes is essential to enable the neural recording. Saving the data to a memory and analysing it after the recording is not feasible during experiments with living animals. The adjustment of the electrode would take much too long and the animal would be stressed longer than necessary.

To enable the live display of the neural signals, a neural recording data acquisition system is presented. It implements a high speed data transmission from the ASIC to a computer with a live display functionality of the neural data. High-speed data acquisition systems based on FPGA have been presented in [8, 9]. To adopt to the specific needs of the custom designed ASIC, a custom designed digital interfacing had to be developed.

## 2 Material and methods

The neural recording system is designed in such a way that it adopts to the custom designed integrated circuit and that it fits into the environment of the neuroscience. Existing

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interfaces like Neuroscope [10] are integrated to enable an easy handling of the interfaces for the experimenters. The selection of the field programmable gate array (FPGA) is based on the system requirements and influenced by the wide spread existence of the opal Kelly Interface board [11], that is used by the open source community open ephys [12] or the company Intan [13].

## 2.1 Specification and system requirements

The acquisition system interfaces to a custom designed integrated circuit [4, 14]. The circuit with the size of only $1.5 \times 1.5\ mm^2$ comprises of 16 analog inputs that are sampled with 20 kS/s/channel at an ADC resolution of 10 bit. The recording using a single integrated circuit results in a data rate of 3.52 Mb/s [4].

The ASIC implements a four wire serial peripheral interface (SPI) with an additional signal from the analogue to digital conversion (ADC). This additional end of conversion (EoC) signal is used as an interrupt to signal that a new sampled value is available. To handle this interrupt, a custom SPI master interface is implemented on the FPGA that requests the data from the ASIC each time the interrupt is triggered.

## 2.2 Neural data acquisition system

A block diagram of the designed neural data acquisition system is shown in Figure 1. The ASIC communicates with the acquisition board through a SPI interface. For the communication between the acquisition board and the computer a USB connection was chosen [14]. The purpose of the ASIC is the recording of the neural data and the acquisition board transmits the data to the computer. The data is shown immediately on screen in a live mode.

### 2.2.1 Control programm and live display

For the controlling of the neural recording system a control program was developed that is running on the computer. This program writes the data into a binary .dat file. For the live display of the data the tool Neurosccope is used [10]. Neuroscope is a widely used interface in the neuroscientific community. A diagram of the data flow on the computer is shown in Figure 2.


**Figure 1:** Block diagram of the neural data acqusisition system [14].

### 2.2.2 Data acquisition board

The data acquisition board consists of an FPGA Interface board (XEM 6010) from the company Opal Kelly [11], a power supply unit for the integrated circuit and connectors for interfacing. A block diagram of the data acquisition board is shown in Figure 3. The Interface Board consist of a Xilinx Spartan 6 FPGA, an SDRAM for buffering, a Phase Locked Loop (PLL) for clock generation and a USB Micro Interface block. The board communicates through a High-speed USB 2.0 Interface with the computer (data rate up to 38 Mb/s). The FPGA works at 100 MHz and has sufficient speed to handle the required data rate. The board includes an extra memory of 128 Mb SDRAM.

The Opal Kelly board integrates a communication library that is provided from the manufacturer. The library takes care of the communication between the FPGA on the board and a program on the computer by providing endpoints. By integration of the library into the C++ code and the verilog code, data can be transmitted between the computer and the FPGA by handing over the data to endpoints.

### 2.2.3 The control program

The data acquisition system and the SPI master are controlled by the control program, the program is written


**Figure 2:** Data flow diagram on the computer: the control program writes the data into a binary file. The data is then simultaneously read from the binary file with the program Neuroscope and displayed in a live mode.

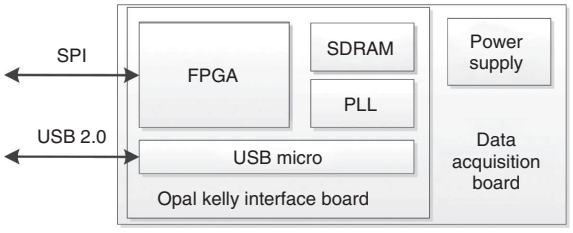


**Figure 3:** Block diagram of the data acquisition board.

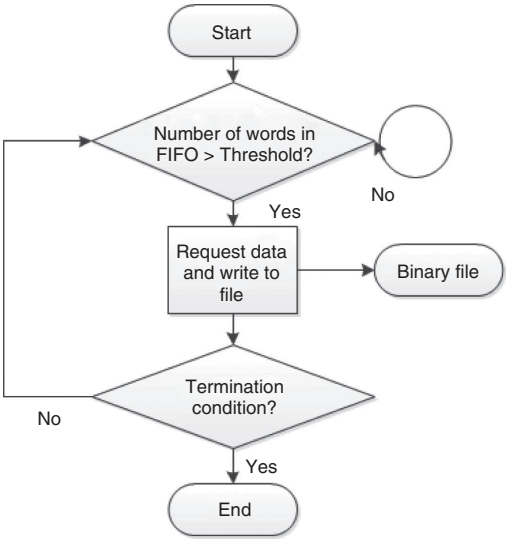


**Figure 4:** Flow chart of the data acquisition phase of the control program.

in C++. The program splits into two parts: A system configuration phase where the communication system parameters are initialized and the recording parameters are set and a data acquisition phase, where the data is requested from the board and written into a file on the PC-memory (hard drive).

In the first step of the configuration phase the recoding parameters of the control program are specified. Then a connection to the FPGA is established and the FPGA is programmed by loading the bit file. The SPI and ADC clocks are configured and started. Finally the integrated circuit is configured to the mode of operation.

In the data acquisition phase the data transfer from the FPGA to the PC is controlled by the counter "*AvailalbeWordsInFIFO*". This counter holds the number of words that are stored in the buffer on the data acquisition board. The control program continuously checks the size of this counter. If the value exceeds a threshold the specified number of words is picked up from the FIFO and written into the *.dat* file. This process continues until the specified number of words is recorded.

For the implementation functions and libraries from OkLibrary.lib from Opal Kelly and from IntanTech rhd2000evalboar.lib are used [11, 13].

### 2.2.4 FPGA implementation with SPI master

The FPGA implements the SPI master, a buffer, a variable frequency clock generator and the communication endpoints. The task of the SPI master is to write the configuration file to the SPI slave on the integrated circuit

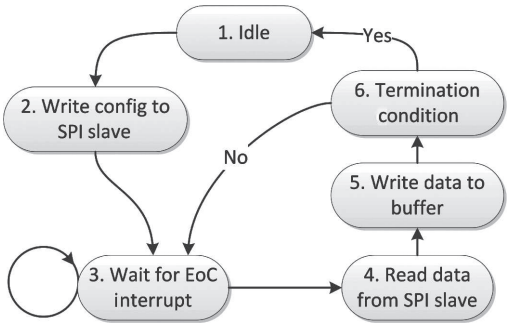


**Figure 5:** State machine of the SPI master.

and to read the neural data from the SPI slave and write it into a buffer on the FPGA.

The SPI master is implemented as a final state machine. The state machine is depicted in Figure 5.

The ASIC is designed in a way that it can work with a wide range of clock frequencies. The clock is provided externally to the ADC. The lowest available clock from the PLL is approximately 2 MHz. To generate clock signals in the kilo Hertz range, a configurable frequency clock generator was implemented. It divides the clock from the PLL down by powers of two in the range of $2^0$ to $2^8$.

For communication the OkLibrary was integrated, this library provides communication endpoints [11].

The data is written by the SPI master into a buffer. The buffer is implemented as a 128 Mb SDRAM FIFO.

The ASIC sends data packages of 22 bits to the SPI master, this contains the data of two channels per SPI-block. To transmit the data to the PC two packages are put together into a container of 64 bis, to fit into multiples of 8. The packages are saved into a buffer on the interface board. As soon as 2048 packages of 64 data bits are available, this data set is transmitted to the C++ program on the PC.

## 3 Results

The presented system is successfully implemented and used in a neural recording of an adult mouse. An acute silicon probe (50 $\mu$m inter-site spacing) [7] was used in a recording in the hippocampus of a urethane-anaesthetized adult head fixed mouse. The neural signals from the cortex of the mouse were recorded with the data acquisition system and the data was displayed in the live view modus during the recording. The system worked at a data rate of 3.5 Mb/s. The control program writes to the .dat file and the Neuroscope program reads from the same file at the same time. Figure 6 shows an example low field potential (LFP) of a sharp wave-ripple event (SPW-R) recorded with the system.

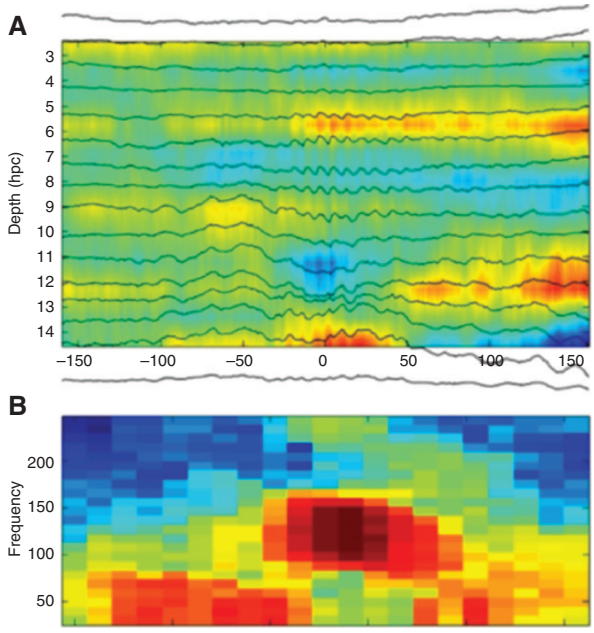


**Figure 6:** Acquisition of LFPs from head fixed mice: (A) Example LFP traces and pseudocolor CSD from an acute silicon probe depth-profile recording in the hippocampus of a urethane-anaesthetized adult mouse during a sharp wave-ripple event (SPW-R). (B) Corresponding spectrogram of the pyramidal layer channel shows the expected ripple event frequency of 100–150 Hz.

# 4 Conclusion

A custom designed high speed digital interfacing for a neural data acquisition system has been successfully developed. The system implements a custom SPI interface and interfaces to a a custom designed integrated circuit. It enables a live view functionality of neural data. The functionality has been shown in *in-vivo* experiments. The measured rate is approximately 30% higher compared to [9].

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### Author's Statement

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