ESPRIT 2434 30 Months Report June 1991

Contribution to:

Activity Task 2.5

-- System Concept for Advanced CIM/AI Controller --

Title:

TEMPORAL INFERENCE ACCELERATOR BOARD

PROGRESS REPORT

Author/Company/Copyright:

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Achievements:

The functional schematic of the qualitative temporal logic hardware accelerator board has been refined to allow for register transfer level simulation of the accelerator, prior to its final implementation. A coprocessor for quantitative temporal reasoning was conceived, and its design has been nearly completed. Goals for the second half year 1991 are outlined.

Summary:

A refined functional schematic of the qualitative temporal logic hardware accelerator board is presented, together with a schedule for the availability of its constituting electrical components. Two coprocessor designs for quantititative temporal reasoning are reported.

INTRODUCTION

One of the tools Artificial Intelligence provides for the solution of planning and sequencing tasks is time logic. At Philips Hamburg, we chose to survey the possibility of speeding up Allen's qualitative temporal logic, together with quantitative enhancements by Rit. Algorithmically, Allen's interval-based, qualitative time logic is NP-complete. Even approximative solution procedures to this kind of temporal logic consume large amounts of computation times on conventional computers (e. g., workstations). The algorithmics of the temporal logic chosen were described in [Jakob 1990].

To make temporal logics useful for practice, Philips Forschungslaboratorium Hamburg is conceiving and designing a hardware accelerator for Allen's temporal logic. This work is done in cooperation with the "Arbeitsbereich für Prozeßautomatisierungstechnik" (Department for Process Automation) of the Technical University of Hamburg-Harburg. The accelerator is to be integrated onto a PC/AT-style hardware extension card. The PC is used to provide a comfortable, Windows 3.0 based graphical user interface. Hardware accelerator card and user interface software are to be packaged into a PC product for planning and scheduling. The PC is used as an IO and communication processor by the accelerator board. All computation-intensive steps are to be performed on the accelerator board.

REFINED SCHEMATIC OF ACCELERATOR BOARD

Currently, the following components form part of the accelerator board (Table 1 and Figure 1):

- Host Bus Interface: interface of the accelerator card to the host hardware bus;
- Edge Memory: memory representating the edges of the qualitative temporal net;
- Edge-to-Triangle Memory: memory mapping each edge onto its associated triangle(s);
- Triangle Memory: memory representing the "triangles" (path constraints) of the qualitative temporal net;
- Edge Registers (alpha-Edge, beta-Edge, gamma-Edge): intermediate storage for the respective edges of the normalized triangle (called alpha, beta, gamma);
- Triangle Congruenter: maps the normalized ("static") triangle onto the actual ("dynamic") triangle as required by the path constraint;
- Temporal Inference Unit (TIU): qualitative temporal reasoning; elementary temporal inference; path[1] consistency in net representation;
- gamma-Edge Comparator: compares the old and new gamma edge values of the current triangle;
- Solution Buffer: FIFO storage for "solutions" (consistent labellings) of the current temporal net;
- Qualitative Temporal Reasoning Control Unit: control logic for all other modules of the board.

[1] A concise introduction to the area of constraint satisfaction is given in [Swain, Cooper 1988]. Especially, the terms path, node and arc consistency are defined. -- This paper is also a good introduction to the idea of using hardware for the speedup of constraint satisfaction tasks. However, the paper is rather general in its approach.

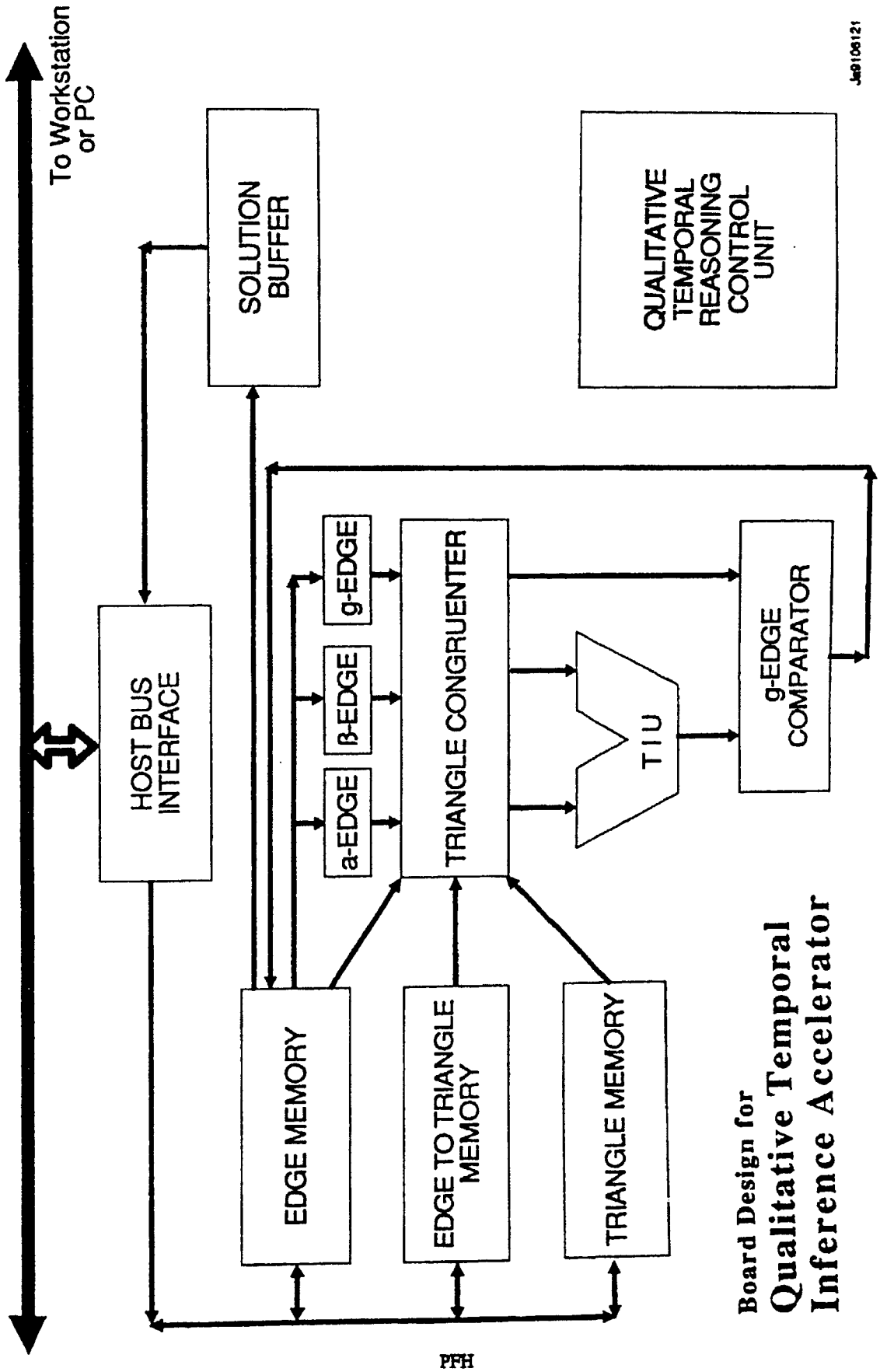
- Interval Constraint Propagator # 1: quantitative temporal reasoning, node consistency of temporal net;
- Interval Constraint Propagator # 2: quantitative temporal reasoning, arc consistency of temporal net.

Table 1: Temporal Logic Accelerator Board Component List

A functional schematic of the accelerator board is to be found in Figure 1. It is a refined version of the schematic introduced at the FSPRIT 2434 2nd Review Meeting at Brussels in August 1990 and documented in [Jakob 1991], p. 332.

Note: Figure 1 is a complete schematic of the *qualitative* temporal logic hardware acceleration board envisaged. Furthermore, there will be two coprocessors added for performing quantitative temporal reasoning as well (called Interval Constraint Propagator # 1 and # 2 in Table 1). However, the overall system structure for quantitative reasoning is not fully settled by now. In the simple-most case, both coprocessors will not be connected to the qualitative temporal logic hardware, although they reside physically on the same PC extension board. Instead they would be used as coprocessors by the software which resides on the PC host. (A discussion of coprocessor concepts is to be found in [Jakob 1991]).

Figure 1: Functional Schematic of Qualitative Temporal Logic Hardware Accelerator Board



AVAILABILITY OF COMPONENTS

Availability of components of the accelerator board (Table 2):

- Temporal Inference Unit ("TIU"): available since fourth quarter, 1990. 1,200 gate equivalents gate array;
- Interval Constraint Propagator #1: design and layout of prototype finished 90 % by June 1991. 8,000 gate equivalents gate array;
- Interval Constraint Propagator # 2: feasibility study performed. Estimate: > 10,000 and < 30,000 gate equivalents gate array;
- Edge Memory, Edge To Triangle Memory, Triangle Memory: feasibility study performed. DRAM (dynamic random access memory) or SRAM (static random access memory) implementation;
- Triangle Congruenter: logic schematic available;
- gamma-Edge Comparator: logic schematic available;
- Solution Buffer: feasibility study performed.
- Control Logic ("L-reasoning Control Unit"): feasibility study performed.
- Host Bus Interface (PC ISA/EISA bus interface): available since third quarter, 1990.

Table 2: Temporal Logic Accelerator Board Availability List

Some of the components are to be implemented as custom-specific integrated circuits. A prototype of the TIU (Temporal Inference Unit) and of the Host Bus Interface were already described in the 24 Months Report of ESPRIT 2434 [Jakob 1991]. Possible extension to the basic hardware algorithm described in this paper are to be found in [Becker 1991].

OUTLOOK

During the second half year 1991, (1) the Interval Constraint Propagator # 1 will be implemented and tested, (2) a register transfer level simulation (cf. [Mead, Conway 1980]) of the qualitative accelerator board of Figure 1 will be performed. Afterwards, the actual hardware implementation will start.

REFERENCES

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