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Simultaneous large-scale reliability analysis of ultra-thin MOS gate dielectrics using an automated test system

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Abstract. This article presents an automated test system targeting the large-scale analysis of ultra-thin MOS gate dielectric degradation. The system allows for stress tests at elevated temperatures as well as supply voltages and long-term tests of thousands of MOS devices simultaneously. The aim is to build-up large and hence significant statistics about the degradation process as a function of time.

1 Introduction

The reliability of ultra-thin MOS gate dielectrics is limited by time-dependent degradation processes inter alia. Gate dielectric thicknesses of MOS devices currently in fabrication range from 1.7 nm for a 130 nm technology down to 1.2 nm for a 65 nm technology or even below for further advanced technologies and correspond to only a few atom layers. Considerable tunnelling currents flow through these ultra-thin dielectrics and cause local rearrangements of the atomic structure. These so-called “weak spots” Lombardo (2005) attract ever more current flow leading to further restructuring on atomic level (“soft breakdown”). At the end, a crystalline Si conducting path through the gate dielectric shortens channel and gate (“hard breakdown”) as illustrated in Fig. 1.

Atomistic computer simulations are expected to expose physical mechanisms originating gate dielectric degradation and to give information on time-dependent breakdown probabilities. A device simulator considering degradation effects and reproducing ageing of electronic circuits is the long-term objective of this project.

Broad and significant databases of appropriate experiments are essential to verify and calibrate the simulations mentioned above. A large-scale automated test system has been developed for this purpose. It offers the possibility to simultaneously analyse thousands of MOS devices under stress conditions (elevated temperatures and supply voltages) as well as under long-term operating conditions.

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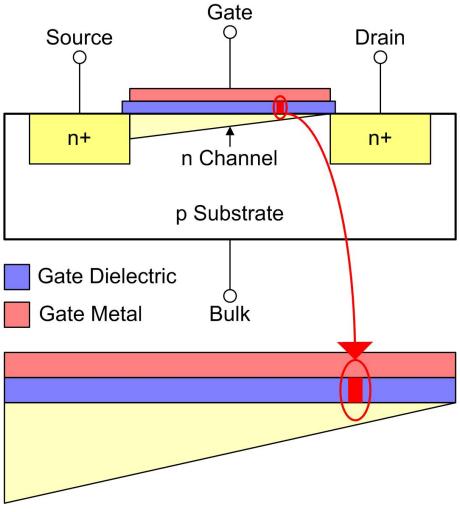

Fig. 1. Hard gate dielectric breakdown.

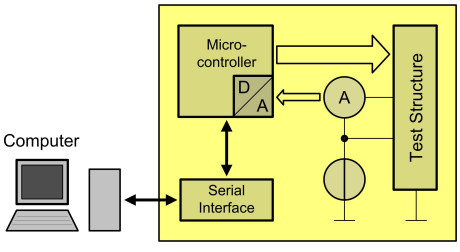

Fig. 2. Automated test system.

2 Automated test system

The automated test system is shown in Fig. 2. It consists of an integrated test structure, a current sense circuit, a voltage source, a microcontroller with A/D-converter, and a serial interface. During testing, the automated test system operates stand-alone. A computer is only required to set up tests at the beginning and to evaluate the results at the end.

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3 Integrated test structure

Figure 3 depicts the block diagram of the integrated test structure. In the case shown, the MOS device under test (DUT) cells are arranged in a 32x32 matrix. Every single DUT cell can be accessed via column/row decoders and a clock signal CLK. The column/row decoders are driven by two external 5 bit busses X, Y.

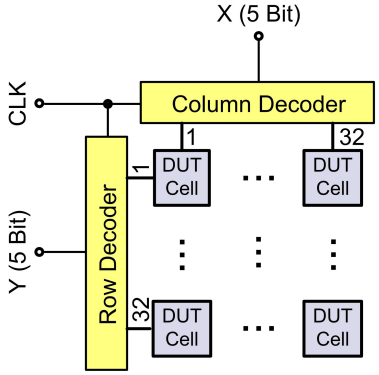

Fig. 3. Integrated test structure overview.

Details of the DUT cells are shown in Figure 4. Each of the 32x32 cells consists of the MOS DUT itself, a switch, and a logic with a memory. The memory stores the state of the switch that either connects the DUT gate to a supply line common to all cells in a row or disconnects it from that line. Its memory contents can be written via a data line when the decoders set the appropriate row and column lines. The logic then connects the data line to the memory to set the state of the switch. Every single cell of the matrix can be addressed, measured, and switched-off in case of breakdown separately in this manner.

A switch at the beginning of every row connects that row either to CSTRESS ("common stress") or to SSTRESS ("single stress"). CSTRESS is the stress voltage line. All rows are normally connected to that line during testing. Temporarily, one single row can be switched to SSTRESS in order to measure the current of that single row with the external current sense circuit. All other rows are not affected by that operation. A single gate current is measurable when all other DUTs of a row are shut off.

To ensure all DUTs are stressed under the same conditions, each source is connected to CSOURCE ("common source") and each drain is attached to CDRAIN ("common drain") respectively. With CSOURCE and CDRAIN at the same potential, it is possible to stress the DUTs as MOS capacitors. Real operating conditions can be obtained with CSOURCE and CDRAIN at different potentials.

The integration of both the DUTs and the periphery (logic, decoders) on one chip means that all devices are stressed with the same conditions and degrade similarly. This problem is solved by the usage of MOS transistors with different gate dielectric thicknesses for DUTs (thin dielectrics) and logic as well as decoders (thick dielectrics). Figure 5 shows the layout of the integrated test structure with 32x32 devices. The 130 nm technology chosen features 1.7 nm and 6.0 nm gate dielectrics.

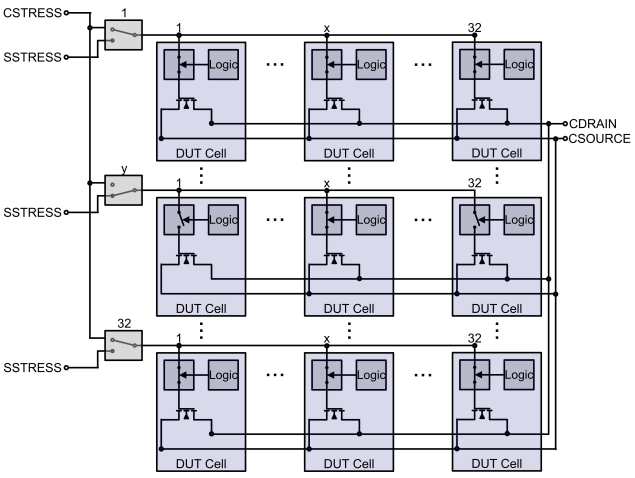

Fig. 4. Integrated test structure details.

Fig. 5. Integrated test structure layout.

4 Current sense circuit

Gate dielectric degradation causes increasing gate currents. The lowest currents to be measured occur at the beginning of the DUT lifetime. These are due to direct tunnelling. In the course of time, the gate currents increase which is accompanied by noise. At a certain point, the noise affects the functionality of the DUT. This is called soft breakdown [Lombardo (2005)]. At the end of lifetime, the gate dielectric finally breaks down which means gate electrode and channel are shorted. This is the so-called hard breakdown. The currents to be measured are comparatively high in this case. The

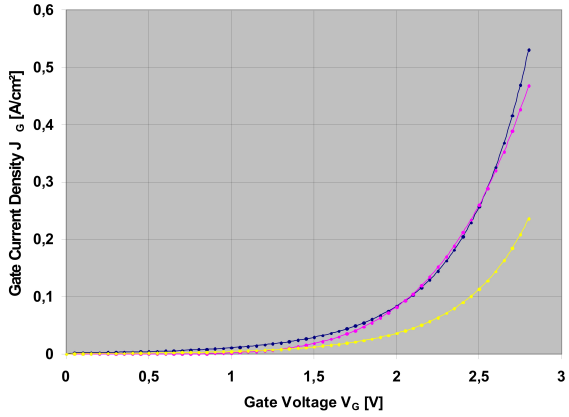

Fig. 6. Direct tunnelling current densities.

gate current variation at the beginning and at the end of lifetime covers several orders of magnitude.

Direct tunnelling currents through the gates of fresh DUTs have been estimated with the aid of literature Depas (1995) and computer simulations. Figure 6 shows the results (yellow curve: rough estimation with literature values, blue curve: simulation results, magenta curve: calculated values). It can be seen that the expected direct tunnelling current density ranges from 0.04 $\frac{A}{cm^2}$ to 0.08 $\frac{A}{cm^2}$ at 1.8 V gate voltage. This means direct tunnelling currents from 300 pA to 1 nA at 1.8 V stress voltage and with the geometries chosen for the DUTs.

Research workers have investigated the gate currents of MOS devices after hard breakdown. E.g. Lombardo (2005); Avellan (2004) report an increase of the gate current density of several orders of magnitude. Breakdown gate currents up to the mA region have been measured. Both literary sources consider MOS devices with geometries comparable to those of the integrated test structure.

The current sense circuit in Fig. 2 must cover the measuring range from pA to mA. An appropriate measurement instrument for this purpose is the feedback current sense circuit as shown in Fig. 7 schematically. The circuit is based on a low leakage, high input resistance, high gain operational amplifier. The feedback element defines the measurement range. In case a resistor is used, the pA region can be measured linearly. If a diode or a bipolar transistor is applied, the feedback current sense circuit covers the range from pA to mA logarithmically.

5 Microcontroller

The microcontroller scans the test structure for broken down DUTs. It selects one row after the other, connects the current sense circuit to that row, switches off all DUTs in that row except for one, and measures the gate current of the one single DUT. In case the gate current is unacceptably high, a hard breakdown has occured and the broken device is shut

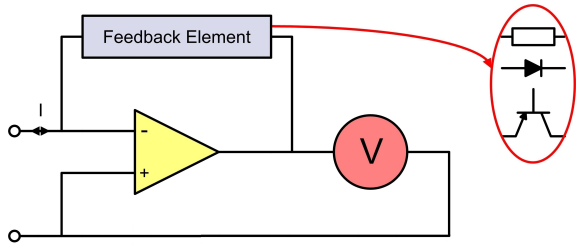

Fig. 7. Feedback current sense circuit.

off. These steps are repeated for every single DUT. The microcontroller automatically ends the test if no working DUT is left. Note that the operations in one row do not affect the other rows.

The microcontroller stores characteristic data of the gate dielectric degradation for every single DUT in its internal memory. In case of long-term tests, the microcontroller is able to capture the gate current of all DUTs every second for up to four years. If short-term stress tests are performed, an accordingly increased resolution in time is possible.

Generally, the microcontroller can be set up for test through any terminal program. A graphical user interface (GUI) under MATLAB eases the setup and the data transmission to as well as evaluation on a computer.

6 Conclusions

This paper presents an automated test system for MOS gate dielectric analysis based on a 1024 DUT integrated test structure. A version with 4096 DUTs is also available.

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