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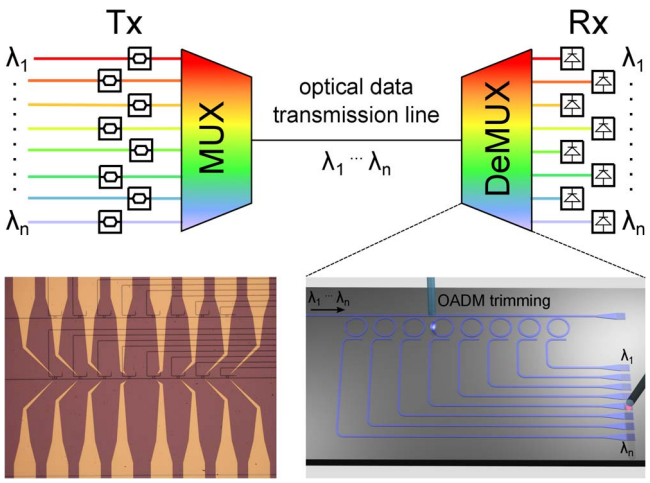

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Energy-Efficient Wavelength Multiplexers Based on Hydrogenated Amorphous Silicon Resonators

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Abstract: Optical multiplexers are key components of modern data transmission systems that have evolved from long-haul fiber communication applications down to the photonic interconnect level on-chip, which demand high bandwidths and low-power photonic links with small footprint. We present compact, energy-efficient, and high-bandwidth optical add/drop multiplexers that are based on complementary metal–oxide–semiconductor (CMOS) backend-compatible hydrogenated amorphous silicon microring resonators. We study the manufacturing nonuniformity of the as-fabricated devices and analyze the static power consumption that is required to actively align the multiplexers to a 100-GHz grid by using state-of-the-art microheaters. The microring filter banks are in excellent agreement with the design and satisfy a good tradeoff between concurrent properties of high-data-rate capability, low filter loss, high channel isolation, and manufacturing uniformity, which facilitates the operation with low static power consumption. In addition, we demonstrate that it is possible to permanently correct the unavoidable fabrication imperfections and to arrange the individual wavelength channels by a postfabrication trimming method so that the static power is reduced by more than an order of magnitude and allows minimization of these parts of the overall power requirements of such photonic integrated circuits down to record low metrics of a few femtojoules per bit.

Index Terms: Amorphous silicon, a-Si:H, integrated optics, photonic interconnects, dielectric photonic wire waveguides, microring, wavelength multiplexer, add drop filter, thermo-optic tuning, trimming.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) is a promising material for the realization of photonic electronic integrated circuits (PEICs). In addition to the low a-Si:H absorption in the established fiber-optic-communication transparency windows at 1.3 μm and 1.55 μm [1], [2], the attraction of the material arises from the same fundamental reasons as for crystalline silicon-on-insulator (SOI). The most important economic and physical characteristics are the compatibility with mature complementary metal-oxide semiconductor (CMOS) industry providing access to highly-developed process technology and infrastructure [3], and the high refractive index contrast (HIC) of $\Delta n \geq 2$ enabling dense PICs that come closest to the footprint of microelectronics; with minimal inter-layer distances and closest possible proximity to metals. Since a-Si:H is deposited at $T \leq 300\,^{\circ}\mathrm{C}$, a 3-D-integration on top of readily fabricated microchips at the back-end becomes

possible [4], [5], which relaxes the size discrepancy and the area competition of electronics and photonics at the most-expensive front-end layers and reduces latencies by minimal vertical distances. This approach includes options to link SOI photonics by optical vias, e.g., with pin-modulators and detectors, and provides possibilities in terms of packaging and off-chip coupling favorably placed at the better accessible top of the chip. Further integration potential is offered by heterogeneous materials, e.g., III-V [6], inorganic dielectric (SiN, TiO_2, Al_2O_3) [7]–[9], ferroelectric ($LiNbO_3$, $BaTiO_3$) [10]–[12], and plasmonic and/or organic hybrid materials [13]–[15], providing additional functionality and a high degree of flexibility for customized PEICs. Because of these integration capacities, there is an increasing interest in amorphous-SOI (a-SOI) research.

The material has been utilized to realize low-loss waveguides [16]–[20], and functional integrated-optic devices like interferometers and microring resonators (MRRs) with key metrics comparable to SOI [16]–[18]. The flexible deposition process enables the fabrication of three dimensional tapered fiber-to-chip couplers [21], [22], vertical arranged MRRs [23], and optical vias which allow interfacing vertically stacked photonic circuits [24]–[26]. Beside these passive devices, a-Si:H is subject of interest for nonlinear and active photonic functions, both, in the all-optical [27]–[34], and electro-optical domain [35]–[37]. However, although the tight mode confinement and the strong thermo-optic-effect (TOE) are in particular useful to realize compact, energy-efficient, and high-bandwidth data transmission systems employing wavelength division multiplexing (WDM) techniques, circuit components like e.g., multichannel optical add/drop multiplexers (OADMs) have not been investigated. Furthermore, the manufacturing non-uniformity (NU) which is directly related to the power consumption and the thermal load of the PEICs, and post-fabrication compensation techniques of such devices have not been explored yet.

In this paper, we present 8-channel OADMs that are based on low footprint MRRs. The devices are modeled to satisfy a good trade-off between concurrent properties of high data rate (DR), low filter drop loss, and low channel crosstalk (XT). We systematically analyze the device NU from fabrication and determine the static power consumption that is required to actively fine-tune the multiplexers to a fixed 100 GHz frequency grid in accordance to the International Telecommunication Union (ITU) specifications by using integrated microheaters. In addition we demonstrate the permanent correction of the OADM manufacturing imperfections by a post-fabrication trimming method so that the contribution due to the static power consumption can be reduced to record-low energy/bit values of a few fJ/bit, thereby mitigating the temperature overhead by active tuning.

2. Optical Add/Drop Multiplexer Design and Fabrication

2.1. Optical Add/Drop Multiplexer Design

In principle, the ideal OADM should be capable to process as many high-speed parallel data signals as possible while providing small device insertion and drop port losses with high channel isolation and low XT. However, for MRR devices these design objectives are in conflict, e.g., a low XT implies a weak coupling coefficient which results in a high Q-factor limiting the DR. Therefore, a good compromise needs to be found between these competing factors including the evaluation of fabrication constraints, e.g., the coupling gap size or the spectral device NU, so that the manufactured devices function within the desired target specifications. The design objective was to fabricate 8-channel OADMs on a 100 GHz frequency grid with a channel XT $\geq$ 15 dB, single channel data rates $\geq$ 20 Gb/s, and $\leq$ 1 dB drop losses.

The MRRs were modeled with coupled mode theory employing a FEM solver in order to define the resonator key properties and were designed with a SiO_2 bottom and a SU-8 top cladding taking material dispersion into account [38]. The calculations were carried out for single-mode 480×200 nm^2 photonic wires (TE-mode) with a guided mode index of $n_{\text{eff}} = 2.359$ at 1.55 μm and include a straight waveguide propagation loss of 3 dB/cm. The transmission capability of the OADMs was analytically derived from (1) which describes the transient dynamics of the MRR filter e.g., upon square wave input signals [39]. The model assumes the case of resonance

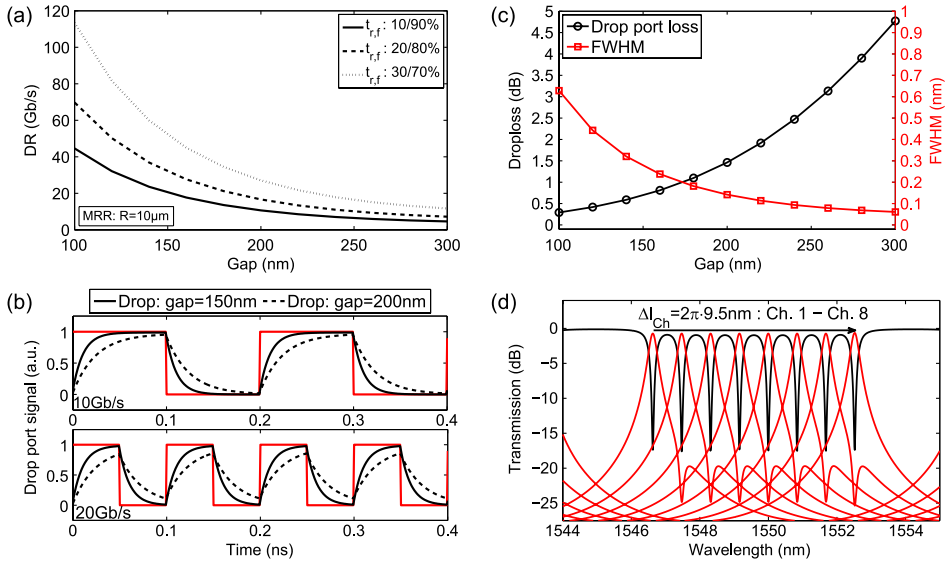

Fig. 1. Optical add/drop multiplexer design based on 10-μm ring resonators at 1.55-μm wavelength. (a) Data rate calculations for different bus-to-ring gaps. (b) Transient MRR response for 10 and 20 Gb/s data rates with 150 and 200 nm coupling gaps. (c) Drop port loss and corresponding FWHM for different coupling gaps. (d) Transmission and drop port spectra of the optimized 8-channel OADM.

condition so the waves of each round-trip are phase-matched. The add/drop MRR coupling sections are considered to be loss-less with $|\tau_{1,2}^2| + |\kappa_{1,2}^2| = 1$ using symmetric couplers $\kappa = \kappa_1 = \kappa_2$, with $\tau_{1,2}$ as through- and $\kappa_{1,2}$ as cross-coupling coefficients. For a realistic modeling, the sum of the coupling, bend, and mode conversion losses due to the straight and curved photonic wire sections were included in the loss coefficient α with 0.025 dB:

$$E_{\mathrm{MRR}}(n\Delta t) = \kappa \cdot \sum_{i=0}^{n} \left[\tau_1 \cdot \tau_2 \cdot \exp\left(\frac{-\alpha L_{\mathrm{res}}}{2}\right)\right]^i \cdot E_{\mathrm{bus}}((n-i)\Delta t). \tag{1}$$

The electric fields of the bus $E_{\mathrm{bus}}(n\Delta t)$ and the MRR waveguide $E_{\mathrm{MRR}}(n\Delta t)$ were evaluated for fixed time-steps $n\Delta t$, with $n \in \mathbb{N}_0$ as the number of round-trips, and $\Delta t = L_{\mathrm{res}} \cdot n_{\mathrm{gr}}/c$ with L_{res} as physical MRR length and group index n_{gr} at the speed of light c. Hence, the maximum DR is governed by the cavity intensity build-up, e.g., the 10–90% rise- and 90–10% fall-times (t_r, t_f), which in terms of cavity round-trips N_{rt} are given by (2) and are predominantly influenced by the MRR perimeter and the bus-to-ring waveguide coupling:

$$N_{\mathrm{rt}} = n_{90\%} - n_{10\%} = \frac{\log\left(\frac{1-\sqrt{0.9}}{1-\sqrt{0.1}}\right)}{\log\left[\tau_1 \cdot \tau_2 \cdot \exp\left(\frac{-\alpha L}{2}\right)\right]}. \tag{2}$$

The maximum DR is further calculated by $\mathrm{DR} = 1/(t_r + t_f)$, which according to (2), results in

$$\mathrm{DR} = \frac{\log\left[\tau_1 \cdot \tau_2 \cdot \exp\left(\frac{-\alpha L}{2}\right)\right]}{2 \cdot \Delta t \cdot \log\left(\frac{1-\sqrt{t_r}}{1-\sqrt{t_f}}\right)}. \tag{3}$$

The DR capability for different bus-to-ring gaps are presented in Fig. 1(a), numerical calculations of the MRR transient response due to 10 and 20 Gb/s input signals are shown in Fig. 1(b). The drop port losses and the full width at half maximum (FWHM) of 10 μm MRRs that reveal the drop loss/bandwidth trade-off for different coupling gaps are summarized in Fig. 1(c). The FWHM decreases for weaker couplings down to ≈60 pm for 300 nm, whereas the filter losses

increase by 4.5 dB from 100 nm to 300 nm. A good compromise that meets the design criteria with a tolerable ease of fabrication is determined for a gap distance of 150 nm, resulting in a drop port loss of $\leq$ 0.8 dB, a FWHM of 0.275 nm, and a possible DR beyond 20 Gb/s with low channel XT of 16.5 dB at the targeted 100 GHz spacing. The wavelength channels $\Delta\lambda_{Ch}$ were defined by a perimeter increment Δl_{Ch} with respect to the initial resonator lengths L_0 with resonance position λ_0 using (4). The calculated through and the drop port spectra of the optimized 8-channel OADM are shown in Fig. 1(d)

$$\Delta\lambda_{Ch} = \frac{L_0 + \Delta l_{Ch}}{L_0} \cdot \frac{\lambda_0}{1 - \frac{\lambda}{n_{eff}(\lambda)} \frac{dn_{eff}}{d\lambda}}. \tag{4}$$

2.2. Photonic Device and Microheater Fabrication

Standard crystalline silicon wafers (10 cm) with 3 μm grown thermal oxide were used as substrates which ensures a negligible power loss due to substrate leakage. The deposited a-Si:H waveguide core layer was deposited with 200 nm thickness which was controlled with ellipsometry. The optimized PECVD-process facilitates the deposition of highly uniform and reproducible thin films with a bulk absorption loss $\leq$ 0.5 dB/cm at 1.55 μm wavelength [2]. The photonic systems were patterned with electron beam lithography using ZEP-520A positive resist. First an O_2 plasma process was carried out in order to smooth the resist which minimizes sidewall roughness, after which, the a-Si:H core layer was subsequently structured by an anisotropic dry etch process with SF_6 and C_4F_8 in an inductively coupled reactive-ion etcher.

Titanium microheaters were fabricated on top of photonic MRRs on reference chips in order to determine the power requirement for the active compensation of the OADMs. The microheaters were optimized with FEM-simulations. The metal-heaters are integrated on top of the photonic structures in order to realize efficient TOE-tuners with low power consumption. The vertical arrangement facilitates a good heat transfer to the photonic components and simplifies the routing of the optical and electrical signals on different layers. Since the electric energy is converted to heat by resistive material losses, the best heating efficiency is achieved with materials that exhibit high electrical resistance and low thermal conductivity. The actual design is a trade-off between heater efficiency, low optical loss due to the highly absorptive metal, robustness, and ease of fabrication. Hence, from the above considerations the microheaters were realized on a 1 μm SiO_2 top cladding with 2 μm wide and 200 nm thick titanium metallic wires in Ω-shape. Using these parameters the FEM simulations provided low parasitic losses $\leq$ 0.02 dB/cm in telecommunication C-band and a steady-state temperature rise of $\Delta T \approx 4.5$ °C at the waveguide for a $P = 1$ mW power dissipation which corresponds to a heater efficiency of about 2.4 mW/nm.

The heater fabrication was carried out on 1.5×1.5 cm^2 chips that were cut from the wafer. The SiO_2 cladding was DC-sputtered on top of the prior structured photonic systems, followed by sputtering the titanium for the heaters and gold for the contact pads. The resulting layer thicknesses were measured with reference chips using laser-ellipsometry and step-height profilometry, respectively. The patterning was performed with I-line exposure contact photo lithography using alignment markers that were etched in the a-Si:H core layer. The metal layers were structured with Au ($KI:I_2:H_2O$) and Ti ($HF:H_2O_2:H_2O$) wet etching until the microheaters were defined.

3. Thermo-Optic Tuning and Post-Fabrication Device Trimming

From the technological and physical perspective, HIC integrated-optic materials like a-/SOI are subject to a trade-off originating from the susceptibility to fabrication imperfections on the one hand, and the distinctly large TOE on the other hand. As a result even sub-nm scale imperfections have a deteriorate impact on the photonic circuit performance, however, due to the strong intrinsic thermo-optic-coefficient (TOC) the compensation of the photonic circuits requires only low tuning powers/voltages for the NU correction. This facilitates the active-tuning and reconfiguration of complex network topologies like ROADMs with considerably less energy compared to low index materials with weaker TOC and with CMOS-compatible voltage levels which should

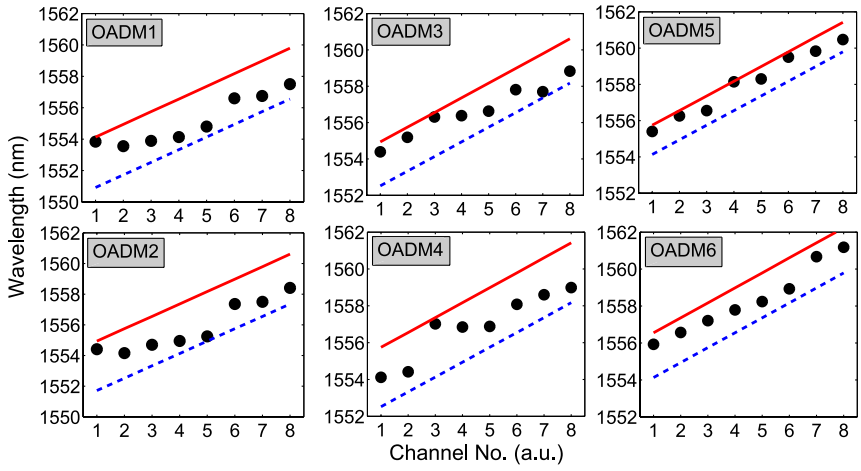

Fig. 2. Resonance peak positions of six as-fabricated 8-channel OADMs. The closest 100-GHz ITU-grid lines on the shorter (dashed blue) and longer (solid red) wavelength side are shown.

not be neglected. Although, low-loss a-Si:H can be deposited with high uniformity and reproducibility [40], the single-mode photonic wire geometry of 480×200 nm^2 is prone to process variations. The MRR spectra will for instance differ by about $\Delta\lambda \approx 0.6$ nm and $\Delta\lambda \approx 1.3$ nm if the waveguide is subject to a 1 nm deviation in widths or heights, respectively, whereas a percentile variation in refractive index (RI) results in $\Delta\lambda \approx 13$ nm relative to the design.

For that reason it is obligatory to equip the photonic circuits with efficient tuning devices like e.g., microheaters or free carrier injectors employing the TOE or free-carrier-dispersion (FCD) effect. However, in contrast to actively controlling the PEIC functionality the NU correction is pure dissipation of energy. Hence, in order to mitigate the disadvantage of the fabrication complexity while keeping the advantage of the high and energy-efficient tuning capability, a method to compensate for fabrication NU and to fine-tune individual photonic circuit components is inevitable for wafer-scale photonic systems even with most-advanced manufacturing. Recently several promising trimming methods have been reported which can make these tuners expendable to some extent, or at least, minimize the effort for the thermal compensation by adjusting the circuit components to their predefined working point so that global cooling/heating options with less manufacturing costs or higher efficiency can be utilized. The most prominent approaches that are used to tailor the guided mode are based on surface oxidation [41], thin film layer deposition or surface etching methods [42], [43], and laser trimming [44], [45].

3.1. Optical Add/Drop Multiplexer Characterization and Device Non-Uniformity

In a first step after fabrication the OADM channel variations were analyzed by measuring the wavelength peak positions of each device. The experimental data which were determined against an air cladding are provided in Fig. 2. The dots represent the measured MRR peak positions whereas the straight lines correspond to the nearest ITU-100 GHz grid to which the single MRR filters need to be adjusted. Note that the thermal tuning due to the increase of the RI results in a positive wavelength shift (solid red), whereas the trimming (dashed blue) induces a RI reduction and hence produces a shift to shorter wavelength. The channel NU of the as-fabricated OADMs with a successive 6 nm (OADM 1/2), 8 nm (OADM 3/4), and 10 nm (OADM 5/6) radius increment for each MRR ($\Delta d = 200$ μm) were determined to be $\sigma_{\lambda_{\text{res}}} = 0.56$ nm, $\sigma_{\lambda_{\text{res}}} = 0.45$ nm, and $\sigma_{\lambda_{\text{res}}} = 0.31$ nm, respectively. With respect to the tight manufacturing constraints the results are in excellent agreement with the design. The deviations of the worst OADM correspond to either a width NU of $\Delta w \approx 1$ nm, height NU of $\Delta h \approx 0.5$ nm, or a RI variation of $\Delta n \approx 5 \cdot 10^{-4}$. For the sake of clarity, the values do not reflect the absolute deviation from design but were calculated from the linear wavelength gradient due to the even perimeter increase.

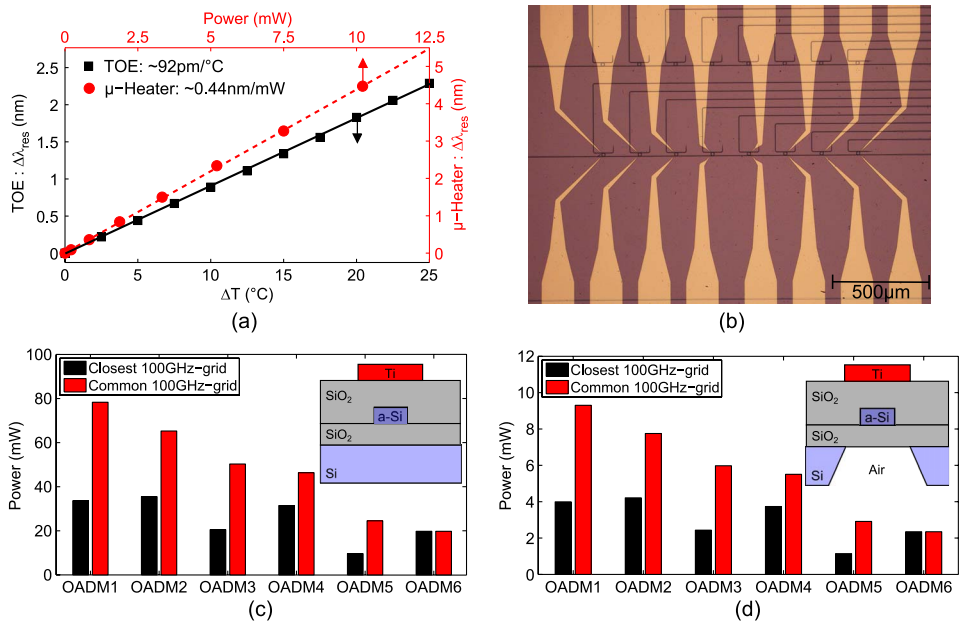

Fig. 3. (a) Measurement of thermo-optic-effect and microheater efficiency. (b) Micrograph of an OADM with heater array on top. (c) Power consumption to configure the OADMs to the nearest possible 100-GHz ITU-grid and to the closest common grid for top heaters. (d) State-of-the-art underetched systems with local substrate removal. The heater types are inset for better comprehension.

3.2. Thermo-Optic Effect and Static Power Consumption

The most prominent and effective method to actively correct fabrication inhomogeneities and to configure photonic components without introducing additional losses is the TOE. The effect originates from the temperature dependence of the RI via the TOC of the material and is treated as a real scalar value (5), shown below, which is appropriate for $T \leq 200\,^{\circ}\mathrm{C}$:

$$\mathrm{TOC} = \Delta n_{\mathrm{aSi}} \approx \frac{\partial n_{\mathrm{aSi}}}{\partial T} \cdot \Delta T. \tag{5}$$

The temperature dependent resonance wavelength shift is calculated by (6), shown below, using the guided mode index n_{eff} which includes the contribution of the cladding materials. The strong a-Si:H TOC of about $2.1 \cdot 10^{-4}$ $(1/^{\circ}\mathrm{C})$ facilitates an efficient MRR tuning of complex photonic systems [1], [46], up to about $\Delta\lambda_{\mathrm{res}} = 20$ nm with a linear relationship upon temperature and a wavelength set resolution in the pm-range [47]

$$\Delta\lambda_{\mathrm{res}} = n_{\mathrm{eff}} \frac{\partial n_{\mathrm{eff}}}{\partial T} \cdot \frac{\lambda_{\mathrm{res}}}{n_{\mathrm{gr}}} \cdot \Delta T. \tag{6}$$

The TOE of 92 pm/°C was experimentally determined by heating the photonic chip in $\Delta T = 2.5\,^{\circ}\mathrm{C}$ increments using a thermo-electric controlled chip-mount as shown in Fig. 3(a). The microheaters were wire-bonded to a PCB board and were characterized with different voltages applied to the heater contact pads as illustrated in Fig. 3(b). The microheater tuning efficiency of 2.25 mW/nm (about 20 mW/FSR) was determined from Fig. 3(a) which is comparable to best-in-class top heaters based on SOI [42]. The experimental results are in close agreement with the FEM-simulations. A further reduction of the energy consumption employing the same heaters can be realized by a local removal of the silicon substrate which acts as a heat sink [48], [49].

The total power consumption for the active NU compensation of all eight MRRs within the devices are analyzed for two realistic, although, still simplified scenarios. We investigate the power that is required to correct the channels to the nearest possible ITU-100 GHz grid (NG) of each

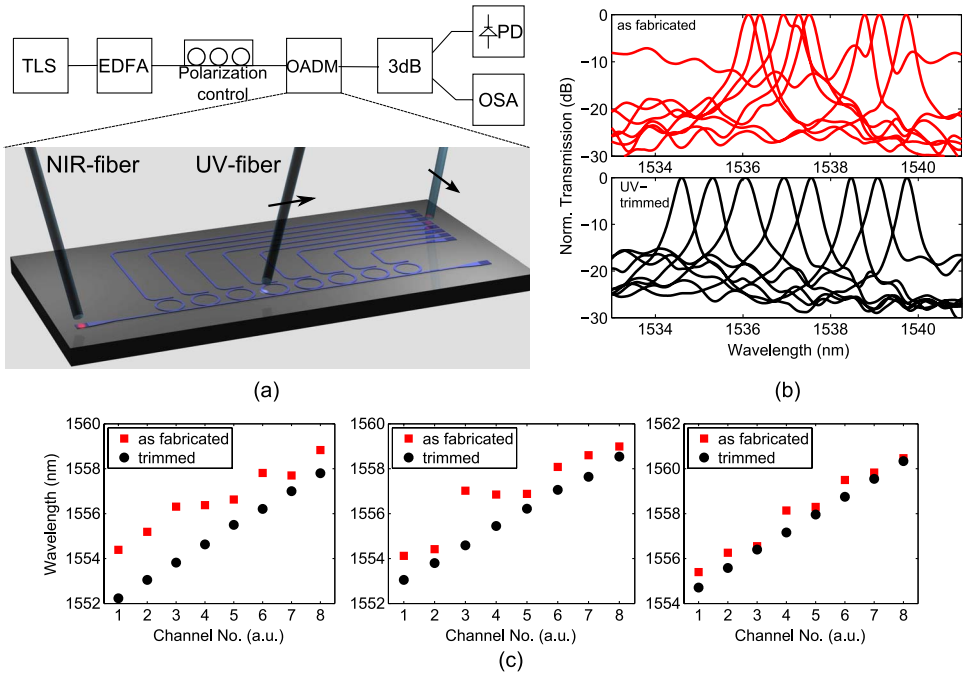

Fig. 4. (a) Optical characterization and in-line trimming setup with a schematic picture of the locally selective OADM trimming using a UV-fiber. (b) Close view of the OADM-drop channels which are corrupted by fabrication non-uniformity in comparison with the corrected device. (c) Resonance wavelengths of the OADMs before and after postfabrication trimming.

single OADM, and the case where all OADMs need to operate on the closest common grid (CG). The results using the heater efficiency of our top heaters for the analysis are provided in Fig. 3(c). Furthermore, the calculations for suspended OADMs with local substrate removal using the benchmark value of 2.4 mW/FSR reported in [48] are summarized in Fig. 3(d). The average power per device that is required to set all OADM channels to the grid were determined to be $P_{NG} = 25.06$ mW $(P_{CG} = 47.41$ mW$)$ with the standard top heaters and $P_{NG} = 2.98$ mW $(P_{CG} = 5.63$ mW$)$ in case of the underetched photonic systems. Thermal crosstalk is negligible due to the strong a-Si:H TOE and the relatively large distance of 200 μm between the MRRs.

3.3. Device Correction by UV-Laser Trimming

Although the TOE is ideally suited to actively configure PEICs the correction of fabrication imperfections is a waste of energy. For this task a permanent and passive device trimming is more advantageous because it results in a significant reduction of the static power consumption, which becomes a crucial issue for 100 or even 1000 devices per wafer. In this work, a low-cost continuous wave UV-laser with 405 nm wavelength was used for the OADM trimming. The measurement setup and an illustration of the trimming strategy is depicted in Fig. 4(a). Since the devices were designed for a SU-8 cladding the MRRs were trimmed against air in order to exclude the influence of the polymer bleaching.

The NIR-light was supplied to the photonic chip via grating couplers and was inline-monitored during trimming. The UV-light was coupled into a single-mode fiber by a collimator such that the cleaved facet could be positioned with μm-precision on top of the photonic MRRs which were successively trimmed to their target position. Further information about the trimming process is reported in [45]. Fig. 4(b) provides an example of the drop port channels before and after trimming, the spectral positions of three trimmed devices that are plotted against their channel counts are presented in Fig. 4(c). The channel NUs after the device correction were determined

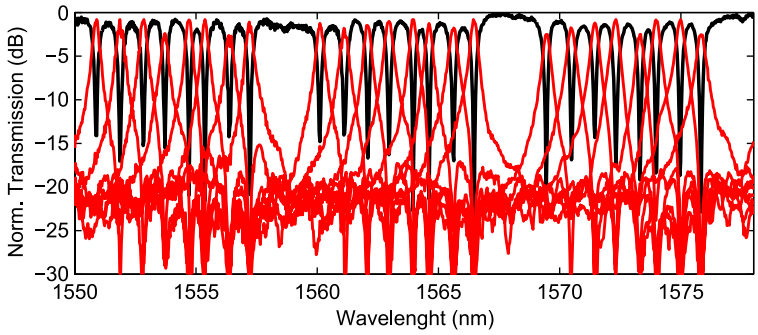

Fig. 5. OADM through and drop port spectra after the channel adjustments and SU-8 spin-coating.

TABLE 1

Experimentally determined key metrics of the OADM filters in comparison with the design parameters

Property	Design	Fabricated & Trimmed
Q-factor (a.u.) / FSR (nm) / Finesse	5800 / 9.31 / 35	5700±250 / 9.25 / 33.5±2
Mean drop loss (dB)	0.8	≈1.25
Mean X-Talk (dB)	16.5	≈15
Non-adjacent channel isolation (dB)	22.5	≥20
Mean ER through/drop (dB)	15 / 27.5	≈15 / ≥22.5

to be $\sigma_{\lambda_{res}} \approx 0.03$ nm, $\sigma_{\lambda_{res}} \approx 0.07$ nm, and $\sigma_{\lambda_{res}} \approx 0.024$ nm, respectively. The transmission spectra of an OADM after fine-trimming which was cladded with SU-8 after the channel adjustments is presented in Fig. 5. The grating coupler envelopes are subtracted from the spectra for a better visibility. A comparison with the design from Section 2.1 is given in Table 1. The results are in good agreement and the OADM channel positions are well-defined without the need for any active tuning.

4. Experimental Result Discussions and Trimming Prospects

Active-tunable and wavelength-trimmable OADM filter banks with 8-channels based on a-SOI photonic MRRs are systematically analyzed. The low-footprint devices exhibit low drop port losses of ≤ 1.25 dB, a mean channel crosstalk of 15 dB, and an overall device insertion loss of ≤ 2 dB. The as-fabricated photonic devices are examined for fabrication induced device NU and the static power consumption which is required to configure the individual channels to the nearest and a common 100 GHz frequency grid is evaluated for two heater versions. The results demonstrate that due to the low device NU it is possible to realize truly energy-efficient and compact photonic filters and networks-on-chip by employing the strong TOE of the a-Si:H material. Considering the isolated energy/bit metrics which are required to compensate the channel NU for a 20 Gb/s DR, the OADMs can operate with 157 fJ/bit (NG), 296 fJ/bit (CG) in case of standard top heaters and with 18.6 fJ/bit (NG), 35.2 fJ/bit (CG) for more-efficient underetched heaters. Nevertheless, even these low single device power budgets scale with the number of circuit elements and significantly increase the overall consumption and the thermal load of the photonic circuit, in particular for macroscale photonic interconnect architectures like those envisioned for data-center and high-performance computing systems with many thousands or even millions of devices.

Hence, trimming methods are essential tools in order to enhance the energy-efficiency of PEICs. It is projected that the static and dynamic tuning can account for 20–30% of the overall

photonic link power [50], or even up to 50%, depending on the network topology [51]. As presented in this work the trimming can almost completely avoid the static energy consumption, for instance, translating the remaining device NU into energy/bit metrics results in $\leq$ 10 fJ/bit with standard top heaters and about 1 fJ/bit with underetched heaters for DRs exceeding 10 Gb/s per channel. Apart from spectral channel accuracy, another important issue of OADMs is to ensure critical coupling. Indeed, the trimming is applicable to modify the strength of the evanescent field coupling, although the effect is limited for standard MRRs. Instead, racetrack or pulley resonators with a higher directional coupler sensitivity due to RI modification [52], [53], or even more suited, ring-assisted Mach–Zehnder-interferometers that can be tailored by a phase change in the interferometer arm can provide a flexible control of both, critical coupling and 3 dB-bandwidths [54], [55].

However, even with post-fabrication trimming approaches the thermal control of photonic circuits is necessary in many applications, in particular, for reconfigurable circuits that share common resources like lasers and detectors. In this context the flexible fabrication and the possibility to deposit a-Si:H on top of the microheaters is a valuable option because the components can be actively-tuned by buried TOE-tuners whereas the circuit trimming for NU-correction can be applied from the top after finishing the complete manufacturing cycle.

Besides these manufacturing challenges, a further significant source of the PEICs energy consumption originates from the run-time compensation of thermal fluctuations on chip and ambient temperature. Hence, a reduction of the thermal susceptibility is another key issue to realize low-energy photonic systems [56], [57]. Recently, we demonstrated that it is possible to compensate photonic wires of same dimensions used in this work and that second-order ring filters can be stabilized over $\Delta T = 40\ ^{\circ}\mathrm{C}$ and up to $\Delta\lambda = 100$ nm without any significant performance drawbacks [46].

The thermal-compensated PEICs provide the additional advantage that the photonic devices can operate even under varying thermal loads that are introduced by spatially close active-tunable photonic devices or hotspots originating from CMOS-electronics during operation. However, if the photonic circuits are based on athermal waveguides the TOE is canceled out and therefore the trimming becomes even more essential for the NU correction. Otherwise weaker effects like e.g., FCD need to perform the compensation, which indeed is favorable in case of modulators, nevertheless, due to the limited tuning range $(\Delta\lambda_{\mathrm{res}} \leq 1\ \mathrm{nm})$ and additional optical loss introduced by free-carriers seems less appropriate to compensate passive devices [56], [58]. Presently, our laboratory setup relies on manual adjustments and is restricted to trim single devices; however, automated systems with step-and-repeat processing during device inspection including the usage of pulsed lasers, e.g., in the fs-time regime [59], and/or spatial light modulators might prove to be viable solutions for high-throughput photonic chip or full-wafer trimming.

5. Conclusion

We designed, fabricated, and systematically characterized 8-channel OADMs based on CMOS backend-compatible a-Si:H and investigated the static power consumption for non-uniformity compensation. The active-tunable and wavelength-trimmable filters are built with low-footprint MRRs and were realized on a 100 GHz DWDM grid. The experimental results demonstrate the potential of a-SOI as a viable material platform for the realization of high bandwidth interconnects on a small area and in form of 3-D photonic circuits on top of microelectronics. The as-fabricated filter banks can operate at relatively low power levels due to the pronounced thermo-optic-coefficient which facilitates an effective tuning or reconfiguration of photonic circuit components. Even more importantly, we demonstrate that a-Si:H exhibits excellent material properties for a post-fabrication correction of the device imperfections enabling to minimize the power consumption and temperature overhead of such circuits significantly via a highly-accurate permanent trimming method. Hence, the relatively high static power contribution due to unavoidable manufacturing tolerances, even though among the lowest reported data on any integrated optic material platform, can be almost completely avoided paving the way for densely integrated and ultra-low-power photonic 3-D-network architectures.

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References

[1] G. Cocorullo *et al.*, "Amorphous silicon waveguides and light modulators for integrated photonics realized by low-temperature plasma-enhanced chemical-vapor deposition," *Opt. Lett.*, vol. 21, no. 24, pp. 2002–2004, Dec. 1996.
[2] A. Harke, M. Krause, and J. Mueller, "Low-loss single mode amorphous silicon waveguides," *Electron. Lett.*, vol. 41, no. 25, pp. 1377–1379, 2005.
[3] M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," *Nat. Photon.*, vol. 4, no. 8, pp. 492–494, 2010.
[4] L. C. Kimerling *et al.*, "Electronic-photonic integrated circuits on the CMOS platform," in *Proc. SPIE*, San Jose, CA, USA, Feb. 2006, vol. 6125, pp. 612 502–612 510.
[5] J. M. Fedeli *et al.*, "Development of silicon photonics devices using microelectronic tools for the integration on top of a CMOS wafer," *Advances in Optical Technologies*, vol. 2008, Art. ID. 412518.
[6] M. Heck *et al.*, "Hybrid silicon photonic integrated circuit technology," *IEEE J. Sel. Top. Quantum Electron.*, vol. 19, no. 4, Jul./Aug. 2013, Art. ID. 6100117.
[7] J. Mueller, M. Mahnke, G. Schoer, and S. Wiechmann, "Inorganic materials integrated optics," in *Proc. AIP Conf.*, 2004, vol. 709, pp. 268–289.
[8] C. C. Evans, C. Liu, and J. Suntivich, "Low-loss titanium dioxide waveguides and resonators using a dielectric lift-off fabrication process," *Opt. Exp.*, vol. 23, no. 9, pp. 11160–11169, 2015.
[9] M. Pollnau, "Rare-earth-ion-doped channel waveguide lasers on silicon," *IEEE J. Sel. Top. Quantum Electron.*, vol. 21, no. 1, pp. 414–425, Jan./Feb. 2015.
[10] L. Cao, A. Aboketaf, Z. Wang, and S. Preble, "Hybrid amorphous silicon (a-Si:H)-LiNbO3 electro-optic modulator," *Opt. Commun.*, vol. 330, pp. 40–44, Nov. 2014.
[11] W. Pernice, C. Xiong, F. Walker, and H. Tang, "Design of a silicon integrated electro-optic modulator using ferroelectric $BaTiO_3$ films," *IEEE Photon. Technol. Lett.*, vol. 26, no. 13, pp. 1344–1347, Jul. 2014.
[12] S. Fathpour, "Emerging heterogeneous integrated photonic platforms on silicon," *Nanophoton.*, vol. 4, no. 1, pp. 143–164, May 2015.
[13] J. Tian, S. Yu, W. Yan, and M. Qiu, "Broadband high-efficiency surface–plasmon–polariton coupler with silicon–metal interface," *Appl. Phys. Lett.*, vol. 95, no. 1, 2009, Art. ID. 013504.
[14] H. Wassel *et al.*, "Opportunities and challenges of using plasmonic components in nanophotonic architectures," *IEEE Trans. Emerging Sel. Topics Circuits Syst.*, vol. 2, no. 2, pp. 154–168, Jun. 2012.
[15] H. C. *et al.*, "All-plasmonic Mach–Zehnder modulator enabling optical high-speed communication at the microscale," *Nat. Photon.*, vol. 9, no. 8, pp. 525–528, Aug. 2015.
[16] S. K. Selvaraja *et al.*, "Low-loss amorphous silicon-on-insulator technology for photonic integrated circuitry," *Opt. Commun.*, vol. 282, no. 9, pp. 1767–1770, May 2009.
[17] R. Sun, J. Cheng, J. Michel, and L. Kimerling, "Transparent amorphous silicon channel waveguides and high-q resonators using a damascene process," *Opt. Lett.*, vol. 34, no. 15, pp. 2378–2380, Aug. 2009.
[18] T. Lipka, O. Horn, J. Amthor, and J. Müller, "Low-loss multilayer compatible a-Si:H optical thin films for photonic applications," *J. Eur. Opt. Soc. Rap. Publicat.*, vol. 7, 2012, Art. ID. 12033.
[19] K. Furuya *et al.*, "Nanometer-scale thickness control of amorphous silicon using isotropic wet-etching and low loss wire waveguide fabrication with the etched material," *Appl. Phys. Lett.*, vol. 100, no. 25, pp. 251108–251113, 2012.
[20] R. Takei *et al.*, "Sub-1 db/cm submicrometer-scale amorphous silicon waveguide for backend on-chip optical interconnect," *Opt. Exp.*, vol. 22, no. 4, pp. 4779–4788, 2014.
[21] A. Harke *et al.*, "Amorphous silicon 3-D tapers for Si photonic wires fabricated with shadow masks," *IEEE Photon. Technol. Lett.*, vol. 20, no. 17, pp. 1452–1454, Sep. 2008.
[22] H. Yoda *et al.*, "A two-port single-mode fiber-silicon wire waveguide coupler module using spot-size converters," *J. Lightw. Technol.*, vol. 27, no. 10, pp. 1315–1319, May 2009.
[23] J. Cheng and N. Yan, "Three-step lithography to the fabrication of vertically coupled micro-ring resonators in amorphous silicon-on-insulator," *Chin. Opt. Lett.*, vol. 13, no. 8, 2015, Art. ID. 082201.
[24] J. Kang *et al.*, "Amorphous-silicon inter-layer grating couplers with metal mirrors toward 3-D interconnection," *IEEE J. Sel. Top. Quantum Electron.*, vol. 20, no. 4, pp. 317–322, Jul./Aug. 2014.
[25] R. Takei *et al.*, "Low-loss and low wavelength-dependence vertical interlayer transition for 3d silicon photonics," *Opt. Exp.*, vol. 23, no. 14, pp. 18 602–18 610, Jul. 2015.
[26] M. Hammer, A. Hildebrandt, and J. Förstner, "How planar optical waves can be made to climb dielectric steps," *Opt. Lett.*, vol. 40, no. 16, pp. 3711–3714, Aug. 2015.
[27] Y. Shoji *et al.*, "Ultrafast nonlinear effects in hydrogenated amorphous silicon wire waveguide," *Opt. Exp.*, vol. 18, no. 6, pp. 5668–5673, Mar. 2010.
[28] K. Narayanan, A. W. Elshaari, and S. F. Preble, "Broadband all-optical modulation in hydrogenated-amorphous silicon waveguides," *Opt. Exp.*, vol. 18, no. 10, pp. 9809–9814, May 2010.

[29] B. Kuyken *et al.*, "Nonlinear properties of and nonlinear processing in hydrogenated amorphous silicon waveguides," *Opt. Exp.*, vol. 19, no. 26, pp. B146–B153, Dec. 2011.
[30] J. Matres *et al.*, "High nonlinear figure-of-merit amorphous silicon waveguides," *Opt. Exp.*, vol. 21, no. 4, pp. 3932–3940, Feb. 2013.
[31] C. Lacava *et al.*, "Nonlinear characterization of hydrogenated amorphous silicon waveguides and analysis of carrier dynamics," *Appl. Phys. Lett.*, vol. 103, no. 14, 2013, Art. ID. 141103.
[32] X. Gai, D.-Y. Choi, and B. Luther-Davies, "Negligible nonlinear absorption in hydrogenated amorphous silicon at 1.55 m for ultra-fast nonlinear signal processing," *Opt. Exp.*, vol. 22, no. 8, pp. 9948–9958, Apr. 2014.
[33] S. Suda *et al.*, "Optical-time-division demultiplexing of 172 Gb/s to 43 Gb/s in a-Si:H waveguides," *IEEE Photon. Technol. Lett.*, vol. 26, no. 5, pp. 426–429, Mar. 2014.
[34] J. J. Wathen *et al.*, "Non-instantaneous optical nonlinearity of an a-Si:H nanowire waveguide," *Opt. Exp.*, vol. 22, no. 19, pp. 22 730–22 742, Sep. 2014.
[35] S. Rao, F. Della Corte, C. Summonte, and F. Suriano, "Electrooptical modulating device based on a CMOS-compatible a-Si:H—A-SICN multistack waveguide," *IEEE J. Sel. Top. Quantum Electron.*, vol. 16, no. 1, pp. 173–178, Jan./Feb. 2010.
[36] F. Corte and S. Rao, "Use of amorphous silicon for active photonic devices," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1495–1505, May 2013.
[37] Y. H. D. Lee, M. O. Thompson, and M. Lipson, "Deposited low temperature silicon GHz modulator," *Opt. Exp.*, vol. 21, no. 22, pp. 26 688–26 692, Nov. 2013.
[38] T. Lipka, J. Amthor, H. K. Trieu, and J. Müller, "Travelling wave resonators fabricated with low-loss hydrogenated amorphous silicon," in *Proc. SPIE*, 2013, vol. 8767, p. 876707.
[39] J. Park, S. Park, and G. Kim, "Transient analysis of static and dynamic responses for a single ring-resonator-based WDM add/drop filter array," *Opt. Quantum Electron.*, vol. 44, no. 15, pp. 731–740, Dec. 2012.
[40] T. Lipka, J. Amthor, and J. Müller, "Process and device uniformity of low-loss a-Si:H," in *Proc. IEEE IPC*, 2012, pp. 923–924.
[41] C. J. Chen *et al.*, "Selective tuning of high-q silicon photonic crystal nanocavities via laser-assisted local oxidation," *Opt. Exp.*, vol. 19, no. 13, pp. 12 480–12 489, Jun. 2011.
[42] A. H. Atabaki, A. A. Eftekhar, S. Yegnanarayanan, and A. Adibi, "Sub-100-nanosecond thermal reconfiguration of silicon photonic devices," *Opt. Exp.*, vol. 21, no. 13, pp. 15 706–15 718, Jul. 2013.
[43] S. Chandran and B. Das, "Surface trimming of silicon photonics devices using controlled reactive ion etching chemistry," *Photon. Nanostruct.*, vol. 15, pp. 32–40, Jun. 2015.
[44] D. Bachman *et al.*, "Permanent fine tuning of silicon microring devices by femtosecond laser surface amorphization and ablation," *Opt. Exp.*, vol. 21, no. 9, pp. 11048–11056, May 2013.
[45] T. Lipka, M. Kiepsch, H. K. Trieu, and J. Müller, "Hydrogenated amorphous silicon photonic device trimming by UV-irradiation," *Opt. Exp.*, vol. 22, no. 10, pp. 12122–12132, May 2014.
[46] T. Lipka, L. Moldenhauer, J. Müller, and H. K. Trieu, "Athermal and wavelength-trimmable photonic filters based on TiO2-cladded amorphous-SOI," *Opt. Exp.*, vol. 23, no. 15, pp. 20075–20088, 2015.
[47] T. Lipka *et al.*, "Label-free photonic biosensors fabricated with low-loss hydrogenated amorphous silicon resonators," *J. Nanophoton.*, vol. 7, no. 1, Jan. 2013, Art. ID. 073793.
[48] P. Dong *et al.*, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Exp.*, vol. 18, no. 19, pp. 20298–20304, Sep. 2010.
[49] J. Amthor *et al.*, "Fabrication of freestanding SiO_2 membrane systems for thermo-optic adjusting of SOI photonic wires," *IEEE Photon. Technol. Lett.*, vol. 23, no. 16, pp. 1142–1144, Aug. 2011.
[50] A. Krishnamoorthy, H. Schwetman, X. Zheng, and R. Ho, "Energy-efficient photonics in future high-connectivity computing systems," *J. Lightw. Technol.*, vol. 33, no. 4, pp. 889–900, Feb. 2015.
[51] J. Ahn *et al.*, "Devices and architectures for photonic chip-scale integration," *Appl. Phys. A*, vol. 95, no. 4, pp. 989–997, Jun. 2009.
[52] E. Shah Hosseini *et al.*, "Systematic design and fabrication of high-q single-mode pulley-coupled planar silicon nitride microdisk resonators at visible wavelengths," *Opt. Exp.*, vol. 18, no. 3, pp. 2127–2136, Feb. 2010.
[53] M. J. Strain *et al.*, "Tunable q-factor silicon microring resonators for ultra-low power parametric processes," *Opt. Lett.*, vol. 40, no. 7, pp. 1274–1277, Apr. 2015.
[54] L. Chen, N. Sherwood-Droz, and M. Lipson, "Compact bandwidth-tunable microring resonators," *Opt. Lett.*, vol. 32, no. 22, pp. 3361–3363, 2007.
[55] H. Shen *et al.*, "Eight-channel reconfigurable microring filters with tunable frequency, extinction ratio and bandwidth," *Opt. Exp.*, vol. 18, no. 17, pp. 18067–18076, 2010.
[56] Z. Li *et al.*, "Reliability modeling and management of nanophotonic on-chip networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 1, pp. 98–111, Jan. 2012.
[57] Z. Zhou *et al.*, "Lowering the energy consumption in silicon photonic devices and systems," *Photon. Res.*, vol. 3, no. 5, pp. B28–B46, 2015.
[58] R. A. Soref and B. Bennett, "Electrooptical effects in silicon," *IEEE J. Quantum Electron.*, vol. 23, no. 1, pp. 123–129, Jan. 1987.
[59] D. Bachman *et al.*, "Permanent phase correction in a polarization diversity Si PIC by femtosecond laser pulses," *IEEE Photon. Technol. Lett.*, vol. 27, no. 17, pp. 1880–1883, Sep. 2015.