Probing and Fixturing Techniques for Wideband Multiport Measurements in Digital Packaging

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Abstract

This thesis deals with test signal probing and fixturing techniques for wideband multiport measurements in digital packaging in the frequency range from a few MHz to 50 GHz. Three different signal launch techniques are investigated in time and frequency domains. At first, the performance of the coaxial surface mounted connector launch is explored in case of crosstalk measurements in a backplane connector via pin field. In the next step the recessed probe launch technique is briefly presented. After that the main focus is on the results obtained in recent investigations with respect to the launch calibration, application to measurements of embedded multilayer structures and modifications to improve the launch bandwidth. Finally, the concept of a novel multiport probing fixture is presented and its electrical performance explored. Using a simple two-tier calibration procedure, the effect of the probing fixture on measurements of dense via array structures is reduced and the results obtained are validated with microprobe based measurements. Based on 3D full-wave electromagnetic modeling, suggestions for layout optimization are made which will be needed to extend the applicability of these techniques to data rates of 20 Gbit/s and beyond.

Kurzfassung

Diese Arbeit befasst sich mit der Testsignalkontaktierung und Signaleinführungstechniken für breitbandige Multitor-Messungen im Bereich der Aufbau- und Verbindungstechnik für digitale Systeme im Frequenzbereich von wenigen MHz bis 50 GHz. Drei verschiedene Signaleinführungstechniken werden im Zeit- und Frequenzbereich untersucht. Zuerst wird die Leistungsfähigkeit der Kontaktierung mit koaxialen Steckern in Messungen des Übersprechens von Backplane-Stecker analysiert. Im nächsten Schritt wird die “Recessed Probe Launch“-Technik präsentiert, wobei die Ergebnisse aus aktuellen Untersuchungen in Bezug auf ihre Kalibration, ihre Anwendungen für Messungen von eingebetteten Multilagen-Strukturen und mögliche Modifizierungen für die Verbesserung der Messbandbreite im Mittelpunkt stehen. Schließlich wird das Konzept eines neuartigen Multitor-Adapters präsentiert und seine Hochfrequenz-Eigenschaften untersucht. Mittels eines zweistufigen Kalibrationsverfahrens wird der Einfluss des Multitor-Adapters in den Messungen von dichten Via Array Strukturen reduziert und die Ergebnisse mit Microprobe-Messspitzen basierten Messungen validiert. Basierend auf 3D Vollwellen-Simulationen werden Vorschläge für die Optimierung des Layouts gemacht, die für die Anwendbarkeit dieser Technik für Datenraten bis 20 Gbit/s und darüber hinaus notwendig sind.

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Contents

List of Symbols and Acronyms

Notation

x, y, z	Cartesian coordinates

Symbols

V_0	Amplitude of the inserted step voltage
V_r	Amplitude of the obtained reflected voltage
ω	Angular frequency
α	Attenuation constant
T_b	Bit time
F_{-3dB}	Bandwidth of the low-pass filter of a time domain oscilloscope
C	Capacitance
Z_0	Characteristic impedance
σ	Conductivity
I	Current
$tan\delta$	Dielectric loss tangent
$\Delta\varphi_{eff}$	Effective phase difference
f	Frequency
$f_{\lambda/4}$	Frequency at a quarter-wavelength
F_{notch}	Frequency where a deep notch appears in the transmission parameters
$\boldsymbol{I}$	Identity matrix
j	Imaginary unit
L	Inductance

f_{max}	Maximum frequency of interest
T_{signal}	Period
μ_0	Permeability of free space (~ $4\pi \cdot 10^{-7}$ H/m)
ε_0	Permittivity of free space (~ $8.854 \cdot 10^{-12}$ F/m)
β	Phase constant
γ	Propagation constant
T_{single}	Propagation time of a single discontinuity
μ_r	Relative permeability
ε_r	Relative permittivity
R	Resistance
t_r	Rise time
T_{meas}	Rise time delivered at the end of a probe or a fixture
T_{TDR}	Rise time in accordance with the TDR module data sheet
S	S-parameter
t	Time
Δl	Trace length mismatch
T	Transformation matrix for currents (modal decomposition)
l	Transmission line/ trace length
λ	Wavelength
Y	Y-parameter
Z	Z-parameter

Acronyms

2D	Two Dimensional
3D	Three Dimensional
ABCD	Microwave Network Chain Parameters
AC	Alternating Current
ATE	Automatic Test Equipment
BGA	Ball Grid Array

CM	Common-Mode
CPW	Coplanar Waveguide
CS	Calibration Substrate
DC	Direct Current
DDR	Dual Data Rate (for random access memories)
DR	Data Rate
DUT	Device Under Test
ECAL	Electronic Calibration Module
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEM	Finite Element Method
FEXT	Far-end Crosstalk
FFT	Fast Fourier Transform
FIT	Finite Integration Method
GND	Ground
GS	Ground Signal
GSG	Ground Signal Ground
HDMI	High Definition Multimedia Interface
HFSS	High Frequency Structure Simulator (FEM Solver)
IBM	International Business Corporation
IC	Integrated Circuit (or chip)
IEEE	Institute of Electrical and Electronics Engineers
LGA	Land Grid Array
LRM	Line-Reflect-Match (Calibration Procedure)
LRRM	Line-Reflect-Reflect-Match (Calibration Procedure)
MMSNT	Microwave Measurement Software
NEXT	Near-end Crosstalk
PCB	Printed Circuit Board
PI	Power Integrity
PLTS	Physical Layer Test System
PTFE	Polytetrafluorethylen

QSOLT	Quick-Short-Open-Load-Thru (Calibration Procedure)
RF	Radio Frequency
RPL	Recessed Probe Launch
RPM	Revolutions Per Minute
S-	Microwave Network Scattering Parameters
SATA	Serial Advanced Technology Attachment
SG	Signal Ground
SI	Signal Integrity
SMA	SubMiniature version A
SMP	SubMiniature Push-On
SMT	Surface Mount Technology
SOL	Short-Open-Load (Calibration Procedure)
SOLR	Short-Open-Load-Reciprocal (Calibration Procedure)
SOLT	Short-Open-Load-Thru (Calibration Procedure)
SWR	Standing Wave Ratio
TDR	Time Domain Reflection
TDT	Time Domain Transmission
TEM	Transverse ElectroMagnetic
TET	Institut für Theoretische Elektrotechnik, TUHH
TL	Transmission Line
TRL	Thru-Reflect-Line
TUHH	Technische Universität Hamburg-Harburg
TV	Test Vehicle
VNA	Vector Network Analyzer

In this work board and structure dimensions are often given in mils, which are the typical units used in the electronic industry. The conversions to SI units are as follows:

$1\,\text{inch} \approx 2.54 \cdot 10^{-2}\,\text{m}$

$1\,\text{mil} = 0.001\,\text{inch} \approx 25.4 \cdot 10^{-6}\,\text{m}$

1. Introduction

1.1. Motivation and Context of this Work

The communication between high speed digital components and systems, represented in data centers as links between servers, links on backplanes between plug-in cards and between devices on a board, implies thousands of electrical and optical signal paths, which have to provide stable signal propagation and enough channel bandwidth to handle the continuously increasing signal data rates. Looking at the progress of initial bit rate per channel of common protocols such as InfiniBand, PCI-express and SATA, one can determine that every new generation doubles its data rate compared to its predecessor.

The international technology roadmap of semiconductors (in 2003) predicted that processor frequencies will exceed 30 GHz by 2018, and that off-chip signaling interface speeds are expected to exceed 56 Gigabits/s [1] - [3]. Optimization of the bandwidth, power, pin count, or number of wires and costs are the goals for high-speed interconnect design. It is a fact that many high-performance chips are often limited by off-chip interconnects whose bandwidth is restricted by noise and timing limitations of package, board, and cable [4]. Driven at these high frequencies, interconnects face signal integrity problems such as skin effect and dielectric losses, reflection noise from impedance discontinuities attributable to vias, connectors and trace impedance tolerances, mode conversion and crosstalk in package via fields and board connectors, which can lead to latent field failures if they are not identified in the development phase (Figure 1.1). Proper design and optimization of these high speed digital interconnects is a comprehensive challenge for engineers using different modeling techniques, simulation tools, and measurement equipment in an attempt to reduce the signal degradation to a minimum and to ensure that the system will pass the required specification and compliance standards [4] - [6].

This work contributes to the design and modeling of multiport probing fixtures and associated broadband test signal launches for measurement and characterization of embedded structures present in digital packaging and in multilayer substrates.

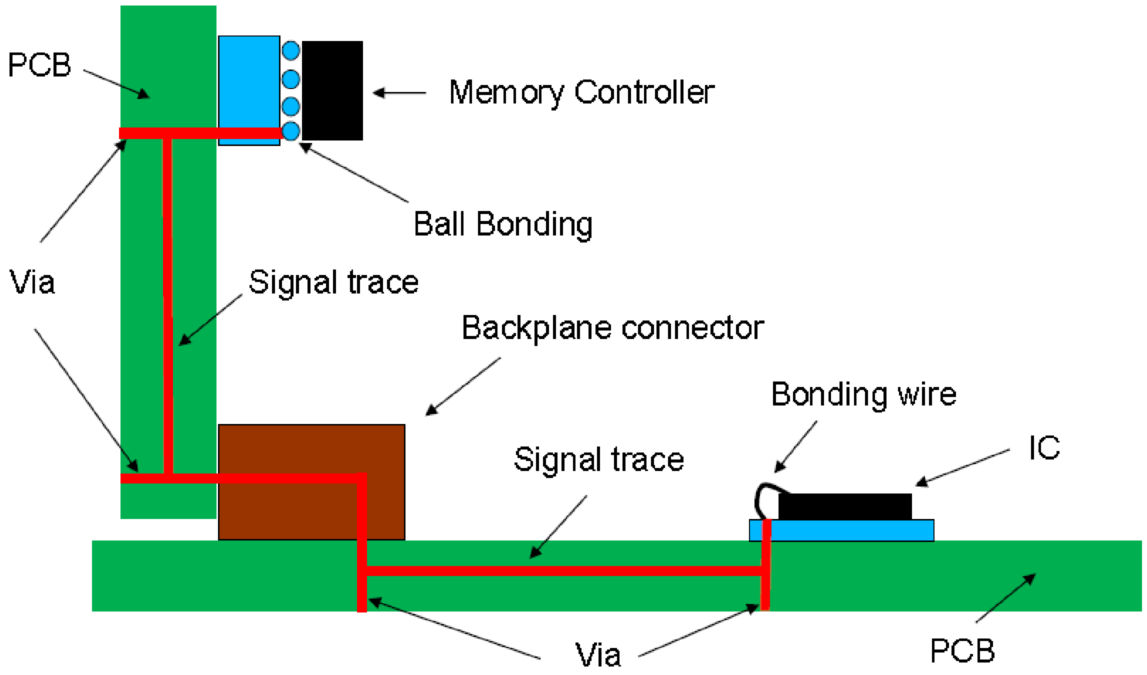


Figure 1.1 Typical high speed digital link scenario considered from the signal integrity perspective. Starting from the memory controller, the main discontinuities are represented by the vias in the package underneath the controller, the via-to-trace transition, the vias of the connector footprint and the vias in the package of the IC and the bonding of the vias in the package and the IC.

1.2. Organization of the Work

The outline of this thesis is as follows.

Chapter 2 presents typical multiport probing issues in dense via structures prevalent in digital packaging. A brief overview is given on the time and frequency domain measurement techniques. The measurement issues and challenges present in signal integrity applications in multilayer substrates are then related to multiport vector network analyzer calibration and probing techniques.

Chapter 3 addresses common multiport measurement techniques based on surface mounted connector signal launches, that are used for investigations of dense via array structures found in backplane connector footprints. The results obtained from frequency domain crosstalk analyses confirm effects seen in previous time domain investigations and extend the knowledge about the crosstalk dependency on different via coupling scenarios present in high speed digital links.

Chapter 4 deals with the design, modeling and characterization of broadband microprobe based signal launches – on-surface and recessed - for measurements of embedded structures in multilayer printed circuit boards. Using full-wave electromagnetic solvers, the recessed probe launch technique has been explored and optimized meeting the recommendations of the signal integrity applications. With the help of two-tier calibration techniques combining commercial and self implemented algorithms a model-to-hardware correlation of the proposed launch models was established.

Chapter 5 presents a novel custom-made multiport probing fixture for measurements in dense via arrays. The mechanical clamping and fixturing are described. Results from the de-embedding of the probing fixture applying custom-made calibration substrates and link measurements obtained by using two probing fixtures are presented. The correlation to probe based measurements performed on the same links are taken into consideration at the end.

Chapter 6 summarizes the main results of this work. The contributions of this thesis are reviewed and recommendations for further research work suggested.

1.3. Conference and Journal Contributions

Within the scope of this work several conference contributions [7] -[14] have been made - in the area of microwave measurement and de-embedding techniques applying multiport vector network analyzers, modeling, characterization and optimization of microprobe based signal launches and multiport probing fixtures for measurements on multilayer substrates. These publications constitute a fundamental part of this thesis. During the development of this project the author has also contributed to publications in related topics [15] - [18].

2. Measurement Challenges in Digital Packaging

In this Chapter, the key challenges of making broadband multiport measurements of high speed digital packaging are addressed. In addition, some basic conditions needed to perform reliable time and frequency domain measurements are reviewed. An overview of common calibration algorithms used in 2-port and multiport vector network analyzer configurations is given focusing mainly on self-calibration algorithms. The advantages and disadvantages of time and frequency domain measurement techniques are presented at the end.

2.1. Signal Launch Techniques and Measurement Challenges

Most of the measurement equipment available in high frequency measurement laboratories such as the time domain reflectometer oscilloscope and the vector network analyzer provide the connection to test devices with ports. Usually the high frequency test devices consist of planar structures implemented on substrates and multilayer printed circuit boards in which contact pads are accessed by microstrip line and stripline structures. Several coaxial connectors, fixtures, and microprobe configurations with 50 Ω characteristic impedances are currently available which provide the test signal transition from the measurement port and cables to the test devices (Figure 2.1). For all mentioned signal launch techniques, the main goal is to design an on-surface launch with smooth coaxial-to-microstrip line (stripline) junction where mainly the fundamental mode propagates to the planar structure (Figure 2.1). Unfortunately, the electrical field distribution for both transmission line configurations is such that when the frequency increases in the region of the junction of the coaxial to microstrip line (stripline) reflections and the excitation of high order modes are to be expected [19], [20]. Signal integrity engineers are aiming to design transparent test signal launches in multilayer PCBs in order to reduce signal distortion issues such as loss, reflection, mode conversion, and crosstalk which become problematic with increasing measurement frequencies [21]. As depicted in Figure 2.1 both connector and probe based signal launches rely on the signal transition from the board surface to the embedded structure

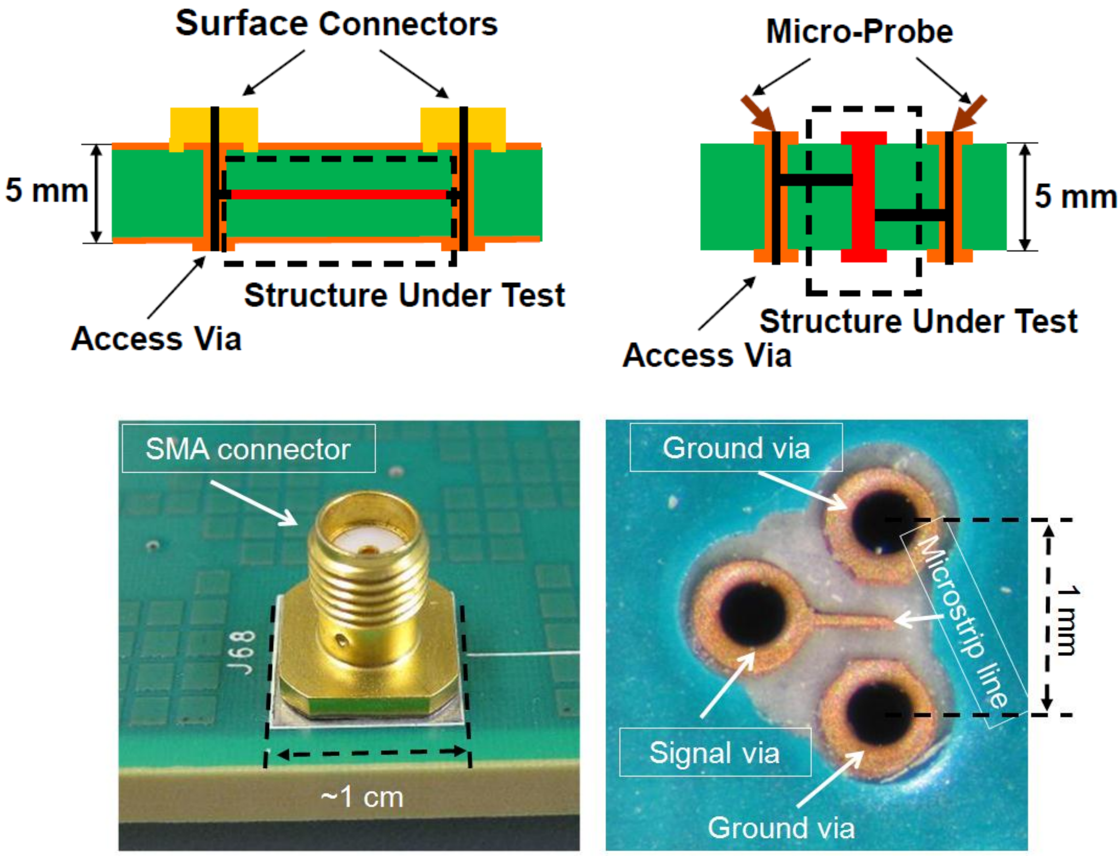


Figure 2.1 Typical on-surface signal launch techniques using surface mounted connectors (e.g. an SMA depicted on the **left**) and microprobe launches (e.g. GSG probe launch shown on the **right**) [7].

(stripline, via) through an access via. Typically, such an access via appears as a bottleneck for the transition of the test signal to the DUT (device under test). Removing the impact of such vias from the frequency response of the structure under test is a complicated process, which usually relies on de-embedding techniques. The validity of this procedure assumes that corresponding DUT and "calibration" structures behave identically. Yet recent via modeling efforts show that vias are sensitive to their local environment and the relatively loose mechanical tolerances available in PCB manufacturing (±10 %) exacerbate this problem [22]. A dedicated test signal launch, which overcomes the access via issue called the recessed probe launch (RPL), was presented in [23]. As shown there, after precise milling of the upper board layers, microprobes can be positioned close to the DUT, which allows high frequency measurements of PCB structures. A contribution to the analysis and optimization of this launch technique was done in the framework of this thesis and is summarized in Section 4.6.

In recent years the signal data rates in high speed digital systems have drastically increased. In order to achieve the overall bandwidth requirements, such digital systems consist of hundreds to thousands of parallel channels operating at high frequencies. In such systems, even though multilayer substrates are used, adjacent channels are routed in close proximity in dense via arrays, which can be found under chip packages and connectors (Figure 2.2). These dense via array structures constitute a confluence of several heretofore disparate concerns and deserve careful attention during the design process. In such multiport configurations, users have to handle not only measurement bandwidth limitation issues but also spatial restrictions due to the dimensions of the investigated device. In both cases, the maximum number of simultaneously accessible measurement ports is determined by the smallest possible test signal pitch (minimum possible signal-to-signal distance between two adjacent measurement ports) and the spatial placement of the used connectors or microprobes/positioners (Figure 2.3). Yet the signal-to-signal pitch in via arrays is often in the range of 1 mm or even less.

For multiport applications, most of the probe manufacturers offer custom configured multipin probe towers and probe cards for mounting in automatic test equipments (ATE) or in manual test stations (Figure 2.4). Different probe configurations are available with higher port counts but usually they are expensive and standard calibration coupons are not widely available [24], [25].

However, engineers are often constrained to use single port probes due to cost limitations or the fact that probes mounted in micropositioners are flexible and easy to move. For measurements of high speed digital link structures the application of more than four measurement ports is a common requirement especially if the crosstalk behavior of adjacent channels has to be taken into account. When increasing the number of used measurement ports, one faces issues such as additional test board space for on-surface mounting/launching of the adapters and probing fixtures, application of a proper multiport calibration algorithm, and substrates.

In Figure 2.2, a measurement set up for multiport measurements in a dense via array structure (1 mm grid) is shown, where the signal-to-signal row and column pitch measures 80 and 57.6 mils respectively. Even using narrow body style single port probes, one faces some spatial limitations, e.g. when more than four adjacent measurement ports have to be simultaneously accessed. As shown in Figure 2.3, the minimum pitch for parallel probes is 13 mm and the minimum angular separation is in the range of 35° - 45°. Depending on the probe design, cable strain reliefs, and microprobe positioners these limitations can vary.

Nevertheless, in recent years the demand for high port count time and frequency domain measurements has greatly increased as measurement data is still needed to establish confidence in various modeling approaches. In the following Sections, some fundamental requirements for obtaining reliable measurement data and achieving a proper high speed interconnect design are reviewed.

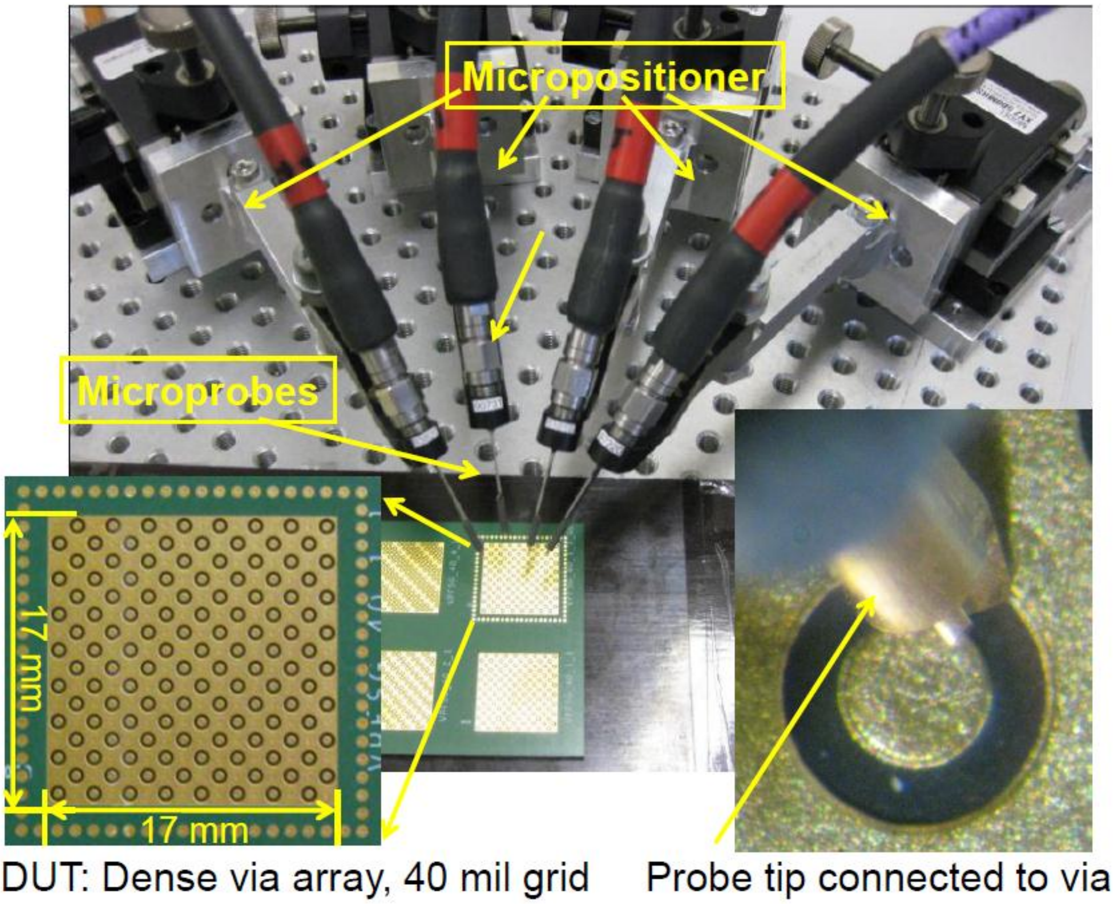


Figure 2.2 Typical dense via array (40 mil grid) used for applications in the signal and power integrity containing 68 signal and 192 ground vias.

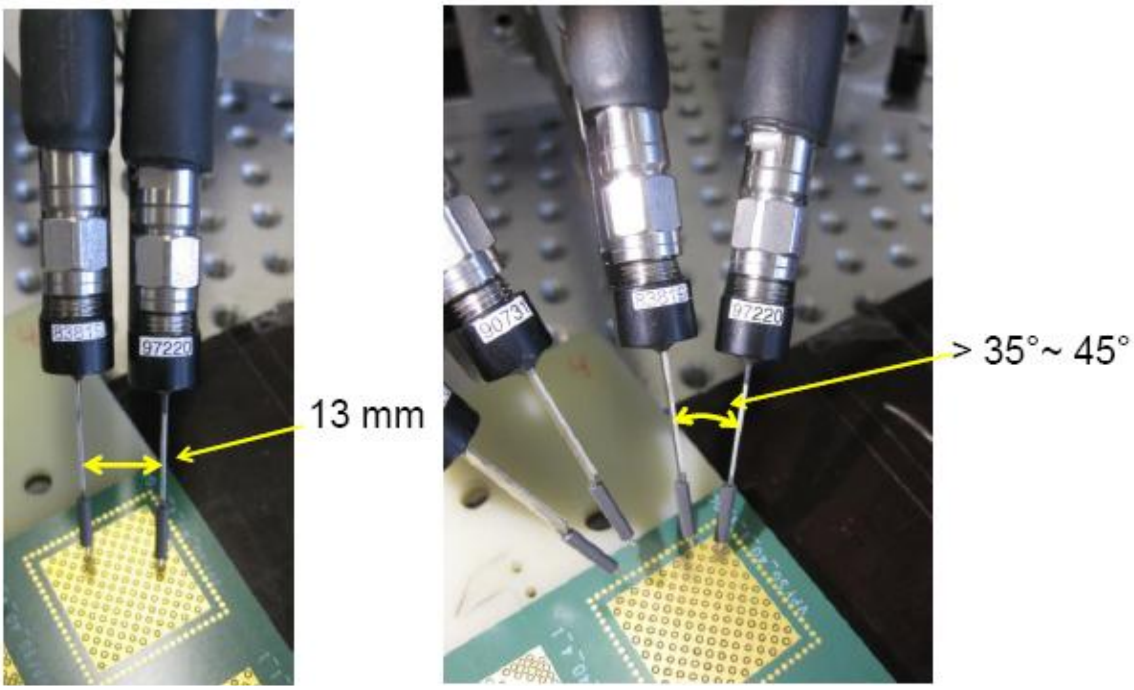


Figure 2.3 Spatial restrictions using commercial microprobes: The minimum pitch for parallel probes is 13 mm and the minimum angular separation is in the range of 35°-45° [15].

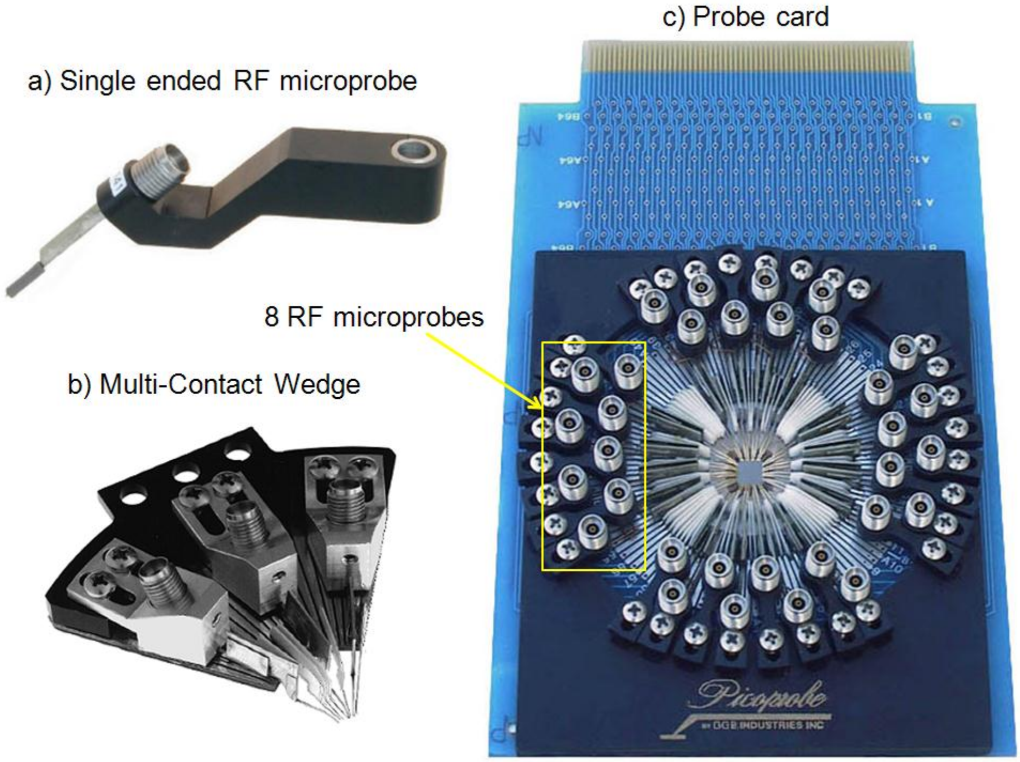


Figure 2.4 Typical RF single ended and multiport probing fixtures: a) single ended RF probe, b) multi-contact wedge and c) probe cards for mixed RF and DC measurements and for testing wafers, chips or packages on either manual or automatic probe stations. Photographs courtesy of GGB Industries, Inc. [24].

2.2. Signal Bandwidth in High Speed Digital Systems

The design of digital systems and components on printed circuit boards requires the accurate prediction of the signal propagation on interconnect structures, which typically represent combinations of cables, connectors, vias and traces. In order to describe and optimize their electrical behavior, interconnects are usually modeled as distributed models or transmission lines. The reliable interconnect modeling is based on measurements in time and/or frequency domain with respect to the compliance of digital communication standards such as SATA, InfiniBand, and HDMI (Table 2.1). In other words, the signals have to be transmitted to the receivers at the desired data rates by the interconnects in such way that their reconstruction at the link end stays feasible within an ever more stringent power budget. In recent years, the crosstalk issue in high speed digital interconnects is increasing in importance as data rates increase, even more than the link transmission characteristic itself. In the area of the signal integrity, the crucial factor for the reconstruction of a digital signal at the channel end and for keeping the present crosstalk as low as possible is represented by the signal rise time (T_r). The needed signal bandwidth of an interconnect for the proper transmission

TABLE 2.1 TYPICAL DATA RATES AND THE APPROPRIATE MINIMUM RISE TIME NEEDED FOR RELIABLE DESIGN OF HIGH SPEED DIGITAL LINK SYSTEMS.

Standard	**Data rate [Gbit/s]**	**Bit width [ps]**	**Rise time [ps]**
Infiniband	2.5	400	100
PCI Express	2.5	400	50
SATA II 1st generation	3.0	333	67
XAUI	3.125	320	60
4 Gb/s FC	4.25	235	60
SATA II 2nd generation	6	167	N/A
Double XAUI	6.25	160	N/A
8 Gb/s FC	8.5	118	N/A
10 G Base-R	10.31	97	24
10 G Base-R FEC	11.10	90	24

of digital signal with signal rise time of T_r can be estimated from the following formula [26]:

$$F_{-3dB} = \frac{k}{T_r} \tag{2.1}$$

Typically, the rise time is defined from some intermediate level considering the low and high level, e.g. 10 % - 90 % or 20 % - 80 % are common definitions. The factor k is related to the low-pass characteristic of the interconnect structures and varies typically between 0.33 - 0.6, which depends on the step response of the interconnect structure e.g. for a structure with Gaussian filter response $k = 0.33$.

The signal rise time T_r of given signal data rate (DR) can be estimated as shown in Appendix A.1, and based on it the maximum upper measurement bandwidth for the applied measurement equipment can be determined, e.g. in case of a digital signal with DR of 10 Gbit/s the maximum frequency content might be 25 GHz or 50 GHz depending on the assumptions which were made in [27].

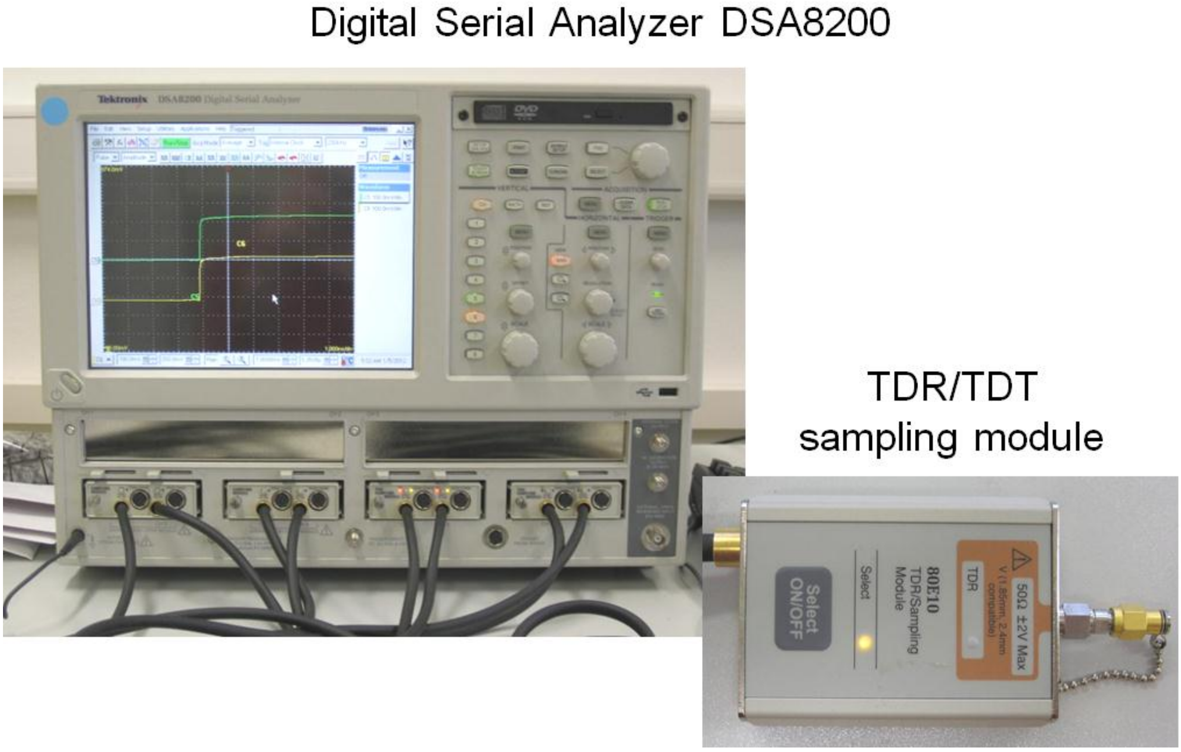


Figure 2.5 A 4-port time domain reflectometer oscilloscope available in the laboratory of the Institute of Electromagnetic Theory, TUHH.

The presented relations between signal rise time and the minimum required measurement bandwidth have been taken into account for the time and frequency domain measurements in the frame of this thesis. As shown in the following Chapters the time domain measurements were basically used for the spatial localization of the interconnect discontinuities and the characterizations of their physical behavior applying a time domain sampling oscilloscope (Figure 2.5).

For the frequency domain measurements a vector network analyzer (Figure 2.6) was used as an alternative to the time domain measurements for the characterization of the test launches and interconnects. Furthermore, the VNA offers adequate correction of error induced by the measurement equipment (e.g. cables, adapters, probes, fixtures) and thus it is more advantageous for multiport measurements with respect to the crosstalk behavior in dense via array structures.

2.3. Time Domain Characterization of Interconnect Discontinuities

The time domain reflectometry (TDR) is based on an impedance measurement principle, which allows to locate faults in test devices, where a voltage step is sent to the test device and after obtaining the reflected waveforms, one can determine the physical behavior of the fault by interpreting the impedance changes of the reflected waveform [26], [28]. For the estimation of discontinuities as shunt capacitances and serial inductances the following formulas have been provided [29], [30]:

$$V_r = -\frac{x \cdot C \cdot Z_0}{2 \cdot T_r} V_0 \tag{2.2}$$

The value of a serial inductance can be estimated with:

$$V_r = \frac{L \cdot x}{2 \cdot Z_0 \cdot T_r} V_0 \tag{2.3}$$

where V_0 corresponds to the amplitude of the inserted step voltage, V_r is the obtained reflected voltage, x is the percentage of the T_r (0.6 (for 60%) or 0.8 (for 80%) or even 1 (for 100%)), and Z_0 is the characteristic impedance [29], [30]. In order to achieve accurate estimation of the discontinuities sufficient spatial resolution of the applied TDR oscilloscope has to be guaranteed which depends on the T_r. For this purpose, the minimum propagation delay between two closely spaced discontinuities has to be not less than the half of the rise time of the falling edge ($T_d \geq \frac{T_r}{2}$). Otherwise, both discontinuities will be not clearly distinguished from each other [28]. Furthermore, single discontinuity cannot be observed if its propagation time T_{single} is very small. Good rule of thumb for the propagation time of a single discontinuity is that $0.1 \cdot T_r < T_{\text{single}} < 0.2 \cdot T_r$ [28].

All mentioned limits and rules lead one to the conclusion that an adequate estimation of the rise time is required. Typically, TDR oscilloscopes are connected to the DUT using cables, probes or test (probing) fixtures which degrade the rise time T_r and thus reduce the spatial resolution of the instrument. The delivered rise time T_{meas} at the end of the probe or fixtures can be estimated using the following formula [26]:

$$T_{meas} \sim \sqrt{T_{TDR}^2 + 2 \cdot \left(\frac{0.35}{F_{-3dB}} \right)^2} \tag{2.4}$$

Further applications of the TDR oscilloscope comprise the extraction of characteristic impedances of transmission lines using impedance peeling algorithms (inverse scattering algorithms) and the so-called lattice diagram [30]. This method is based on the assumption that the loss of the interconnection between measurement port and DUT is negligible. If this assumption is not fulfilled, time domain calibration methods can be applied such as Thru-Match-Short (TMS) in order to reduce the effects from discontinuities on the time domain response of the DUT. To apply the calibration methods for the time domain network analysis the measured voltages obtained from the measurement of the calibration substrates are converted to frequency domain using Fast Fourier Transformation and then applied to the calibration algorithms [31].

Alternative methods for reducing the effect from cables and probes are the de-embedding techniques using subtraction and windowing. The time domain de-embedding requires the design of reference fixture, which reproduces only the effects induced from the fixture in the measurement set up, in order to subtract them from the application of the fixture to the measurement of the DUT. The accuracy of the subtraction method depends on the matching of the reproduced effects on the reference fixture. The windowing in time domain is realized when the scan of the time is limited. In order to achieve adequate accuracy the time-domain window has to include at least one-half wavelength distance at the maximum frequency involved [32].

Furthermore, the time domain reflectometer oscilloscope allows transmission measurements which can be used for extraction of models and dielectric parameters of the substrates. The measurement of crosstalk in time domain reveals the amount of the coupled voltage amplitude to the input of an adjacent link (backward coupling) and to the end of an adjacent link (forward coupling) and additionally the physical characteristic of the forward coupling can be determined, e.g. either inductive or capacitive [30], [33]. Another common time domain measurement technique is the generation of eye diagram which gives an overview over the general jitter behavior of the digital signal propagating on the interconnect. Eye diagrams are good visual tools mainly for rough estimation of the signal distortion in the investigated interconnect [26].

As presented in the following Sections, the focus of this thesis were the measurements in frequency domain and thus more attention is given to the network analysis applying a vector network analyzer (VNA) and its calibration.

2.4. Multiport Measurements and Calibration in Frequency Domain

During the late 1950s, the need for reliable measurement standards began to be an important factor when performing measurements at RF and microwave frequencies. The first reference impedance standards in the form of precision coaxial air lines were presented in [34], [35]. Due to the fact that these lines used high conductivity metal conductors and an air dielectric, their properties were easily predictable and their electrical characteristics resemble ideal transmission lines [36], [37]. It did not take long for the first fully automated vector network analyzer to be introduced in late 1960s in [38], [39]. This laid the basis for the further development of the measurement and calibration techniques using VNAs [40], [41].

In measurement applications using vector network analyzers, typically the measurement setup requires that the measurement cables are connected to its front-panel connectors, and often additional coaxial adapters are placed between the cable end and microprobe or test device. All these components induce additional effects on the measured data, which contribute to the measurement error. The calibration of these effects is called error correction and the nature of these measurement errors can be classified into three groups [42]:

- Systematic errors – are caused by imperfection of the VNA hardware, cables, adapters and fixtures. If it is guaranteed that these errors do not vary over the time, they can be characterized using proper calibration methods and their effect can be removed from the measurement data.
- Random errors – vary as a function of the time and typically are caused by the VNA hardware in the form of noise induced by the samplers, IF noise floor, repeatability of the switches and connectors. Normally, they cannot be predicted and thus cannot be calibrated out. Their effects can be reduced by increasing the source power, narrowing the IF filter bandwidth or trace averaging over multiple frequency sweeps.
- Drift errors – are induced by changes of the environmental conditions, such as temperature and humidity. In order to minimize the effects of temperature drifts, the VNA calibration has to be frequently repeated and the environmental conditions be kept as stable as possible.

In general, the error correction depends on the applied calibration method and the definitions of the calibration standards [43]. For S-parameter measurements with a VNA, systematic errors are described with so-called error models which represent relations of error coefficients. The number of the error coefficients in the error model depends on the hardware topology of the VNA, the number of VNA measurement ports and receivers and the required measurement accuracy [40], [44], [45].

The concept of the error model was introduced in relation to the error correction for the first automated vector network analyzer in case of one port measurements [38], [39]. The so-called 3-term model represents the basis of the one port Short-Open-Load (SOL) calibration which is the most common used error correction routine in the VNA calibration algorithms [43], (Appendix A.2). In case of 2-port bidirectional S-parameter measurements, the number of error parameters is increased to 8, whereas the 8-term model is the common model for most available calibration algorithms [46]. The 8-term model can be reduced to 7-terms as shown in the Thru-Reflect-Line (TRL) calibration algorithm in [47] and might be applied to the most available VNA systems [48].

Further error models were derived: In case of unidirectional measurements the error model can be represented by 5 error terms or even by 6 terms when signal leakage between the measurement ports is considered [49]. Including the leakage terms (crosstalk terms), the 8-term approach can be extended to the 10 (12)-term model [50]. Later on the 10 (12)-term error model was introduced for commercial VNAs and became a standard error model for the two-port VNA independently on the hardware configuration. Hence, the 10 (12)-term model can be found in all modern 2-port VNA instruments nowadays independently on the hardware configuration with only one reference receiver or one reference receiver for every measurement channel (double-reflectometer VNA). Several studies have been performed in order to convert the 7-term error models to 10-term due to the fact that 7-term models are not accurate for error correction of one reference receiver VNAs [46], [48], [51].

Further studies with that regard have shown that the 7-term error model is often insufficient to describe the leakage paths in the case of n-port VNA hardware with only two error terms; thus for accurate representation of the leakage paths, the number of the error terms was extended to 2n-port models connected to the n-port DUT [52]. The suggested error network then consists of $(2 \cdot n)^2$ error coefficients, which fully represent the complex leakage behavior in the VNA and the influence of the measurement ports on each other. Choosing one of the error parameters as free parameter allows the normalization of the rest parameters to this term and thus only $4 \cdot n^2 - 1$ parameters have to be computed as shown in [53]. Here, it is important to note that this assumption is valid in case of double-receiver VNA configurations. Further error term reductions can be achieved if the influence of the crosstalk from the measurement receivers can be omitted - then an error model containing only $4 \cdot n - 1$ error coefficients can be applied [54].

In some measurement scenarios, the crosstalk between adjacent ports cannot be fully ignored e.g. dual microprobes with signal tips in close proximity without an intervening ground tip. In such microprobe tip configurations, the crosstalk of two ports per probe is large. In such applications, one can split the error model into two groups and the $4 \cdot n^2 - 1$ error parameter model reduces to $2 \cdot n^2 - 1$ error coefficients as suggested in [55], [56].

The error coefficients are computed with help of the calibration algorithms, which are broadly classified into algorithms requiring all the calibration standards to be fully known and self-calibration algorithms where only some standards need to be known. A common calibration algorithm requiring the description of all used standards is the Short-Open-Load-Thru (SOLT) method presented in [57]. The TRL calibration algorithm as introduced in [47] was the first self-calibration procedure which did not require all standards to be exactly known. Another advantage of this algorithm is that the redundancy inherent in the measurement yields the reflection coefficient of the reflection standard and the propagation constant of the line standard. This is very useful for applications related to the extraction of material parameters of the substrates. The disadvantage of this algorithm is that TRL is frequency band limited

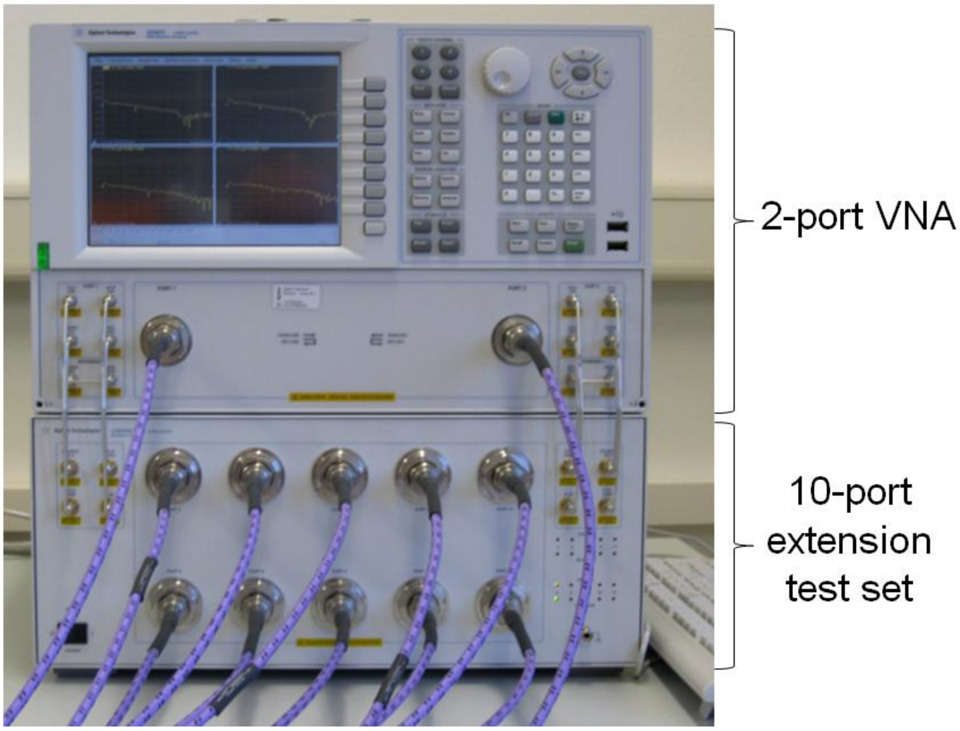


Figure 2.6 A 12-port vector network analyzer available in the laboratory of the Institute of Electromagnetic Theory, TUHH.

and to overcome this bandwidth limitation additional line standards have to be applied [58], [59]. In principle, the self-calibration algorithms rely on the 7-term error model and are suitable for double-reflectometer VNAs. In general, these algorithms are based on the fact that for the computation of the calibration network matrix, only 7 equations are needed and the algorithms derive 12 equations. This redundancy allows the application of particularly known standards and provides more freedom when combining them for different calibration methods [60] - [62]. Some popular self-calibration algorithms are listed below:

- Line-Reflect-Match (LRM) – is an alternative calibration procedure which overcomes the frequency bandwidth limitation of the TRL algorithm, where instead of the line standard two one-port load terminations are used [63].
- Short-Open-Load-Reciprocal (SOLR) – does not require the full characterization of the thru standard. Any passive two port reciprocal network could be used for the calibration. The SOL standards have to be fully known [64].
- Quick-Short-Open-Load (QSOLT) – requires all standards to be known but its advantage is that the one-port standards do not need to be measured at the second VNA port and thus the calibration time could be reduced [65], [66]. For some applications the accuracy at the second port might be not sufficient as shown in [67].

- Line-Reflect-Reflect-Match (LRRM) –is a typical calibration method for on-wafer applications and considers calibration issues caused by the load standard, which is a potential asymmetry source and its impedance is often frequency dependent [68]. Similar to the QSOLT method, this algorithm does not need the measurement of the load standard at the second VNA port and the measurement accuracy at this port is also reduced.

Self-calibration algorithms are available for the leaky VNA systems in the form of 15 (16)-term error model, which require additional calibration standards and the number of calibration measurements is indeed extended as shown in [69] -[72]. In case of the 16-term LRM calibration method, four fully known two port calibration standards are needed: thru, match-match, open-short, and short-open [73].

For the error correction in multiport VNA configurations (Figure 2.6), the 7-term calibration procedures are more common due to the fact that they are less sensitive to inaccuracies of calibration standards as presented in [74], [75]. Another advantage of the 7-term approach is that error coefficients can be computed when combined with different calibration algorithms (so-called hybrid calibration) e.g. SOLR and LRM as shown in [76], [77]. Unfortunately, hybrid calibration procedures often have dynamic range limitations due to the 7-term error model as presented in [78]. However, generalized calibration procedures which overcome issues of the 7-term, the 10-term and the hybrid methods have also been derived, e.g. the generalized Reflect-Reflect-Match-Thru calibration algorithm as proposed in [79], [80].

The hybrid and the dynamic calibration methods represent the basis for some multiport calibration software tools e.g. Agilent PLTS ([81]), Cascade WinCal ([82]) and MMSNT ([83], [84]). The calibration software MMSNT 3.3 (microwave measurement software) has been used for the multiport probe based measurements presented in Section 4. This tool is based on the dynamic calibration principle and thus allows the user to mix-and-match multiple calibration algorithms and standards [44]. Furthermore, the software automatically computes the optimal calibration standard sequence in order to minimize the number of needed connections and to reduce the calibration time.

In the next Section the advantages and disadvantages of the time and frequency domain measurement techniques are briefly presented.

2.5. Time domain vs. Frequency Domain

Even though it has become a trend for the VNA manufacturers to extend the functionality of the VNA hardware, different VNA configurations can be found where time domain transformations have been implemented in order to combine both measurement domains into one with the same measurement equipment. One key advantage of the time domain mode is the possibility to switch “easily” between both

TABLE 2.2 TIME DOMAIN VS. FREQUENCY DOMAIN MEASUREMENT TECHNIQUES: OVERVIEW ON THE ADVANTAGES AND DISADVANTAGES OF BOTH MEASUREMENT SYSTEMS.

Metric	**Time Domain**	**Frequency Domain**
Equipment cost	Less expensive	More expensive
Dynamic range	~ 40dB	> 100dB
Maximum measurement frequency	< 100 GHz	>100 GHz
Frequency content	broadband	narrow band, high Q
Tools compatibility	-	+
Correlation to physical features	+	+/-
Concatenation	-	+
Handling	frequently used by digital designers, easier to setup	usually more complicated to set up
Precision (repeatability) limited by launches	not currently emphasized	essential for calibration/de-embedding
Accuracy	TDR/TDT (few % full scale)	set by standards
Benefit	direct fault locations capability	highly developed calibration techniques

measurement domains by applying Inverse Fourier Transform technique. Hence, novel VNAs with a time domain option are able to be driven in modes such as lowpass and bandpass modes for fault location and impedance variations (TDR/TDT), time domain gating for the elimination of unwanted discontinuities in adapters and launches, and windowing which were features once limited to time domain reflectometer oscilloscopes in the past [43], [85]. The differences between the two measurement techniques are depicted in Table 2.2, [86], [87]. As shown there, other aspects for the selection of the measurement domain which might play a role are e.g. cost, dynamic range, maximum measurement bandwidth, ability of concatenating measurement data (cascading measurement data of individual network Sections), and equipment handling. As discussed in the previous Section in the recent years, several calibration algorithms, de-embedding techniques, and appropriate calibration substrates have been developed for the vector network analyses and thus VNAs became more and more popular. Nevertheless, for applications such as direct fault location, time domain oscilloscopes are more preferred than VNAs.

2.6. Summary

This Chapter has shown major challenges of multiport measurements in dense via array structures, found in connector footprints and underneath packages. In addition to the bandwidth limitation issues of the interconnect structures, electrical engineers have to overcome spatial restrictions in measurement set ups due to inappropriate cable strain reliefs, connector dimensions and commercial microprobe configurations. Multiport probes and probe cards are offered by most of the manufacturers, which often have to be designed for a particular test structure.

With respect to measurement equipment, several multiport configurations are available for measurements in either time or frequency domain. Recently multiport VNAs have offered flexible dynamic calibration algorithms, which allow mixing and matching of different calibration standards. Hence, the required calibration effort can be reduced with less loss of accuracy.

There is still a need for multiport probing fixtures utilizing simple calibration and de-embedding techniques in order to ensure reliable multiport measurements in dense via arrays. This thesis contributes to these topics in the following Chapters where three signal launch techniques for measurements in dense via arrays are considered - application of SMA on-surface connectors, RF microprobes, and multiport interposers - and their advantages and disadvantages are discussed.

3. Measurements Using Surface Mounted Connectors

This Chapter addresses a common multiport measurement technique for investigations on dense via arrays in multilayer PCBs located in backplane connector footprints. The measurement technique is based on test signal launching with coaxial surface mounted SMA connectors which are connected to the dense via structures using long striplines for the signal transition from the top board side to the via structures of interest. Applying common TDR/TDT and VNA measurement techniques some limitations of the used SMA signal launch will be located. Furthermore, the results from the application of this SMA signal launch for crosstalk investigations of different via coupling scenarios in a backplane connector footprint are presented obtained by a 12-port VNA.

3.1. Bandwidth of Surface Mounted Connectors

Typically, in the area of the SI coaxial cables and connectors with a characteristic impedance of 50 Ω are applied. This value was chosen as a compromise for a minimum loss and a maximum power capacity considering the fact that for an air-filled coaxial line the minimum attenuation is achieved by a characteristic impedance of 77 Ω and the maximum power capacity can be obtained by a characteristic impedance of 30 Ω [34], [35]. Hence, the 50 Ω characteristic impedance became the reference characteristic impedance for most measurement hardware and equipment applied in the network analysis [19]. In parallel, with the aim to achieve repeatable and reproducible measurements, several precision coaxial connectors were developed during the late 1950s [88], [89]. To this end, an IEEE subcommittee was established which specified the standards for these precision connectors [90].

As mentioned in Chapter 2, coaxial surface mounted connectors are commonly used for on-surface signal launches when digital packages are investigated in time and frequency domain measurements. Typical requirements for such connectors are e.g. low standing wave ration (SWR), high-order-mode-free operation at a high frequency, high repeatability after a connect-disconnect cycle and mechanical strength [19]. In Table 3.1 some common 50 Ω connectors are listed where the maximum usable frequency is

TABLE 3.1 FREQUENCY LIMITATIONS OF COMMON SURFACE MOUNTED CONNECTORS*

Connector type	Frequency Limit	Dielectric
SMA	25 GHz	PTFE
3.5 mm	26.5 GHz	Air
2.92 mm or K	40 GHz	Air
2.4 mm	50 GHz	Air
1.85 mm or V	60 GHz	Air
1 mm	110 GHz	Air

*Further details about coaxial connectors can be found in [19], [91].

defined with safety margin of 5 % from the corresponding cutoff frequency beyond which the undesired propagation of the TE_{11} mode is expected to appear in the connector structure. Here, it is important to note that the costs for the coaxial connectors increase proportionately to the maximum useable frequency and SI engineers have to find the trade-off between useable bandwidth and costs. Indeed, for applications in multilayer substrates as PCB the utilization of connectors with frequency limits much higher than the required minimum bandwidth might be not rational due to expected PCB manufacturing tolerances (~ ±10 %) which additionally degrade the electrical performance of the connector signal launch even it has been carefully designed. Typical requirement for the design of test signal launches for measurements of embedded structures with characteristic impedances in the range of 50 Ω ±10 % presents the -20 dB maximum allowed reflection of the signal launch. In order to investigate this launch characteristic measurements in time and frequency domain have been performed on the multilayer test board used for the crosstalk investigation in the backplane connector via pin field in the next Section.

The electrical performance of the SMA launches on the test board shown in Figure 3.1 and Figure 3.2 was explored in time domain using the time domain reflectometer oscilloscope shown in Chapter 2 (Figure 2.5). Measurement results from the step responses of four SMA connector launches on the multilayer PCB are presented in Figure 3.3. The variations of the connector launches can be clearly seen according to the discontinuities of the signal transition from the SMA adapter to the SMA surface mounted connector and the transition from the SMA access via to the stripline on the signal layer. The variations of the first discontinuity (SMA adapter-to-surface mounted connector) can be explained with mechanical variations of the SMA connector due to the connector wasting by the connect-disconnect cycles and its mechanical manufacturing tolerances. As depicted in Figure 3.3 the largest discontinuity is represented by the signal access via-to-stripline transition. The amplitude variations (between 33 mV and 29 mV) let one to detect the effect of the PCB manufacturing

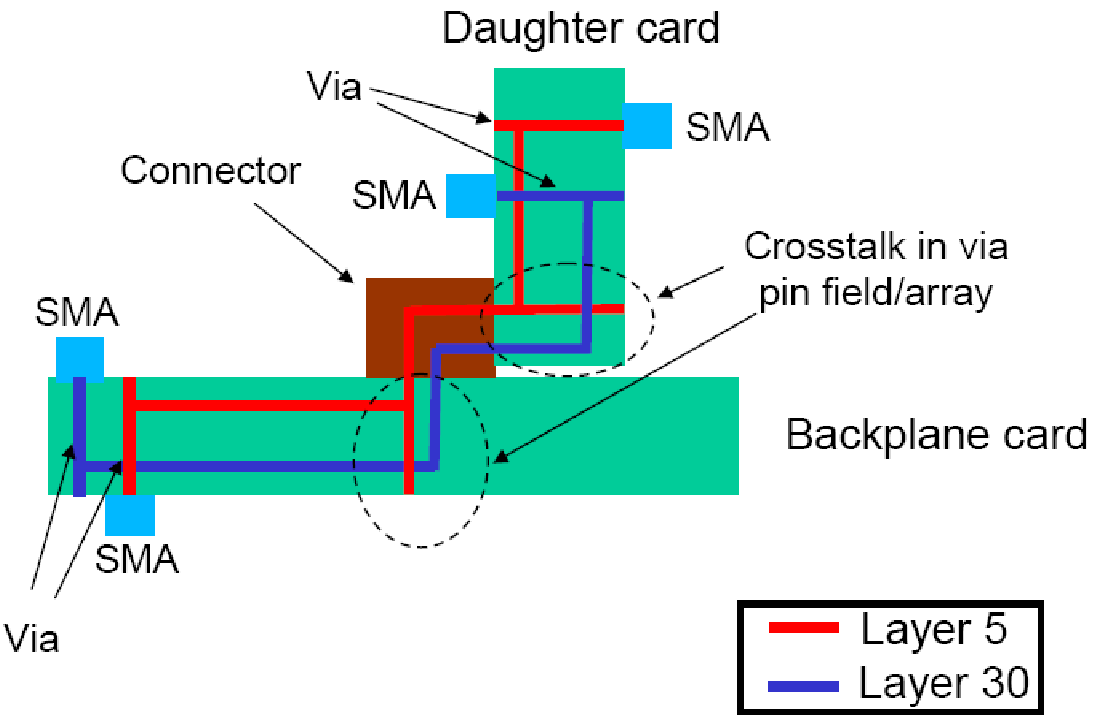


Figure 3.1 Measurement scenario: test signal launching and routing on the daughter card and backplane card. The PCB stack-up contains 34 metal layers with total board thickness of approximately 4.95 mm. The crosstalk is induced in the connector via pin field (footprint) [11].

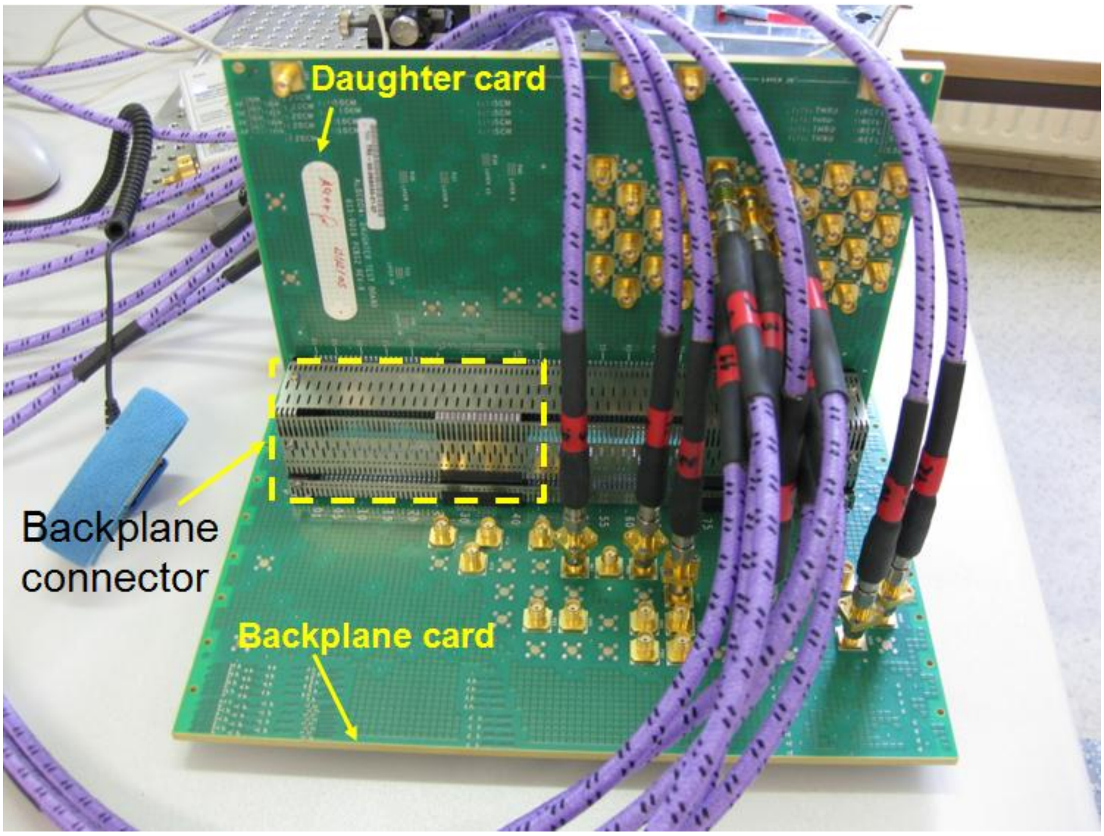


Figure 3.2 Backplane interconnect: daughter card and backplane card with connector receptacle/header and SMA signal launches for crosstalk measurements up to 20 GHz. Test board courtesy of IBM Deutschland Research & Development GmbH [11], [99].

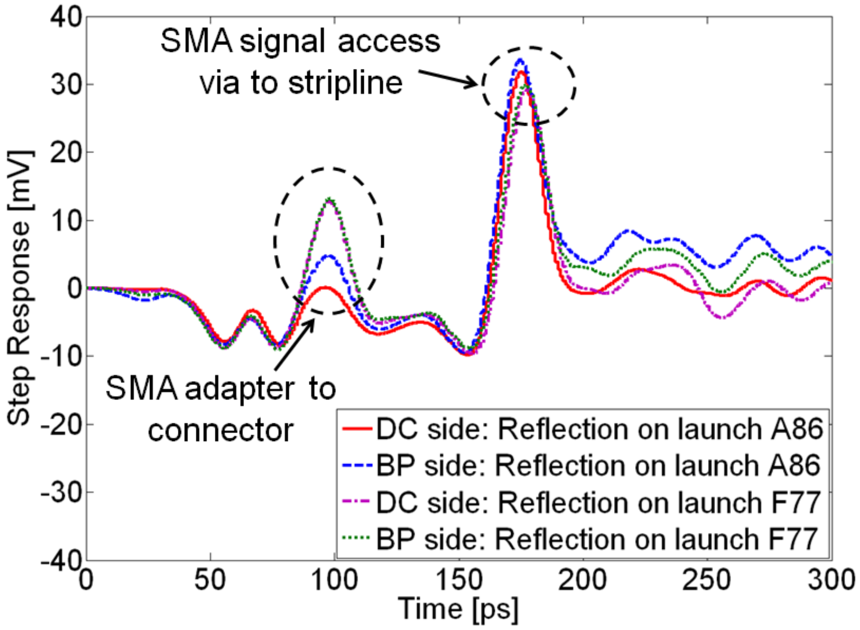


Figure 3.3 Time domain reflection measured on four different SMA launches with a digital sampling oscilloscope (t_r = 12 ps, voltage step = 250 mV). The signal transition between the SMA access via and the stripline represents the largest discontinuity which behaves mainly inductively.

tolerances on the SMA launch design. Based on that the minimum return loss due to the signal launch design variations is expected to be in the range between -17.6 dB up to -18.7 dB. In parallel frequency domain measurements have been performed applying a VNA calibrated up to the cable ends using an ECAL (electronic calibration module). The reflection and transmission characteristics of one digital link on the test board are shown in Figure 3.4.

The expected minimum reflection of the SMA launch (A86) on the daughter card was obtained in the frequency range of 1 GHz and corresponds to approximately -15.4 dB. Similar variations were obtained for the other launches on the test board which is an indicator that the designed SMA launches exceed the -20 dB limit at much lower frequencies than the maximum applicable frequency of the surface mounted SMA connector ($F_{\max} = 18\,\mathrm{GHz}$). Furthermore, the obtained SMA launch variations let one to indicate that calibration or de-embedding of the SMA launches might be very challengeable in order to reduce the effect from the SMA launch on the frequency response of the digital links.

Beside the electrical characteristics the mechanical dimensions of the connectors present another limitation when multiport measurements have to be performed as discussed in Section 2.1. Different high bandwidth connector designs e.g. right angle elbow or vertical access can be found. As shown in the following Section, for investigations in closely spaced via arrays, one prefers to use the connector designs with vertical access in order to ensure suitable simultaneous multiport test signal launching and to utilize as little as possible additional test board space.

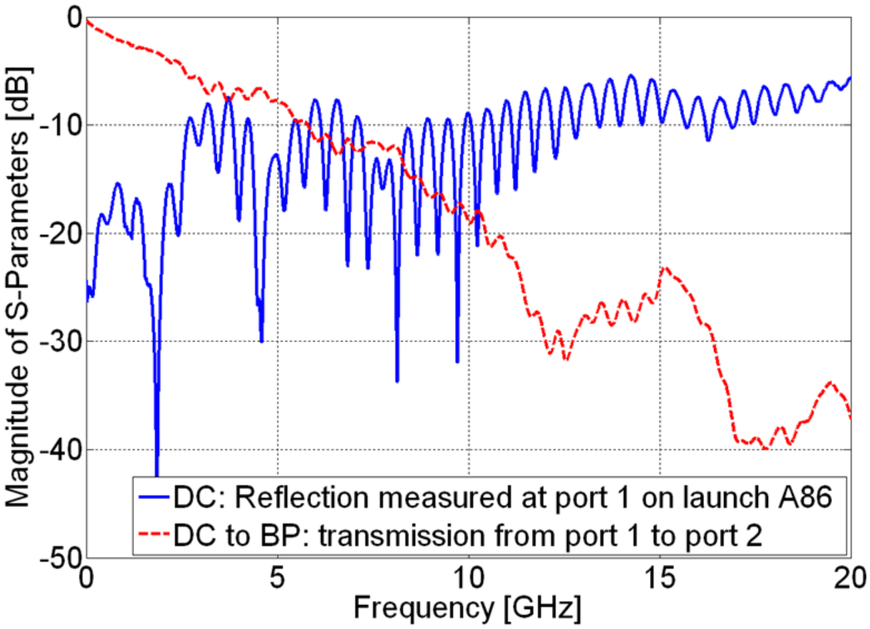


Figure 3.4 Measured S-parameters of the digital link accessed by the SMA launches on the daughter card (DC) and backplane (BP) boards obtained by a VNA calibrated up to the cable ends.

3.2. Crosstalk Analysis in Connector Via Pin Fields

In the next step the crosstalk behavior of a connector via pin field in typical high speed interconnect scenario is investigated in measurements as illustrated in Figure 3.2. Such high speed interconnects with connectors are commonly used in data centers between servers, on backplanes between plug-in cards and between devices on a board. The backplane connectors (connectors for plug-in cards and boards) have to provide enough channel bandwidth for the ever increasing signal data rates. Proper design and optimization of these high speed digital interconnects is a comprehensive challenge which has to deal with the signal degradation issues such as losses, reflection noise, mode conversion and crosstalk.

The backplane connector footprint and its associated card via pattern typically have a major impact on the overall electrical performance of the inter-processor links as shown in [92] - [96]. Crosstalk scaling techniques for the time domain measurements and de-embedding techniques for accurate crosstalk measurements in the frequency domain in a connector via pin field have been presented in [93], [97], [98]. In [11] the crosstalk behavior of a high density via pin field in a connector footprint of a commercial connector embedded in a multilayer printed circuit board (Figure 3.1) was investigated in the frequency domain. The measurements of this high density single ended connector and its associated card via array (Figure 3.2) were performed in the bandwidth from 10 MHz up to 20 GHz applying a 12-port vector network analyzer (VNA). The results from the analysis shown there are summarized in this Section.

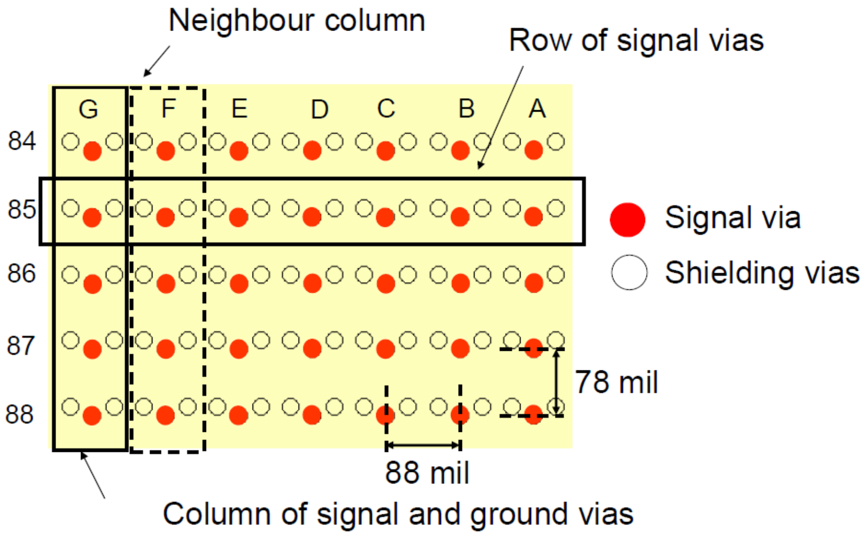


Figure 3.5 Connector footprint definitions. A column contains vias with the same index letter but different number. A row of signal vias has different index letters but the same number [11].

3.2.1. Test Vehicle and Measurement Set Up

The device under test (DUT) used for this study is typical for a high end mainframe processor node to node link scenario consisting of daughter cards plugged into a backplane card by using a multipin connector. The test board was developed by IBM Deutschland Research & Development GmbH [99] and provided for the multiport measurements performed in the frame of this work.

As depicted in (Figure 3.2) the DUT consists of a daughter card, a backplane card with a commercial connector receptacle/header, and SMA (SubMiniature version A) signal launches. The connector via pin field on every test card contains 1400 signal vias and 2800 ground vias, the pitch for signal vias in a row is approximately 88 mils (~ 2.2 mm) wide and in a column 78 mils (~1.98 mm) tall as shown in Figure 3.5. The backplane and daughter card share the same stack-up (34 metal layers, total board thickness ~4.95 mm) but differ in the way that shielding vias (power/ground vias) are connected to the planes (Figure 3.6). All signal vias in the via pin fields are plated through hole vias. The via stub when routing signals to layer 30 is 20.5 mil (~0.52 mm) long and when routing signals to layer 5 is 167.5 mil (~4.2 mm) long. Striplines of ~5.33 inch (~13.54 cm) length provide the access of the test signal from the SMA connectors to the via arrays. Parallel routing of these traces was avoided in order to prevent line to line coupling in the test boards.

The VNA used for the measurements was calibrated up to the cable ends in the frequency bandwidth from 10 MHz up to 20 GHz by using a coaxial SOLT calibration kit. Therefore, the measurement (reference) plane is set to the mating planes of the SMA connectors and the obtained S-parameters contain the response of the long traces to the two via pin fields (on the daughter card and backplane card) and the connector in between.

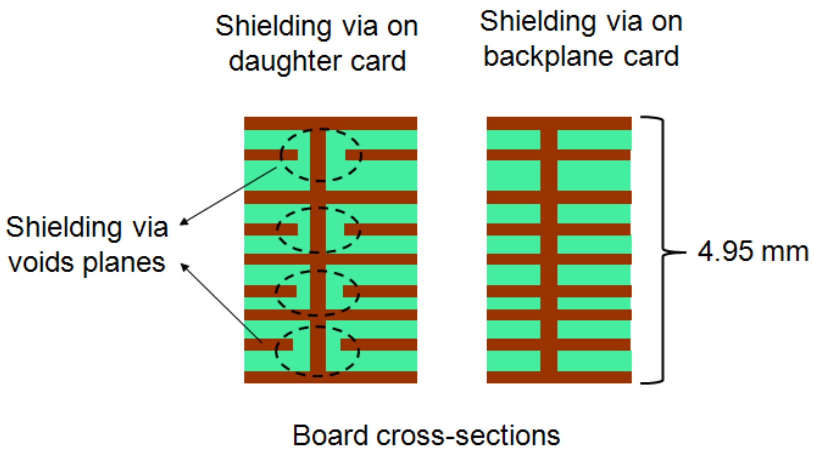


Figure 3.6 Cross-Section of the test boards. Shielding vias on the daughter card are not connected to every ground plane in contrast to the shielding vias on the backplane card. On the daughter card the voided metal planes are intended for power planes [11].

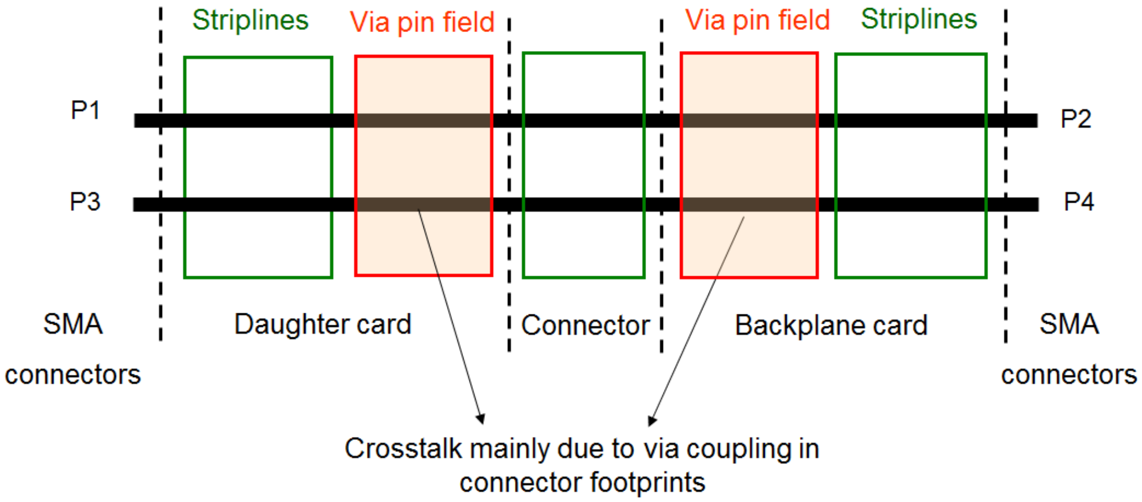


Figure 3.7 Crosstalk measurement of two single ended links: The near-end crosstalk is measured between port 1 and port 3, or port 2 and port 4. The far-end crosstalk is measured between port 1 and port 4 or between port 3 and port 2 [11].

3.2.2. Crosstalk Investigations

In order to extend and complete the crosstalk analysis done in [93], [97] different via array configurations were explored to ascertain the impact of orientation and distance between victim and aggressor via, the common coupled via lengths and the local power/ground environment. For this purpose several adjacent via pin scenarios were studied on the test boards and both near-end crosstalk (crosstalk measured between two ports on the daughter card or two ports on the backplane card, NEXT) and far-end crosstalk (crosstalk measured between aggressor port on the daughter card and victim port on the backplane, or aggressor port on the backplane card and victim port on the daughter card, FEXT) have been explored (Figure 3.7). In particular, the following crosstalk dependencies for single ended links have been investigated:

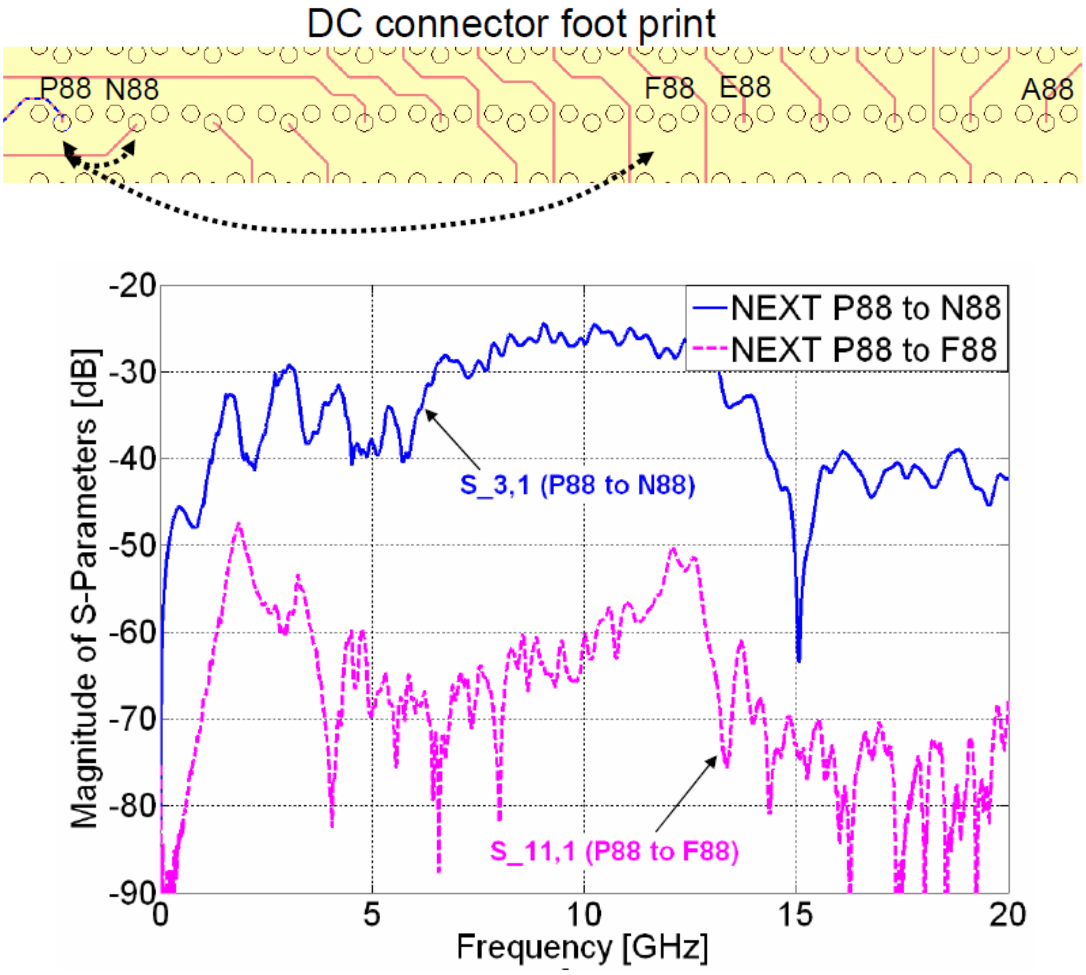


Figure 3.8 Near-end crosstalk dependency on the distance between victim and aggressor via measured on the daughter card. Clearly, a distance dependency is obtained – increasing the distance to the aggressor via (P88) the NEXT reduces [11].

1. Dependency on the distance between victim and aggressor vias.

The near-end crosstalk of vias in a row (Figure 3.5) and its dependency on the distance between aggressor and victim via was explored (pin A88 up to pin P88, Figure 3.8 and Figure 3.9). As expected (Figure 3.8) the near-end crosstalk is reduced as the distance to the aggressor via (P88) increases. The conclusion that via-to-via coupling is dominant (and not the coupling within the connector) can be made from the time domain plot in Figure A.6.15 (Appendix A.6, trace-to-trace coupling within the boards is avoided by careful routing). As shown in Figure A.6.15 when considering two adjacent vias in the time domain the NEXT appears in every via pin field on the daughter card and on the backplane card (two distinct peaks separated by the double delay time of the connector are observed). In the frequency domain, the measurement of the near-end crosstalk contains the overlapped crosstalk present in both via pin fields (Figure 3.7). Similar conclusions were made after Fourier transformation in previous works as shown in [93], [94].

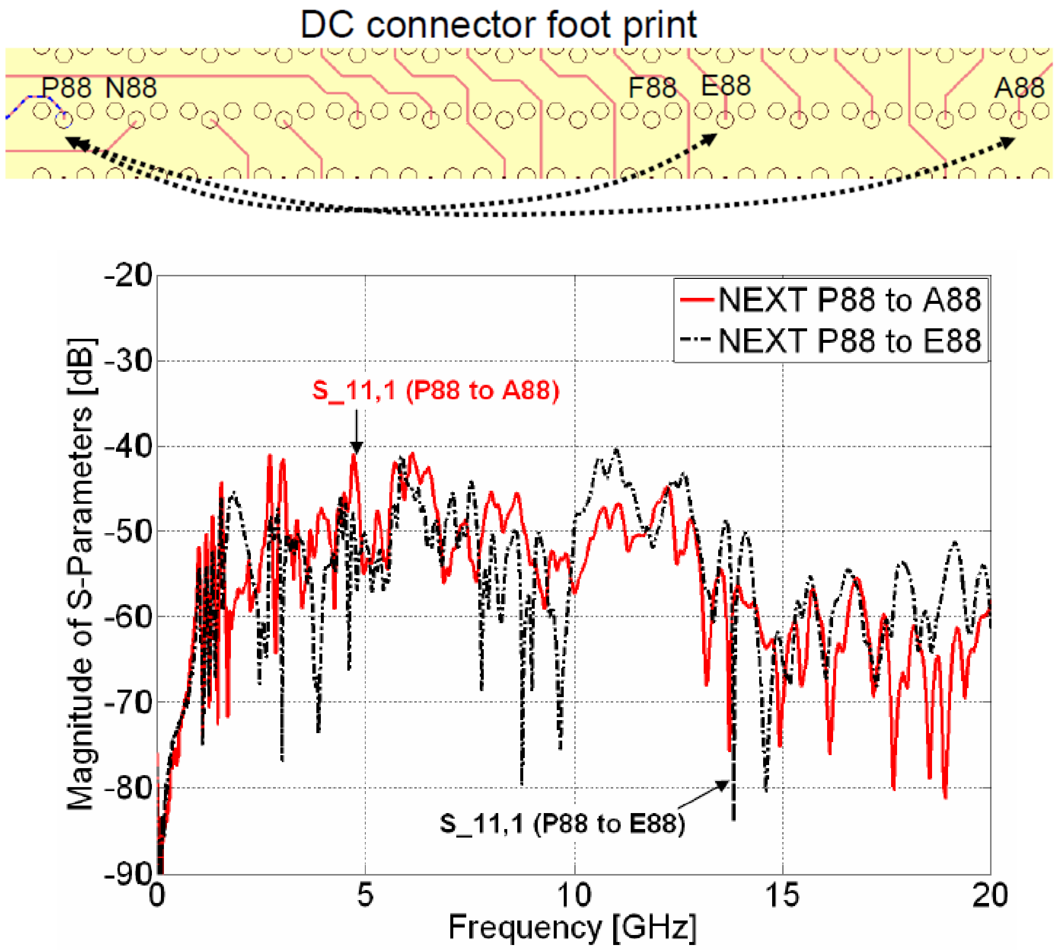


Figure 3.9 Near-end crosstalk dependency on the distance between victim and aggressor via measured on the daughter card. No clear dependency on the distance is obtained when comparing the NEXT between via pair P88 and A88 and via pair P88 and E88 [11].

Furthermore, the time domain analysis shows that the FEXT is mainly inductive. Comparing Figure 3.8 and Figure 3.9 one can see that in a specific case the NEXT (P88 to F88) to a via which is closer to the aggressor is lower than the NEXT (P88 to A88) to a via which is further away with respect to the same aggressor via (P88). As will be discussed later this is due to the fact that the closer victim via (F88) is routing the test signal to signal layer 5 and the other vias (including the aggressor via) route signals to layer 30.

2. Dependency on the orientation.

The analysis of both boards showed that the via-to-via coupling in a row is higher than in a column keeping the same distance to the aggressor via (see Figure A.6.16 in Appendix A.6). This could be due to the fact that the ground vias are ordered differently when looking into different directions with respect to the same aggressor via.

3. Dependency on the coupled via lengths (both through part and stub part).

The effect of the common coupled via lengths on the crosstalk in the connector footprint via array (daughter card and backplane card) was investigated for different scenarios by applying 8-port VNA measurements. As expected when comparing the near-end crosstalk between two long stub vias (both signals routed in layer 5) and the near-end crosstalk of two short stub vias (both signals routed in layer 30) the longer coupled pair induces higher crosstalk (Figure 3.10 and Figure 3.11). The crosstalk dependency on the coupled via length can be better distinguished on the backplane card where the shielding vias are connected to every ground plane (Figure 3.10). Furthermore, it can be seen from Figure 3.12 that in case of via-to-via coupling of a long stub via (via routing signal to layer 5) and a short stub via (via routing signal to layer 30) the near-end crosstalk is higher compared to the case of the two coupled long stub vias (both routing signals to layer 5). Considering the same scenario on the daughter card, the near-end crosstalk between the two coupled long stub vias is higher compared to the via-to-via coupling of the long stub via and short stub via pair (Figure 3.13). A possible reason for this seemingly contradictory behavior is the different power/ground environment.

Another scenario explored was the comparison between coupling of one long stub (routing signal to layer 5) and one short stub (routing signal to layer 30) via and in a pair of two short stub vias (both routing signals to layer 30). Here, the obtained results have shown that the via-to-via coupling of the two short stub vias is higher than the coupling in the pair of the long stub and short stub via (Figure A.6.17 and Figure A.6.18 in the Appendix A.6). Similar to the previous cases, the effect of the different power/ground environments on both card sides can be discerned here due to the fact that the crosstalk between two vias with different stub lengths (a short stub and a long stub) on the daughter card side is higher than the one on the backplane card. Furthermore the results have shown that if the shielding vias are connected to every ground plane as on the backplane card the differences in the via-to-via coupling for the described scenario are less distinctive (Figure A.6.18). Considering the far-end crosstalk (FEXT) on the daughter card (Figure A.6.19, Figure A.6.20 in the Appendix A.6) and on the backplane card one comes to the conclusion that a short stub via on the backplane card induces more FEXT on the daughter card when compared to the FEXT induced from long stub via. The same effect was obtained for the FEXT on the backplane card for this scenario but the FEXT was somewhat smaller – possibly due to the fact that the shielding vias provide more isolation there.

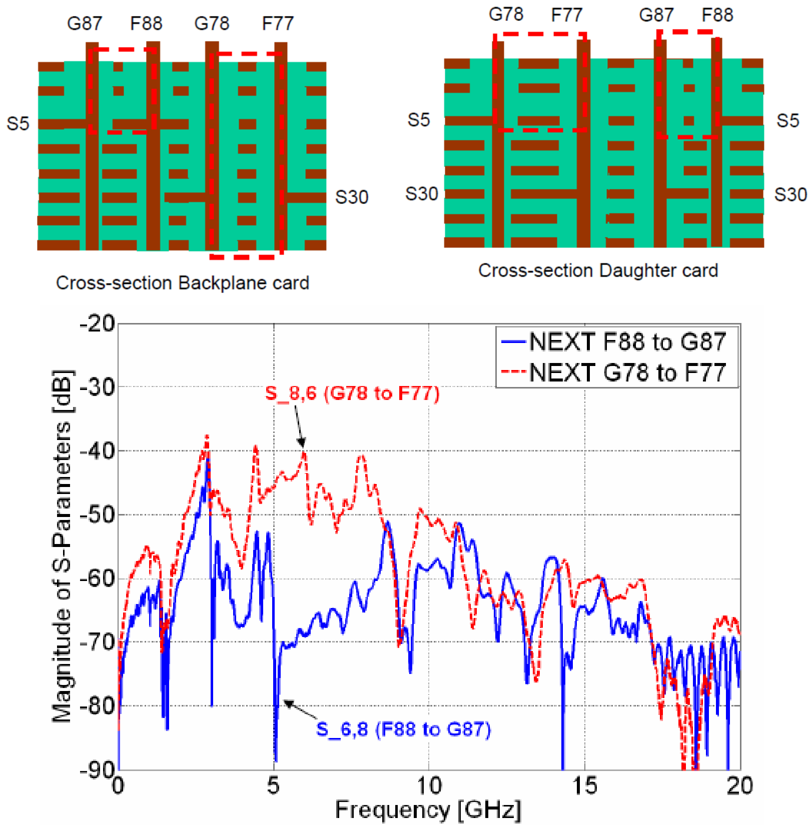


Figure 3.10 Backplane card near-end crosstalk dependency on the common coupled via length [11].

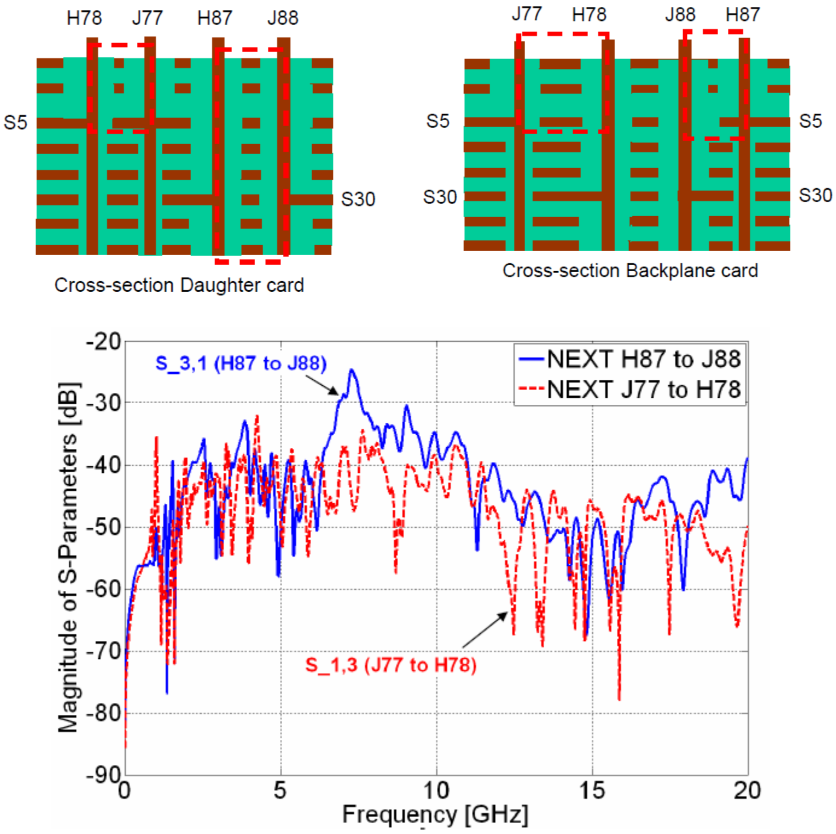


Figure 3.11 Daughter card near-end crosstalk dependency on the common coupled via length [11].

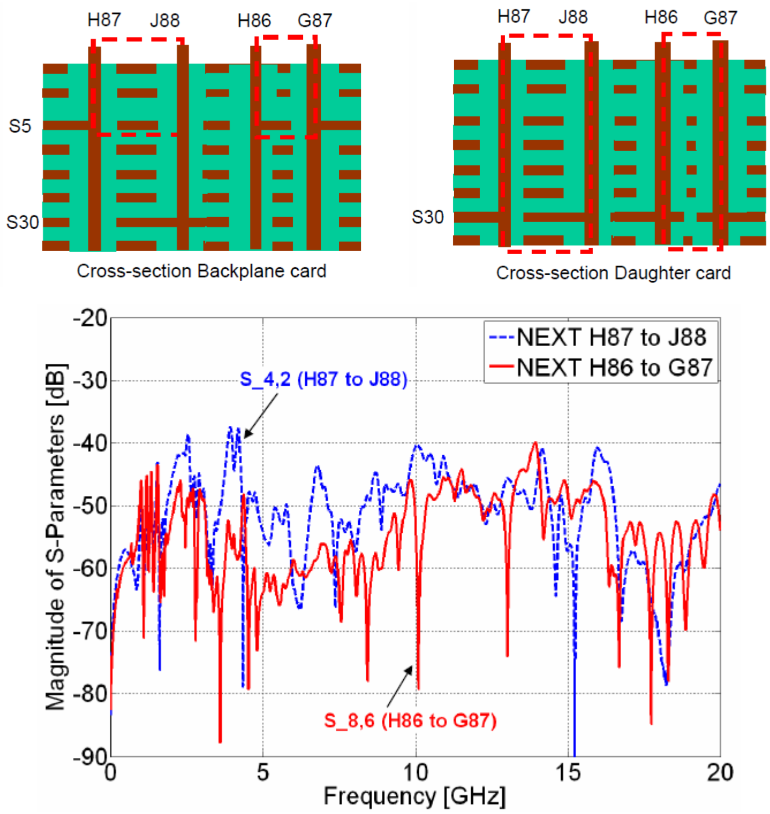


Figure 3.12 Backplane card near-end crosstalk dependency on the common coupled via length [11].

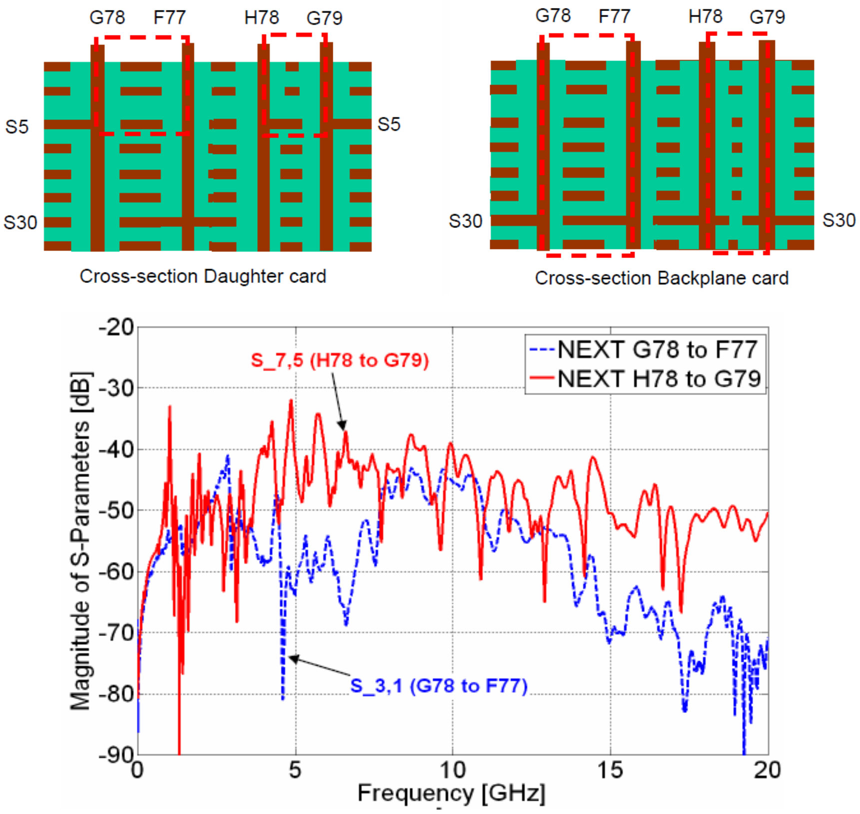


Figure 3.13 Daughter card near-end crosstalk dependency on the common coupled via length [11].

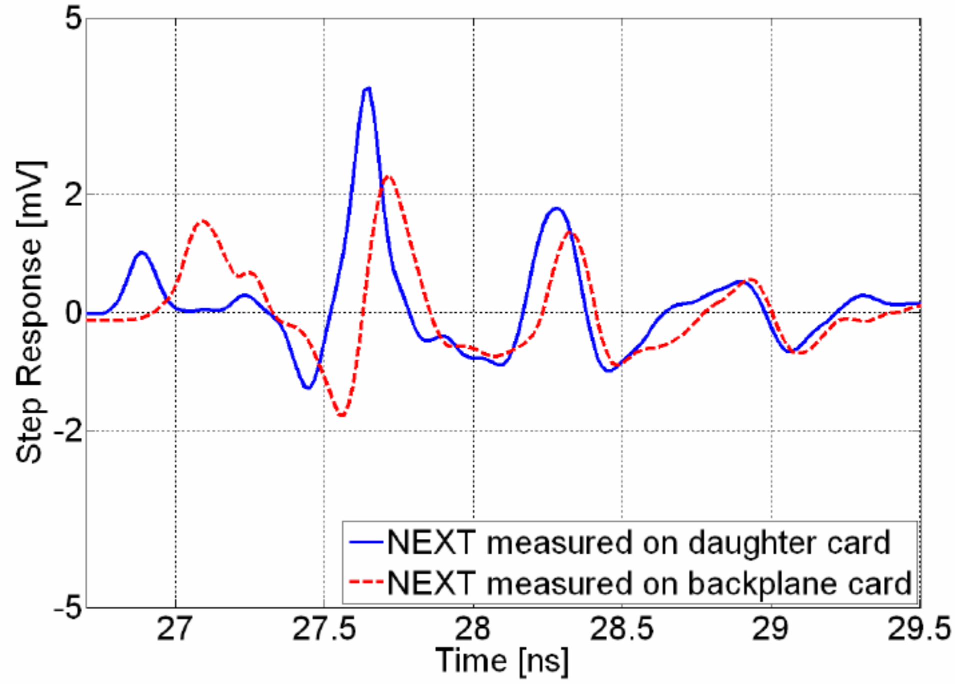


Figure 3.14 Near-end crosstalk of two adjacent vias measured on the daughter card and on the backplane, (1V voltage step, t_r = 67 ps) [11].

4. Dependency on the local power/ground environment (power/ground vias nearby).

The effect of the different power/ground environment on the daughter card (shielding vias void some ground planes, Figure 3.6) and the backplane card (shielding vias are connected to every ground plane, Figure 3.6) can be seen in Figure 3.14. The time domain plot shows that the NEXT measured on the backplane card is lower than the NEXT on the daughter card. Further investigations will show if this effect is only due to the different power/ground environment.

5. Dependency on terminated/unterminated surrounding adjacent vias.

The influence on the crosstalk behavior between two adjacent signal vias when their surrounding signal vias in the connector via field array on the daughter card and backplane card are terminated or left open was explored as well. For this purpose a pair of two coupled long stub vias (both vias routing signals to layer 5) and two coupled short stub vias (both vias routing signals to layer 30) were considered. Here, the crosstalk analysis has shown that the via-to-via coupling is not sensitive to the termination of the surrounding signal vias in both scenarios (Figure A.6.21 and Figure A.6.22 in the Appendix A.6).

3.3. Summary

The time domain analyses of the SMA launches have shown that the –20 dB return loss limit is not maintained for the implemented signal launches in the entire applicable bandwidth of the used SMA surface mounted connector type. A possible explanation for that is the effect of the PCB and connector manufacturing tolerances which were observed in the voltage step response of the SMA signal launches and the associated variations of the amplitudes of the launch discontinuities. In the implemented SMA launch the largest discontinuity is presented by the transition between the access via and the stripline on the signal layer of interest which varies between 33 mV and 29 mV. In order to reduce the effect of the SMA connector launch on the measured S-parameters (expected minimum return loss by the connector approximately -18.7 dB) proper signal launch calibration and/or de-embedding procedures are needed which require adequate matching between the launches implemented on the calibration standards and those on the test vehicle.

Nevertheless, an attempt was made to investigate the crosstalk behavior of a typical backplane connector via pin field assuming that the main crosstalk is basically induced in the connector footprint. Hence, different via coupling scenarios in the connector footprint have been investigated in time and frequency domain. The results from the analysis have shown that the via-to-via coupling in a row signal is higher than in a column. Furthermore the near-end crosstalk in a row of signal vias reduces when the distance to the aggressor via increases. This analysis also identified that the near-end crosstalk in the via pin field is sensitive to the arrangement of the shielding vias which leads to the crosstalk dependency on orientation. The analysis of the effect of different power/ground environment could not be completed with the presented test board – further test will be necessary. However the dependency of the near-end crosstalk on the common via coupled length (via-to-via coupling is highest for a pair of short stub vias) could clearly be shown. No effects on the near-end and far-end crosstalk of two coupled vias could be seen, whether their adjacent surrounding vias are terminated (connected to measurement ports) or left open.

Furthermore, the investigations have shown that the application of the multiport VNA allows to perform measurements in complex dense connector via pin field scenarios with less effort in comparison to the measurement procedure needed using a 2-port VNA e.g. applying port reduction methods [100] - [102].

4. Microprobe Based Measurements

In this Chapter microprobe based measurement techniques for crosstalk study in dense via arrays and for embedded structures (e.g. single/coupled vias, single/coupled striplines, via arrays) in multilayer PCBs are discussed. The application and limitation of one- and two-tier calibration techniques using commercial and custom-made calibration substrates is investigated in order to simplify the double sided probing of via arrays in vertically clamped test boards.

The signal access via stub issue using on-surface probe launches for measurements of embedded structures is explored. Especially the effect of the access via stub on the Thru-Reflect-Line calibration is investigated using multilayer calibration substrates and a self implemented algorithm in Matlab environment. The recessed probe launch technique is briefly reviewed and results from its calibration with help of the TRL algorithm are presented. The obtained results are correlated to 3D full-wave models which are used for the validation and optimization of the RPL.

4.1. Bandwidth of RF Microprobes

RF microprobe manufacturers offer different microprobe configurations suitable for on-wafer, package and PCB board level measurements e.g. [24], [25]. RF microprobes can be classified with respect to the probe tip configuration as single ended, dual- and multi-contact probes (e.g. Ground-Signal-Ground, Ground-Signal-Signal-Ground, mixed-signal RF and DC), the measurement bandwidth (e.g. DC to 110 GHz or only for measurements in a particular bandwidth from 220 GHz to 325 GHz), and the probe inclination with clearance angles of 30° - 45°. Depending on the measurement band the signal launch on the microprobe head can either be a coaxial connector or a waveguide adapter. The applicable probe measurement bandwidth defines the minimum probe pitch (signal-to-ground tip distance) i.e. the higher the measurement bandwidth the smaller the microprobe pitch. According to [25] for $F_{\max} = 50\,\mathrm{GHz}$ the maximum probe pitch corresponds to 500 µm. Alternatively, larger probe pitches can be found e.g. [24] where probes with a signal pitch of 1250 µm are offered for $F_{\max} = 50\,\mathrm{GHz}$. The application of large probe pitches might not be preferable due to the fact that in case of insufficient calibration the residual calibration error induced by the probe loop inductance is larger.

Microprobes are typically mounted in commercial micropositioners which allow manual or automated probe positioning. For measurements on PCBs manual probe positioning is more common due to the fact that test structures and signal launches are irregularly distributed. The clamping and measurement of such test structures using on-wafer probing stations might be very challenging. Furthermore, bad planarity of the PCB surface hampers additionally the automated probing.

4.2. Measurement Techniques for Crosstalk Study in Via Arrays

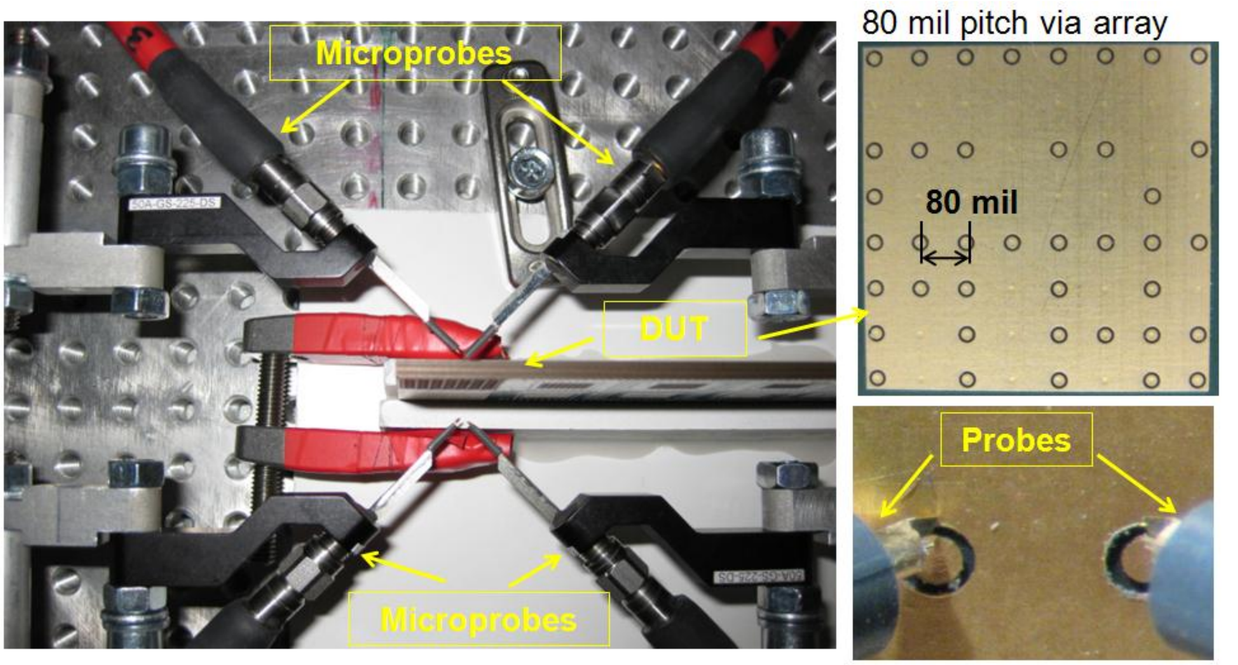
When performing high frequency measurements it is often impossible to directly measure the device under test (DUT). Instead, measurements are made at, and referred to, some reference plane physically removed from the device defined by the particular calibration technique used. When the characteristics (S-parameters) of the fixture (e.g. adapters, microprobes, dedicated launches and etc.) used for launching the test signal into the device under test are known, they can be extracted from the measured data through the use of de-embedding [103].

In this Section, measurement and de-embedding techniques used to investigate crosstalk in via arrays using broadband microprobes and a multiport vector network analyzer are presented. These techniques are based on the desegmentation method suggested in [105] - [107] which dispenses with T-matrices and directly utilizes the S-parameter or Z-parameter matrices of the multiport network that has to be de-embedded. In [10] this method was applied to microprobe based crosstalk measurements in dense via array structure in the frequency range from 10 MHz up to 50 GHz. There, the error boxes of the microprobes were first obtained by the use of a two-tier calibration technique (Appendix A.3). In the next step, desegmentation was used to remove their detrimental effect on the measurement data (Appendix A.4).

In the following Section, the two-tier calibration method and the suggested de-embedding technique are applied to microprobe based measurements of dense via arrays on a multilayer printed circuit board (PCB) and the obtained results are correlated to a nominal measurement procedure. The measurement procedure and obtained results can be found in publications [17] and [18].

4.2.1. Measurements Using Two-tier Calibration

The measurement set up used for the crosstalk investigations of the dense via array (80 mil pitch) is depicted in Figure 4.1. To enable simultaneous probing of the vias in the array from the top and bottom sides, the PCB has been clamped vertically and the probes moved horizontally to examine the vias of interest. As illustrated, the DUT



4-port probe based measurement set-up

Probes connected to adjacent vias

Figure 4.1 4-port via array measurement set up. The via array is positioned vertically, microprobes are moved horizontally for connecting the vias from the top and bottom of the PCB. The measured scattering parameters contain the via array and the four microprobes [12].

represents an 8 by 8 via matrix (40 through vias and 24 ground vias) placed on an 80 mil grid implemented on a multilayer PCB. The board stack-up contains 18 metal layers (6 signal and 12 potential ground planes) and uses Nelco-13 4000 ($\varepsilon_r = 3.7$, $\tan\delta = 0.008$, [104]) as dielectric. The total board thickness measures approximately 105.2 mil (Figure 4.2).

It is important to note that for this scenario the calibration of the microprobes becomes very difficult if they have to be de-embedded from the measurement of the test device. As shown in Figure 4.1, four microprobes (GS and SG probe tips) are used for the crosstalk investigations of the via array. The reason for choosing this measurement set up is that it enables close-up measurement of the via-to-via coupling between every two vias when connecting the vias from the bottom and the top of the PCB. Connecting the vias in this way ensures that the measured crosstalk between adjacent vias is mainly due to the via-to-via coupling and less due to multiple reflections in case of open via ends (using only two ports for crosstalk investigation).

In Figure 4.3 the two-tier calibration procedure is presented that was used for the measurements in order to simplify the measurement effort needed for obtaining of the S-parameter of via pairs in the array. For this purpose the desegmentation method was applied to de-embed the microprobes from the S-parameters of the measured vias. Two-port scattering parameters (error boxes) for the microprobes were extracted with help

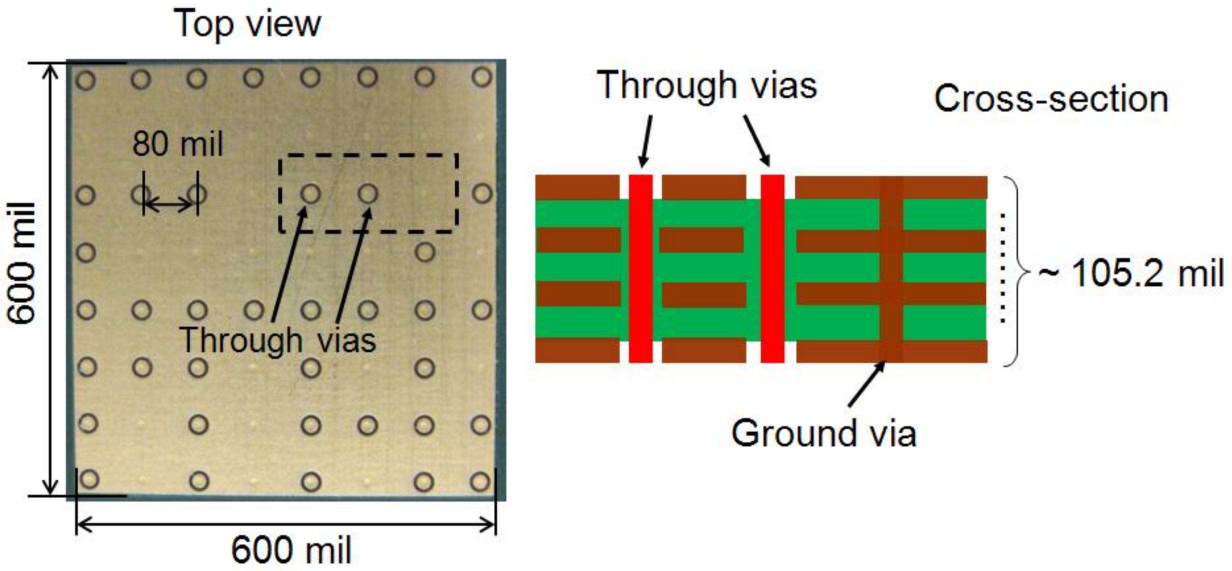


Figure 4.2 Test structure (via array) containing altogether 64 vias (40 through and 24 ground vias). The through vias can be accessed from the top and the bottom, whereas ground vias connect all metal layers [12].

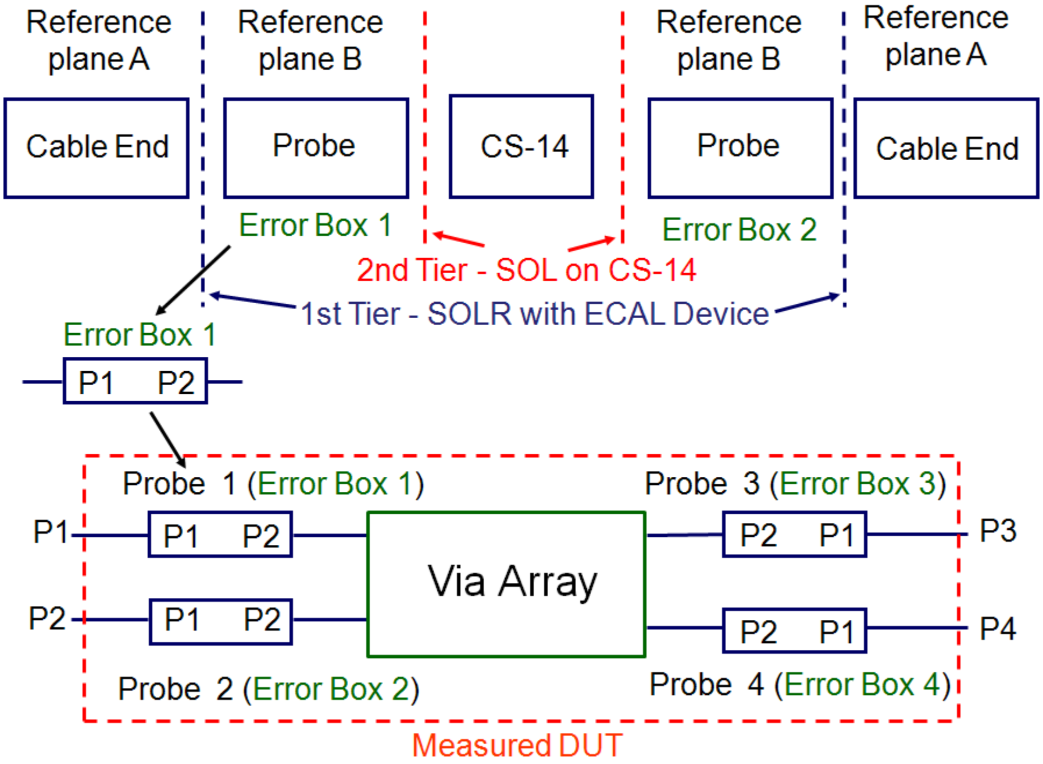


Figure 4.3 Connectivity of error boxes for the microprobes obtained from two-tier calibration. The second tier is used for the extraction of error boxes that represent the change in the system between the first and second calibrations due to the microprobes. The probe error boxes can be then extracted sequentially from the measurement data using desegmentation [10].

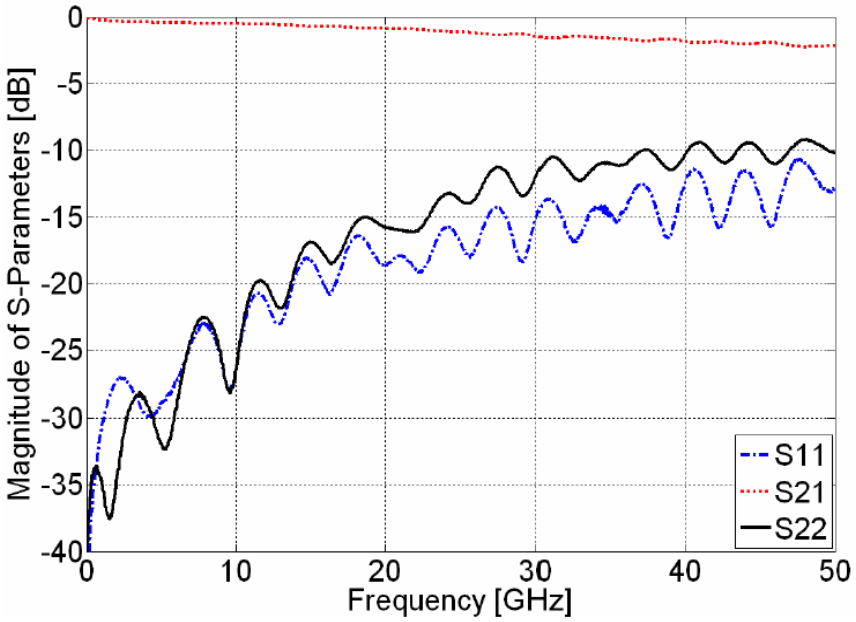


Figure 4.4 Error parameters (S-parameters) of one SG microprobe extracted with the calibration standard CS-14 and the SOL calibration algorithm. Similar parameters can be found in the data sheet of every microprobe [10].

of the two-tier calibration method illustrated there. As depicted for the 1st tier the 4-port VNA was calibrated in the bandwidth between 10 MHz and 50 GHz using a 2-port electronic calibration device and a coaxial SOLR calibration. Using a 2nd tier SOL calibration similar to that in [7], the reference plane was shifted to the microprobe tips which enabled the calculation of the error boxes of the microprobes themselves (Figure 4.4). The calibration standards used for the 2nd tier are available on the CS-14 substrate (Al_2O_3, $\varepsilon_r = 9.8$) from GGB Industries [24].

Performing direct microprobe calibration on CS-14 ([24]) is an alternative method used for comparison to the obtained results later on. It is obvious that due to the specific vertical measurement set up the probe calibration requires either to mount the calibration substrate vertically in order to use the probe vendor substrate or to mount the probes and calibration substrate horizontally. The calibration in vertical position might be very inconvenient if a thru standard has to be measured between two opposite ports.

In [12] custom multilayer calibration substrates were presented which enable the microprobe calibration in the presented measurement scenario when the probes are mounted horizontally. For this purpose, a calibration substrate containing short, open and load terminations was designed on a multilayer PCB. As shown in Figure 4.5, 47 Ohm resistors (SMD, 0402, 1 %) have been soldered at the end of the access via on the bottom board side for the load termination. In case of the shorts, the loads are replaced with solder bridges and for the opens the vias are simply left open. The calibration

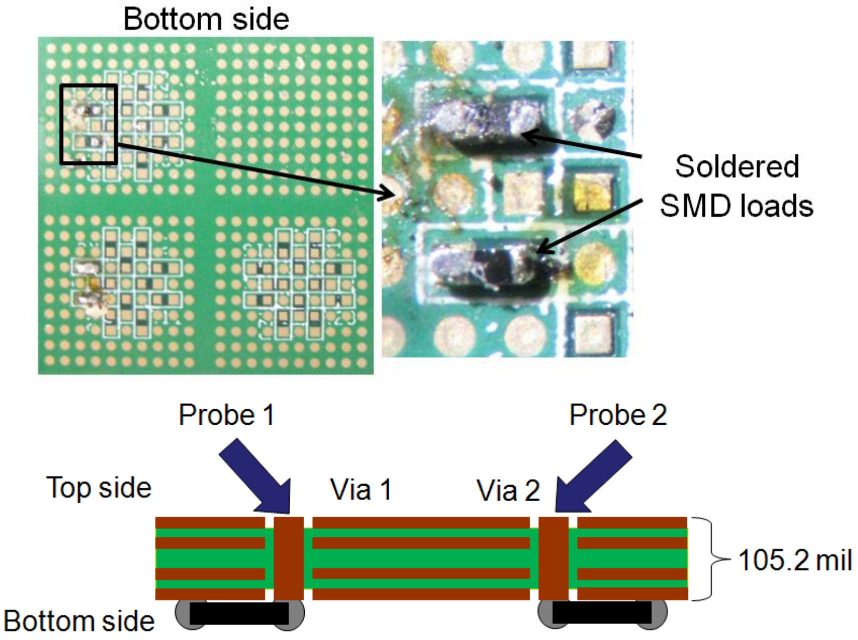


Figure 4.5 Custom-made microprobe multilayer calibration substrates: SMD resistors (47 Ohm, 0402, 1 %) represent the load terminations, solder bridges are used for the short terminations and unterminated vias are used for the open terminations [12].

standards and the via array test structures share the same multilayer stack-up and the dimensions of the through and ground vias in the via arrays are the same in order to achieve maximum calibration bandwidth. Unfortunately, the handmade soldering is an important factor which contributes to the imperfection of the terminations, as the parasitic effects of the soldering joints limit the maximum applicable calibration bandwidth.

In order to investigate the maximum applicable bandwidth of the designed custom-made standards and the limitations of the measurement techniques for extraction and de-embedding of probe error boxes, via array measurements using a VNA were performed. For these measurements, microprobes from Picoprobe Model 40A DS-style GS- and SG-225 µm pitch were applied to the four measurement ports of a multiport VNA. The frequency limits of the custom-made standards were explored using the two-tier methods shown. The obtained results were compared to conventional one- and two-tier calibration methods applying vendor calibration substrates. The following calibration procedures were applied:

- one-tier SOLT calibration using the microprobe vendor calibration substrate available on the CS-14 substrate (Al_2O_3, $\varepsilon_r = 9.8$) from GGB Industries [24],
- two-tier calibration using an electronic coaxial calibration module (ECAL) for the 1st tier and an SOL calibration for the 2nd tier performed for every microprobe using the standards on CS-14 (Figure 4.3).

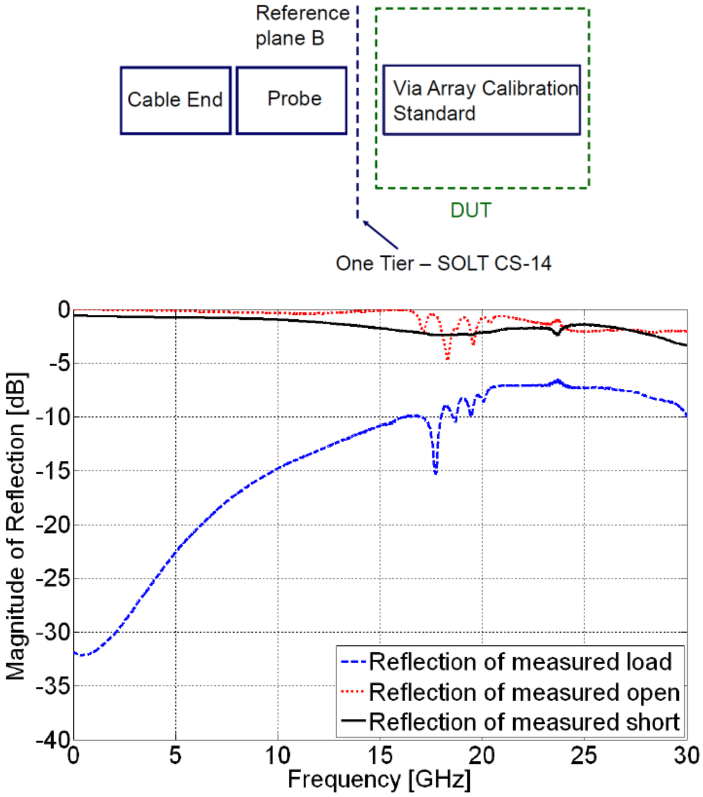


Figure 4.6 Measurement procedure used for obtaining the S-parameters of short, open, and load standards. The effect of the cables and the probes is removed by the calibration up to the probe tips using the microprobe vendor calibration substrate; Measured load, open and short standards on the multilayer substrate obtained after one tier SOLT microprobe calibration on CS-14 [12].

Furthermore, the custom-made substrates were applied in a mixed method as follows. A two-tier calibration was performed with an ECAL module for the 1st tier. Then the custom-made SOL terminations were measured with uncalibrated probes. After that, a 2nd tier SOLT probe tip calibration on the CS-14 substrate was performed and the custom-made standards were measured again using the calibrated probes (Figure 4.6 - Figure 4.11).

From Figure 4.7 one can see that in the range of 30 GHz the measured phases of three terminations are close to each other and thus the SOL calibration algorithm could fail at frequencies higher than 30 GHz. Furthermore, the Smith-chart in Figure 4.8 shows that the load and open terminations are not well separated in the range of 31 GHz, i.e. the prerequisite for the SOL calibration algorithm is no longer met. In order to determine the reliability of the custom-made calibration standards S-parameters (error parameters) of the microprobes were extracted using the commercial calibration standard CS-14 for the second calibration tier (SOL calibration). The comparison of the extracted probe S-parameters shown in Figure 4.9 and Figure 4.10 indicates that the probe error boxes obtained from the different two-tier calibration methods correlate well to each other in the frequency bandwidth up to 30 GHz.

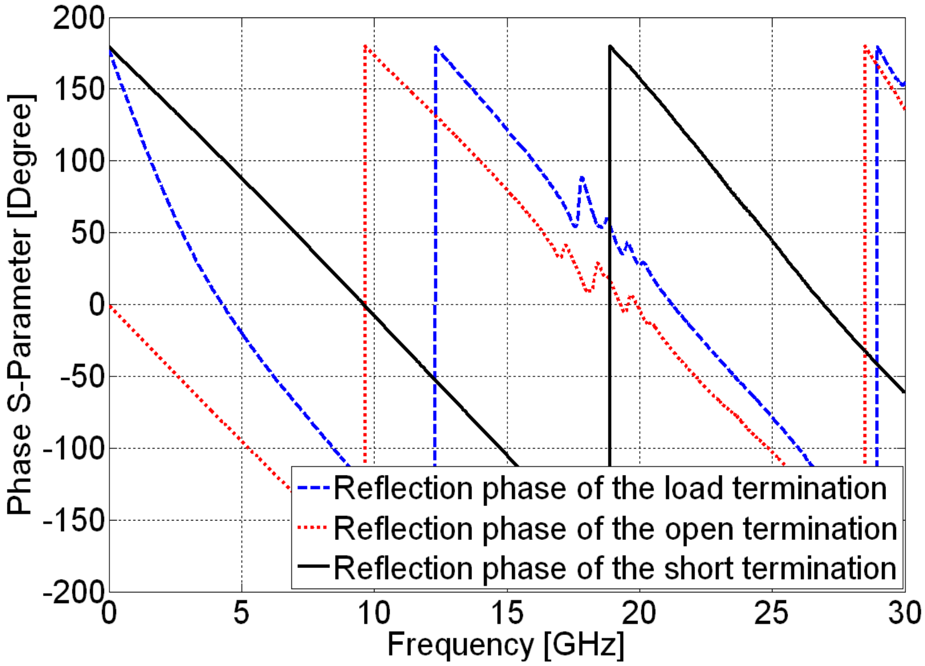


Figure 4.7 Phase of the measured reflections of the load, open and short standards on the multilayer substrate obtained after one-tier SOLT microprobe calibration on CS-14 [12].

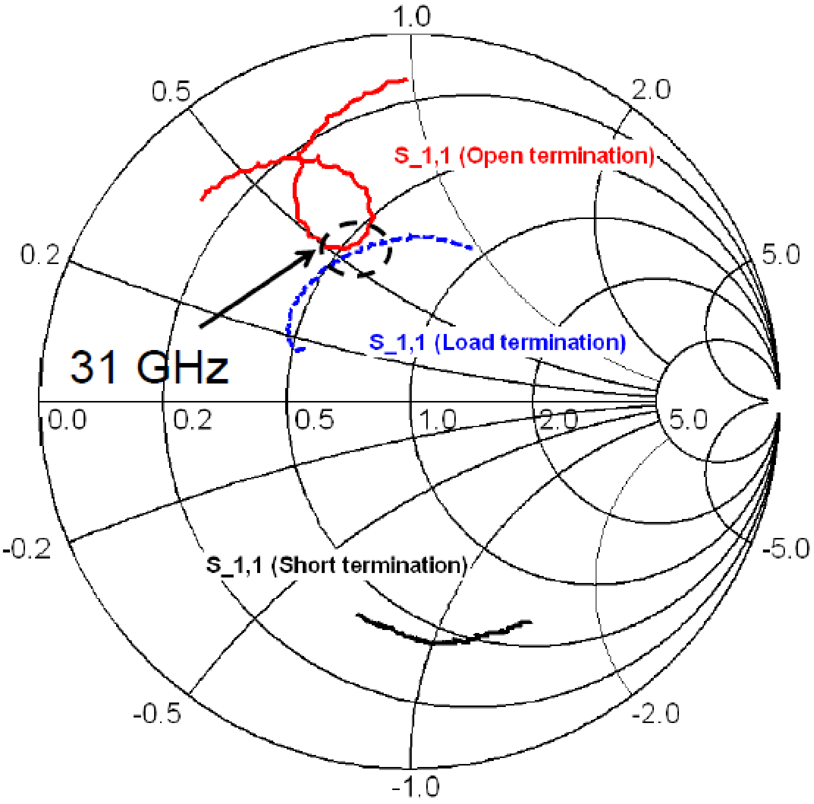


Figure 4.8 Smith-chart plot of the custom-made substrates (30 GHz- 32 GHz). In the range of 31 GHz insufficient separation of the open and load terminations is noted [12].

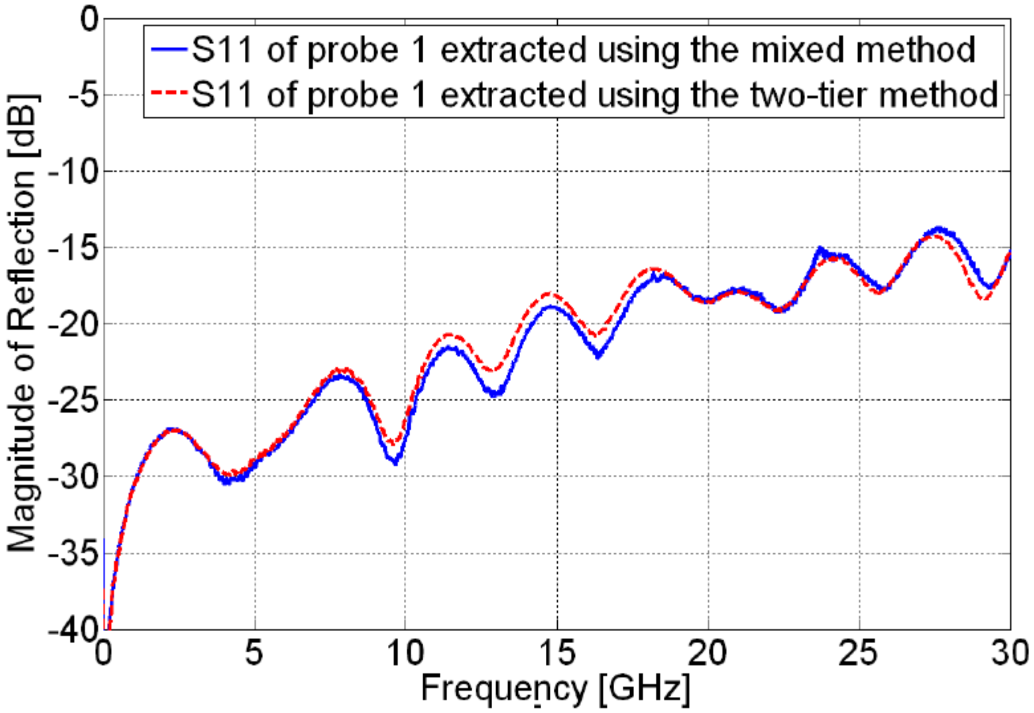


Figure 4.9 Reflection comparison of the extracted error boxes of one microprobe applying the two-tier and mixed calibration methods [12].

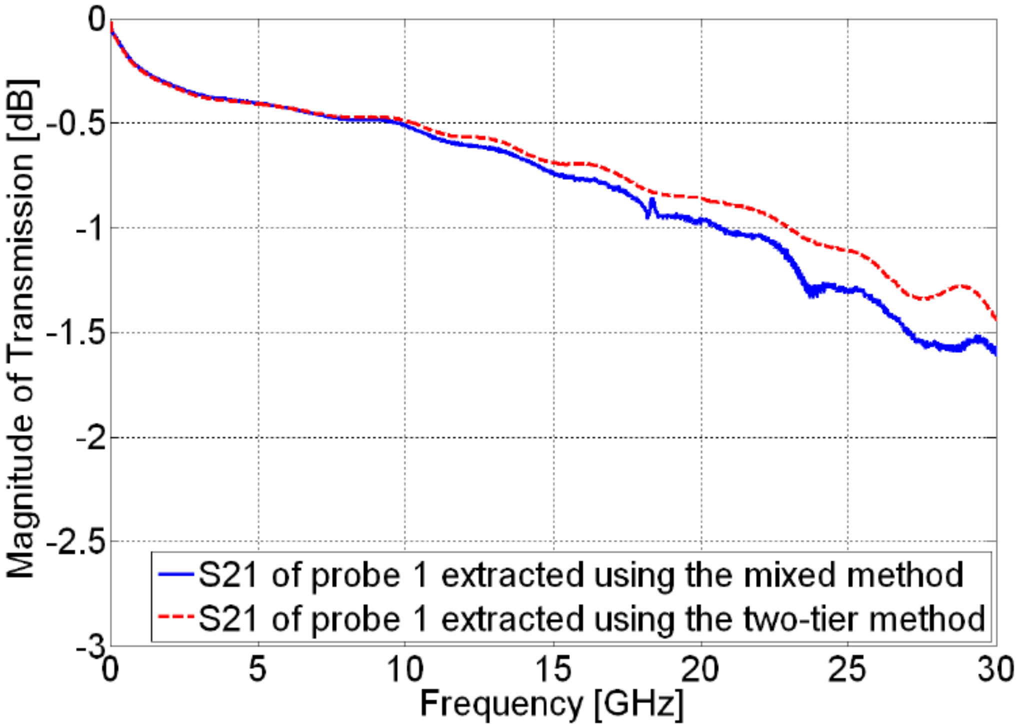


Figure 4.10 Transmission comparison of the extracted error boxes of one microprobe applying the mixed and two-tier calibration methods [12].

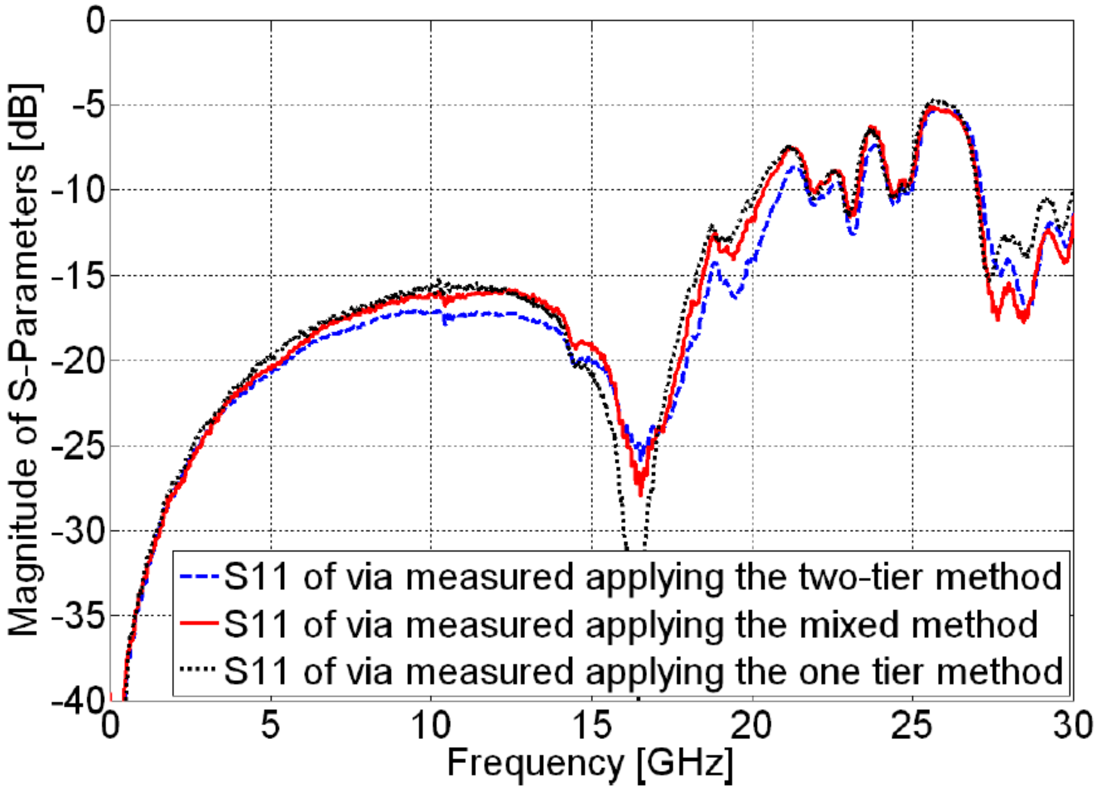


Figure 4.11 Comparison of the measured reflection of one via in the via array obtained by applying the different methods: one-tier SOLT, two-tier and mixed methods [12].

In the measurement set up depicted in Figure 4.1 a lot of effort is necessary for the microprobe calibration and additionally their horizontal positioning. The procedure using the custom-made termination substrates provides the most flexibility if the following steps are followed (Figure 4.12). In order to perform the via array measurements, the probes can be mounted in horizontal position after performing the coaxial ECAL device calibration and then the SOL multilayer substrates measured clamped vertically instead of the test board (Figure 4.5). Additionally, the device under test is measured using the same measurement set up and clamping with the uncalibrated microprobes. In the next step, the microprobes can be de-embedded by desegmentation from the DUT measurements using their extracted error boxes obtained from the two tier calibration method (Figure 4.3). In order to extract the probe error boxes, the VNA has to be calibrated up to the microprobe tips. The probes are mounted horizontally for the SOLT calibration on CS-14 and for the additional measurement of the custom-made terminations with the calibrated microprobes (Figure 4.6).

The comparison of the different methods (Figure 4.11, Figure A.7.23 in the Appendix A.7) reveals good correlation of the obtained S-parameters for the same via arrays (80 mil grid) in the bandwidth from 10 MHz up to 30 GHz. This proves again that the

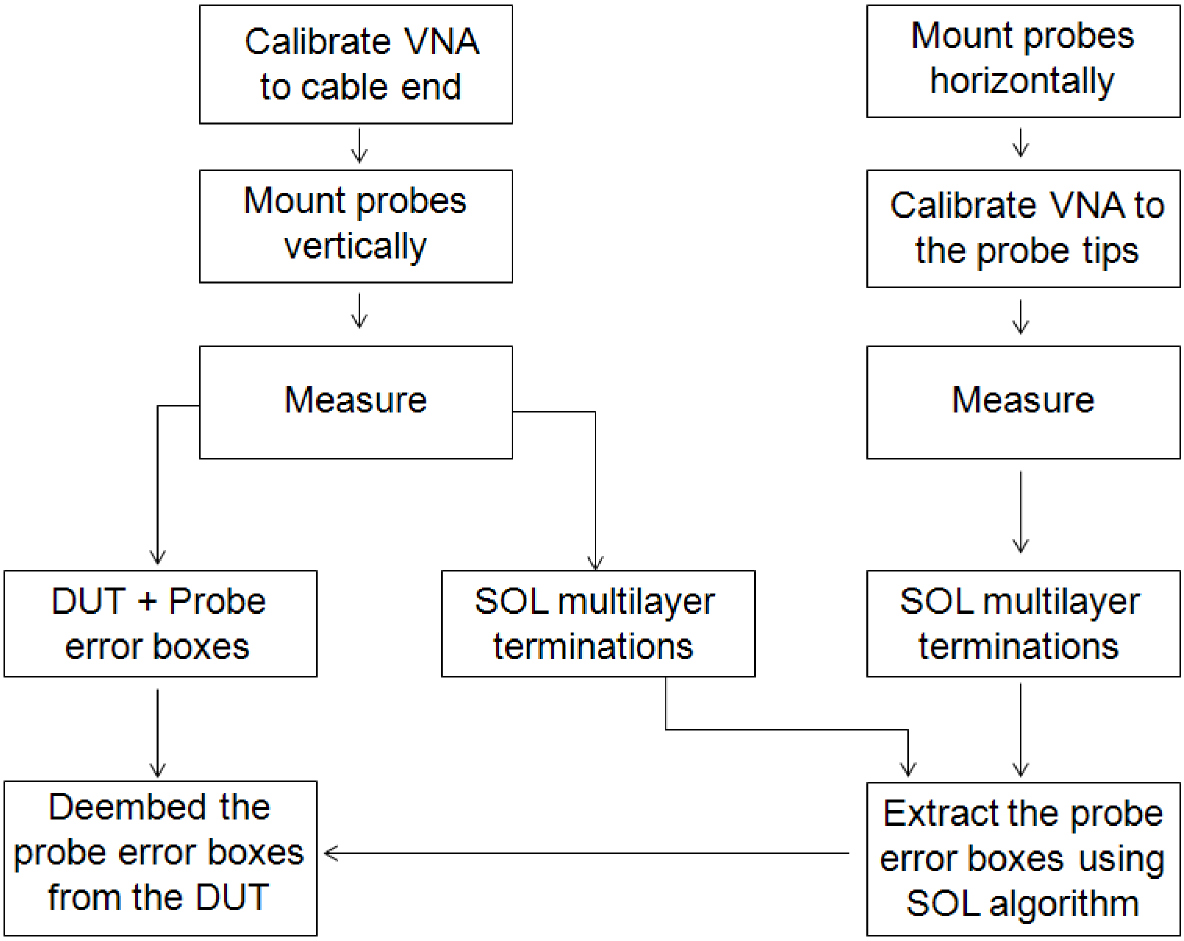


Figure 4.12 Measurement and calibration procedure for the application of the mixed calibration method.

custom-made non-ideal substrates can be applied in the frequency range up to 30 GHz. Furthermore, the custom-made substrates are indeed more flexible for microprobe calibrations (two-tier) for via array measurements where complex mechanical clamping is needed.

4.2.2. Measurements Using One-tier Calibration

In the following the validity of the microprobe measured data obtained by a one-tier SOLT calibration on the alumina substrate CS-14 is investigated using a full-wave model of the via array shown in Figure 4.2. The one-tier calibration procedure is a common one for microprobe based measurements and, furthermore, it was chosen for this analysis because of the fact that errors due to reconnection of the cables to the microprobes (two-tier method) and inaccuracies arising from extraction of their error parameters requiring an additional measurement (mixed method) were avoided.

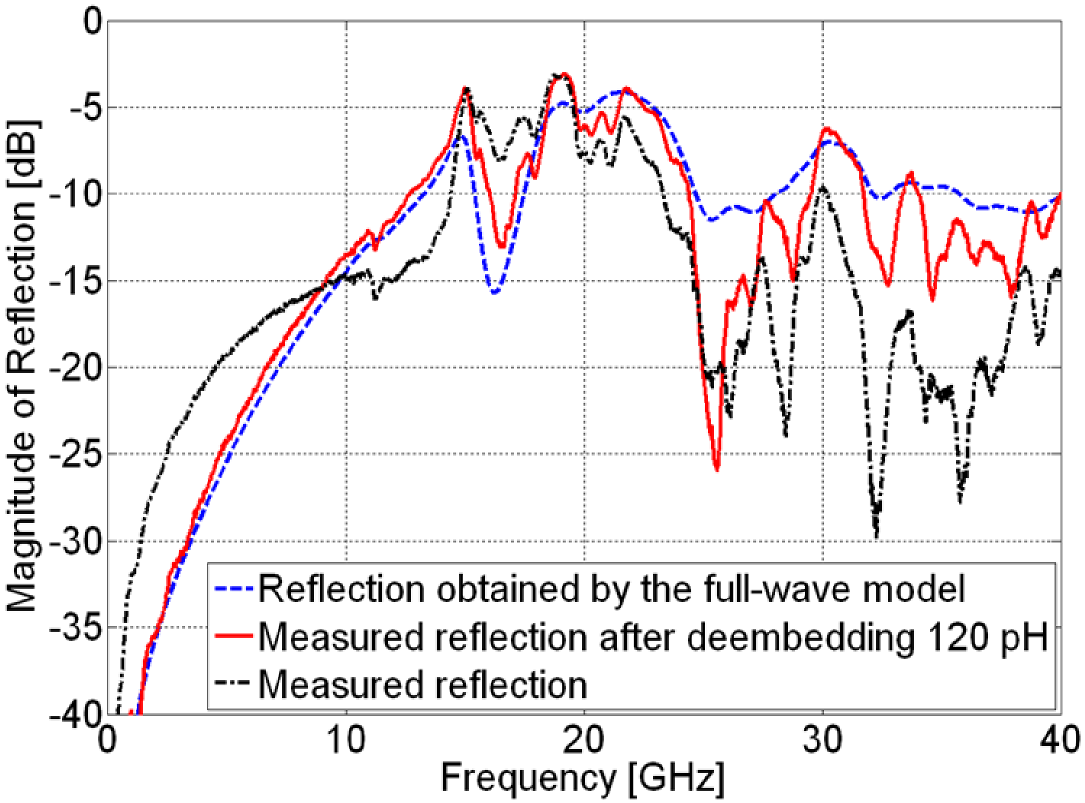


Figure 4.13 Model-to-hardware correlation of measured reflection parameters by de-embedding of the residual parasitics of calibrated GS-probe (120 pH). Good correlation is obtained for the overall bandwidth up to 40 GHz. The resonances in the measured data cannot be captured by the full-wave model [18].

For modeling purposes, the signal vias were excited by lumped ports at their via pads on their top and bottom side in order to reproduce the measurement set up for the vertical via array measurements (Figure 4.2). As depicted in Figure 4.13 and Figure 4.14, the correlation of the measured and computed S-parameters was improved after de-embedding of a serial inductance of 120 pH from every measurement port. This value was derived from previous investigations where it was found out that the residual probe parasitics of GS-probe tip configurations, which were calibrated prior to that on alumina calibration substrate CS-14 (Al_2O_3, $\varepsilon_r = 9.8$) and not on the PCB dielectric substrate, correspond to approximately 120 pH [108]. Apparently, resonances beyond 25 GHz observed in the measured reflection and transmission parameters could not be captured by those obtained from the full-wave model.

Here, it is important to note that the probe-to-probe coupling which was not taken into account in the applied calibration algorithm might contribute to this deviation in the bandwidth beyond 25 GHz. Further possible error sources are represented by the differences between the “real” and the simulated DUT geometry e.g. differences due to manufacturing tolerances, and the influence of other adjacent via array structures.

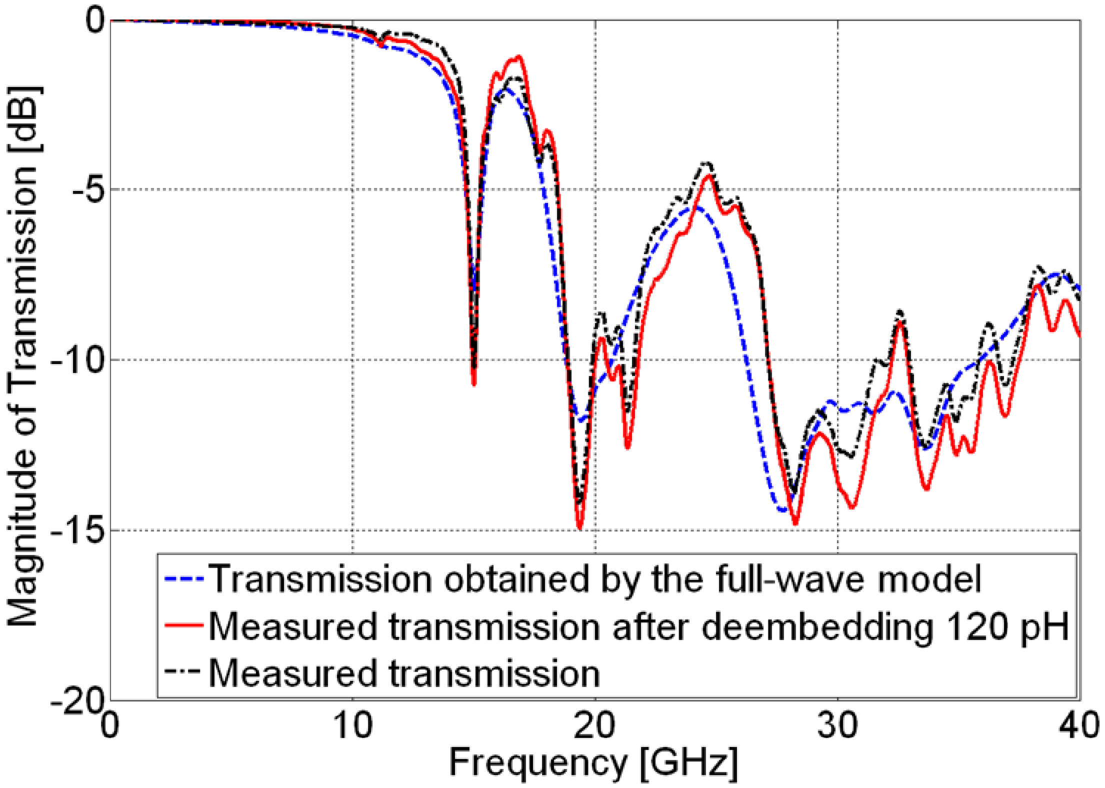


Figure 4.14 Model-to-hardware correlation of measured transmission parameters by de-embedding of the residual parasitics of calibrated GS-probe (120 pH). Again, the resonances in the measured data cannot be reproduced by the full-wave model [18].

Similar model-to-hardware correlation was obtained for the other measurement ports, and for the near-end and far-end crosstalk S-parameters as shown in [17].

4.3. Challenges of Surface Probe Launches

In order to motivate the use of recessed probe launch (RPL) technique in this Section, the effects of PCB manufacturing tolerances (e.g. ±10 % for line impedances) on signal launches for measurement of embedded structures are studied with the help of full-wave models. In the following, the behavior of a surface probe launch is investigated with respect to variations of the access via stub backdrilling depth and the access via antipad radius (Figure 4.15).

In Figure 4.15 the comparison of S-parameters obtained by full-wave simulations of a single turning via (a via which routes signals from one internal signal layer to another) using a surface (cascading Model B + Model A + Model B denoted B-A-B and D-A-D, the latter using backdrilling) and RPL signal launches (C-A-C) is presented. The turning via was additionally simulated using waveguide port excitations to obtain the expected S-parameters from the test device without the influence of both types of signal launches (Model A only). The RPL technique will be described in greater detail in Section 4.5.

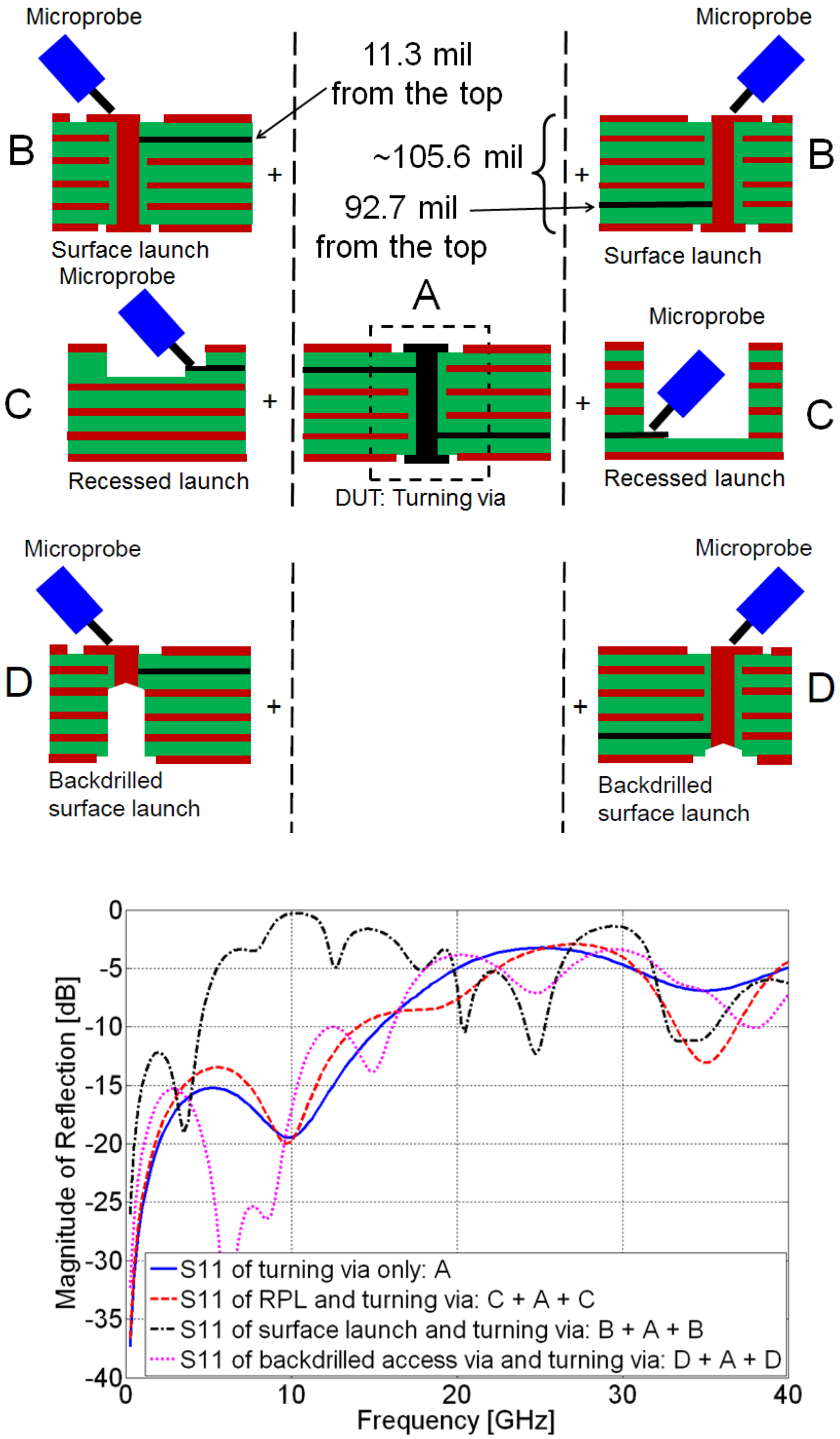


Figure 4.15 S-parameters computed from full-wave models [113]: Comparison of signal launch contributions to the response of a turning via. The S-parameters obtained by the recessed launch correlate best to that from the turning via only.

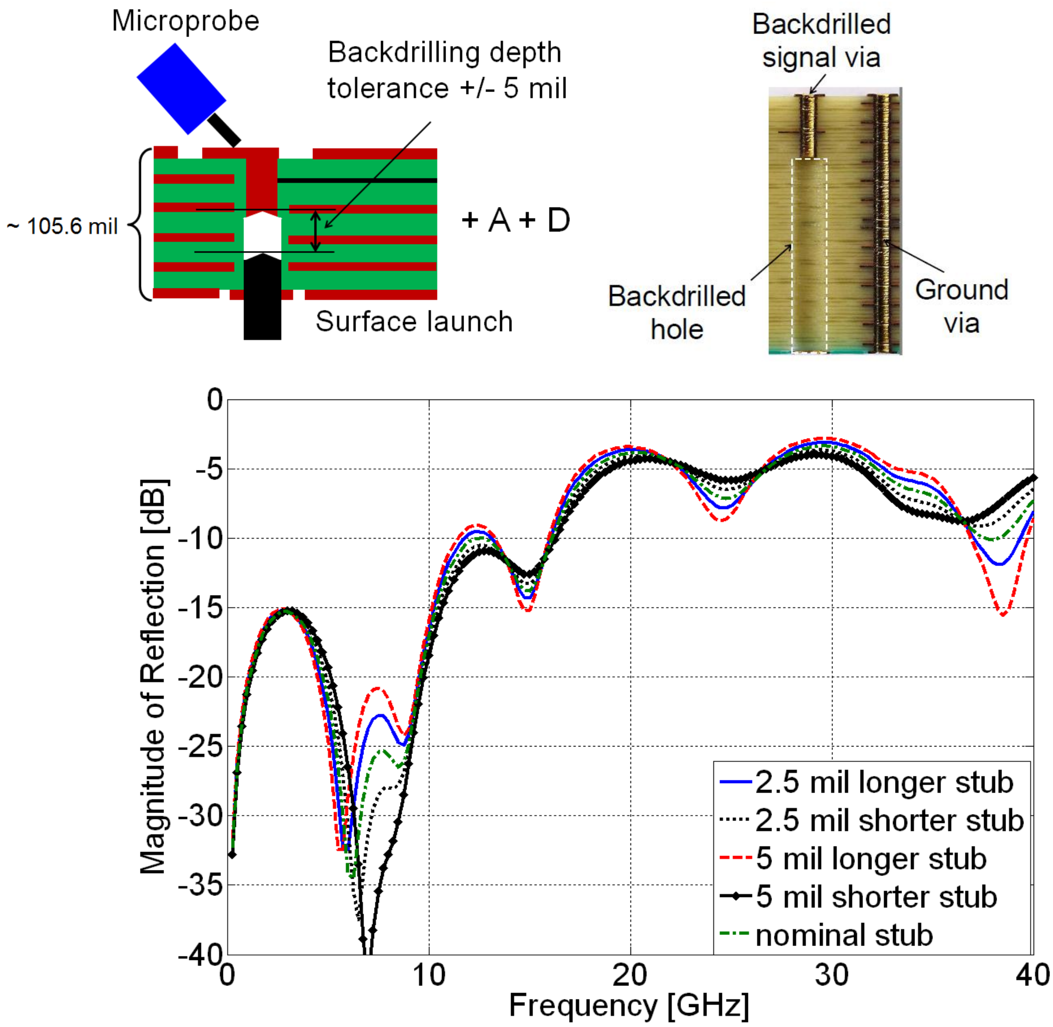


Figure 4.16 Comparison of reflection parameters obtained by a full-wave model of the cascaded models D + A + D [113]. The launch is sensitive to variations of the backdrilling depth. Accurate calibration or de-embedding of the launch in the bandwidth between 6 GHz and 9 GHz will be difficult and not accurate.

As can be seen in Figure 4.15, the detrimental effect on the return loss from the turning via obtained by using the recessed probe launch is less severe than when the surface launch (B-A-B) is used. Even if the access vias are backdrilled (D-A-D), the best performance is still achieved with the RPL (C-A-C). This leads to the conclusion that the surface launch has to be modified (optimized) or even de-embedded to remove its contribution to the obtained S-parameters as it otherwise masks the intrinsic behavior of the turning via.

Furthermore, the influence of the variations in via backdrilling and access via antipad diameter in case of the surface launch model (D-A-D) was investigated. In Figure 4.16 the results from the variation of the backdrilling depth are summarized. One can see that small variations in backdrilling depth can lead to significant errors in any calibration or de-embedding approach, especially in the region between 6 – 9 GHz.

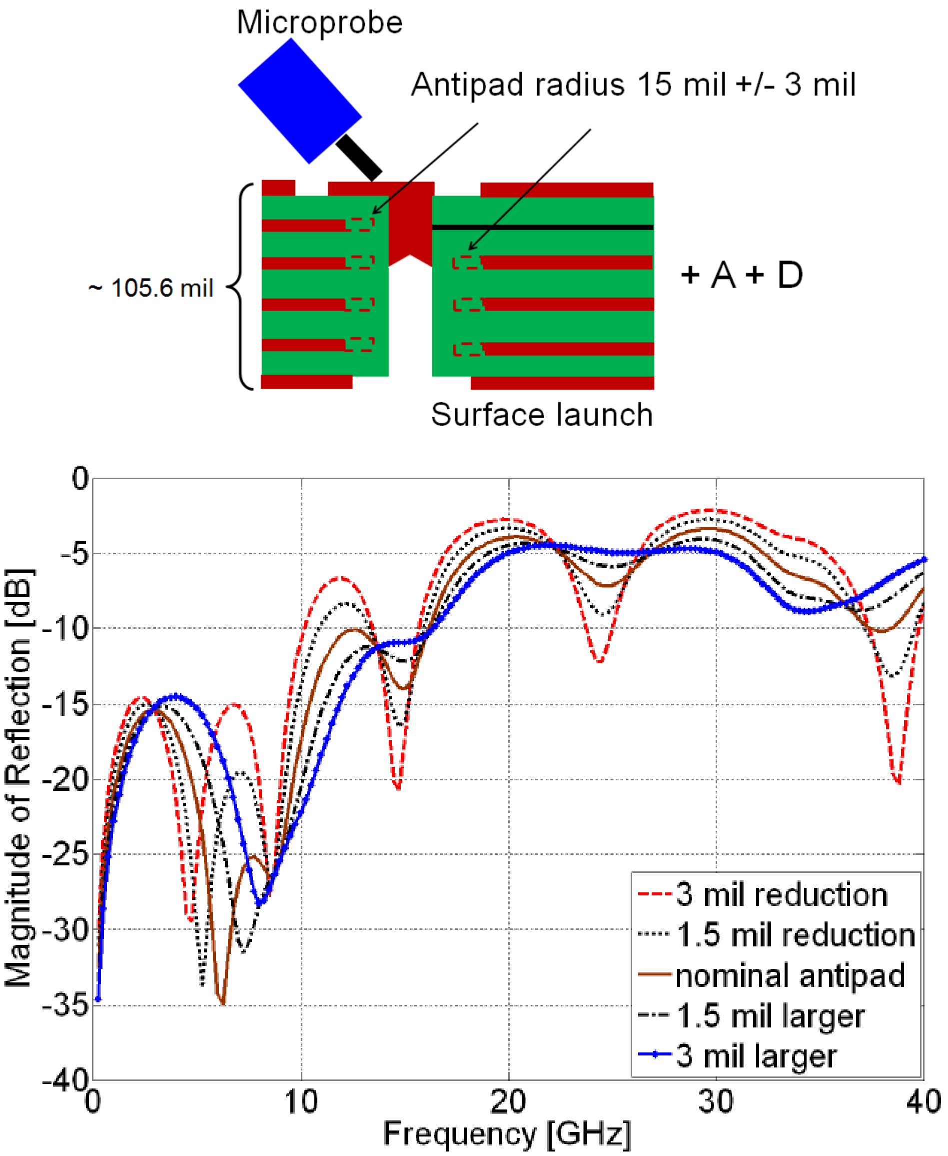


Figure 4.17 Comparison of reflection parameters obtained by a full-wave model of cascaded models D + A + D [113]. The launch is sensitive to the access via antipad variations. Accurate calibration or de-embedding of the launch in the full launch frequency bandwidth will be not accurate.

The sensitivity of the reflection parameters of the launch to antipad radius variations are shown in Figure 4.17. Based on the obtained results, the launch de-embedding might be inaccurate in the entire frequency range up to 40 GHz. Although via barrel/antipad eccentricity introduced by interlayer registration and drill placement tolerances will likely introduce additional significant variability, these effects were not simulated.

In the next Section, results from the investigations of the effect of the access via stub on microprobe on-surface launches and the associated issues applying the Thru-Reflect-Line calibration algorithm are presented.

4.4. Effect of Via Stubs on the TRL Calibration

Measurement of embedded structures in multilayer substrates (both in digital and analog applications) faces the problem of launching a high frequency signal into a layer that cannot be easily accessed from the surface. Using access vias (plated through holes) in combination with connectors or microprobes is a common approach (Figure 2.1). Furthermore, in most of the measurement scenarios one aims to remove the influence of the used signal launch from the measured data in order to reveal the intrinsic behavior of the test structure. In order to remove the effect of the utilized launch and thus to shift the reference (measurement) plane as close as possible to the structure under test, techniques such as time domain gating, port extension, and several calibration methods and de-embedding techniques can be applied [40], [85], [109], [134], [135].

In the following Sections, results from the investigations of the via stub effect ([22]) on the TRL calibration applied to an on-surface signal launch are presented [9].

4.4.1. Design of Multilayer Calibration Substrates

An on-surface probe launch was designed that can be applied to measurements of embedded (internal) printed circuit board (PCB) structures such as striplines and vias (Figure 4.18). In the following Sections, results from the investigations made for extraction of this signal launch by applying TRL calibration method are presented [9].

For this purpose, a dedicated calibration board with single-ended TRL standards containing nominally identical signal launches at the ends of each standard was designed. The board stack-up contains in total 18 metal layers (12 potential ground planes and 6 signal layers) and as dielectric substrate Nelco-13 (ε_r = 3.7, tanδ = 0.008 [104]) has been chosen. Line lengths of 200, 250, 280 and 450 mil were implemented on the test board in such way that the calibration in the bandwidth between 40 MHz and 40 GHz using ground-signal-ground (GSG) microprobes is possible. For the reflect standard the lines were simply left open. For these measurements, Picoprobe Model 50A DS-style GSG-225µm pitch microprobes from GGB Industries were used [24]. As illustrated in Figure 4.18 the proposed signal launch structure allowed both surface and "recessed" probing. Alternatively, probing on the top or the bottom of the PCB offers test signal paths with different signal via stub lengths depending on the investigated signal layer. As depicted in the layout on the stripline layer, one pair of ground vias with copper pads provides ground connection for a GSG microprobe if recessed probing is desired. The recessed probing technique is addressed in Section 4.5.

With help of the designed calibration standards the parasitic effect of the access via stub on the TRL calibration is investigated. Such stubs are always present unless buried via techniques or backdrilling are used. Access via stubs together with via impedance mismatches and other parasitic effects limit the measurement bandwidth.

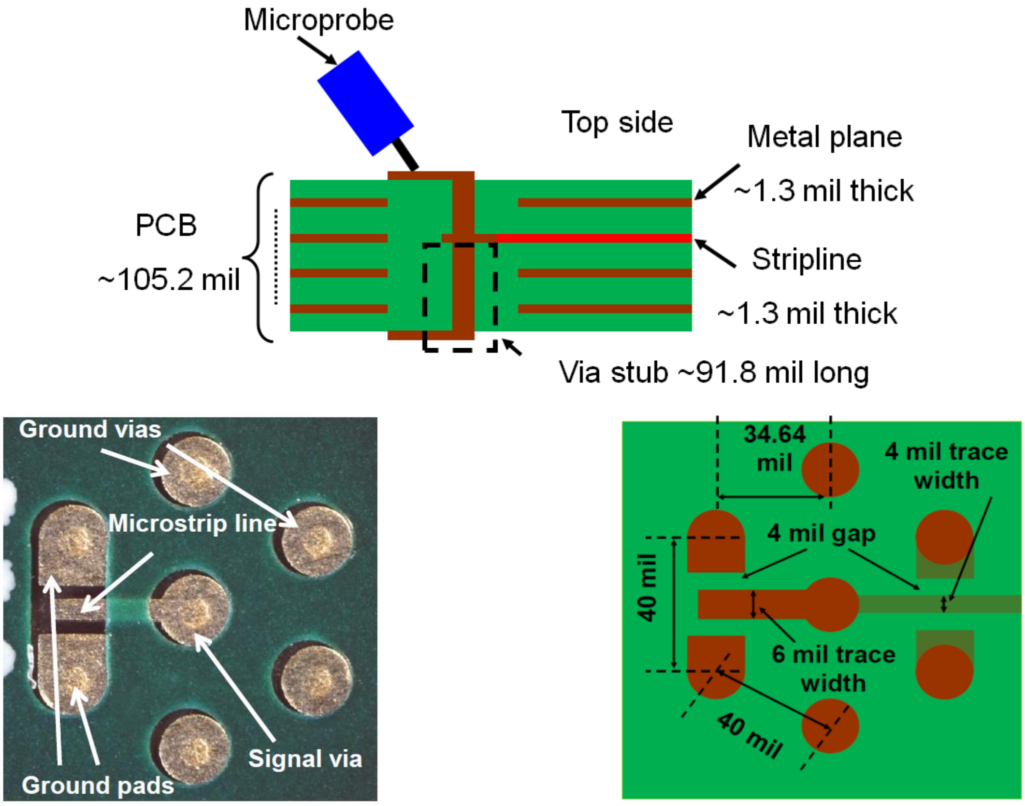


Figure 4.18 Signal launch layout on the top of the PCB (thickness ~105.2 mil) ready to be contacted with GSG-225µm pitch microprobes. The test signal is routed by an access via to the lower signal layer of interest. The access via stub is present when connecting from the top or bottom board side. A pair of ground pads is available on the lower signal layers after milling away of the overlaying layers for recessed probing [9].

Specifically, from transmission line theory it is known that at the quarter wave length frequency (and odd multiples thereof) open stubs act as a short, which leads to extremely high reflection and nearly zero transmission – visible as deep “notches” at the resonance frequencies [22].

4.4.2. Extraction of the On-surface Signal Launch

In this Section, results from the study of the signal launch accessed only from the PCB surface are presented. Measurements were made in the frequency range from 40 MHz to 40 GHz using a 2-port vector network analyzer (Anritsu 37397D). In order to be able to extract the error parameters of the signal launch by itself, a two-tier calibration approach was used (Figure 4.19). As illustrated, for the 1st tier a standard short-open-load-thru (SOLT) calibration was performed using the calibration standards on the calibration substrate (CS-5) provided by the microprobe manufacturer [24]. With this calibration the parasitic effects of the microprobes, cables, adapters etc. were removed from the measurements data. The 2nd tier was the TRL calibration that used the standards on the PCB. The main advantage of the TRL is that the applied standards

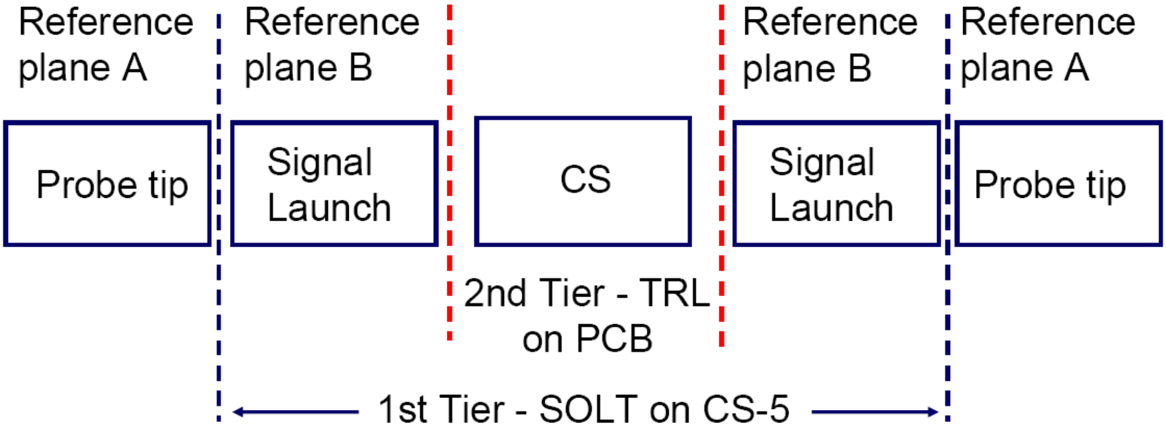


Figure 4.19 Two tier calibration procedure for extraction of the on-surface signal launch in multilayer PCB. For the 1st tier the SOLT calibration algorithm and the alumina substrate CS-5 provided by the microprobe manufacturer are used to set the reference plane at the probe tips. For the 2nd tier the TRL algorithm and the designed standards are measured with the calibrated microprobes to obtain the S-parameters (error parameters) of the on-surface signal launches [9].

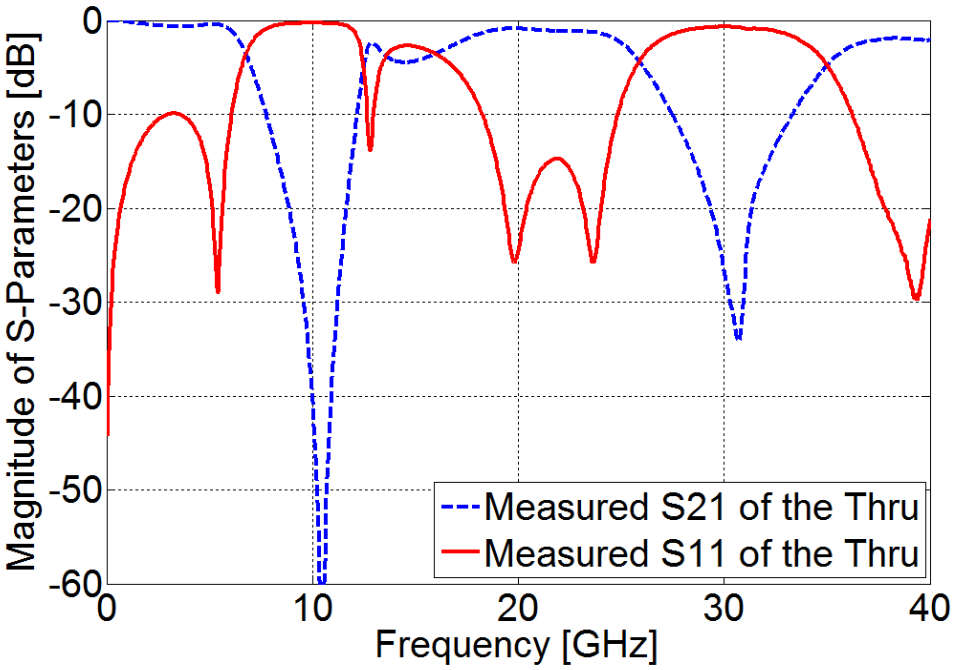


Figure 4.20 S-parameters of the thru standard obtained after the 1st calibration tier. The notches in the transmission parameters due to the access via stub resonance are clearly visible. Later on, these S-parameters are used for the 2nd calibration tier [9].

do not have to be fully known (self-calibration method, Section 2.4). TRL's basic requirements are that the line standard has to be electrically longer than the thru and that a high reflection standard (an offset short or open) is placed at the end of a line which electrical length corresponds to the half of that of the thru line. After the calibration the reference plane is set in the middle of the thru standard [47], [58], [110].

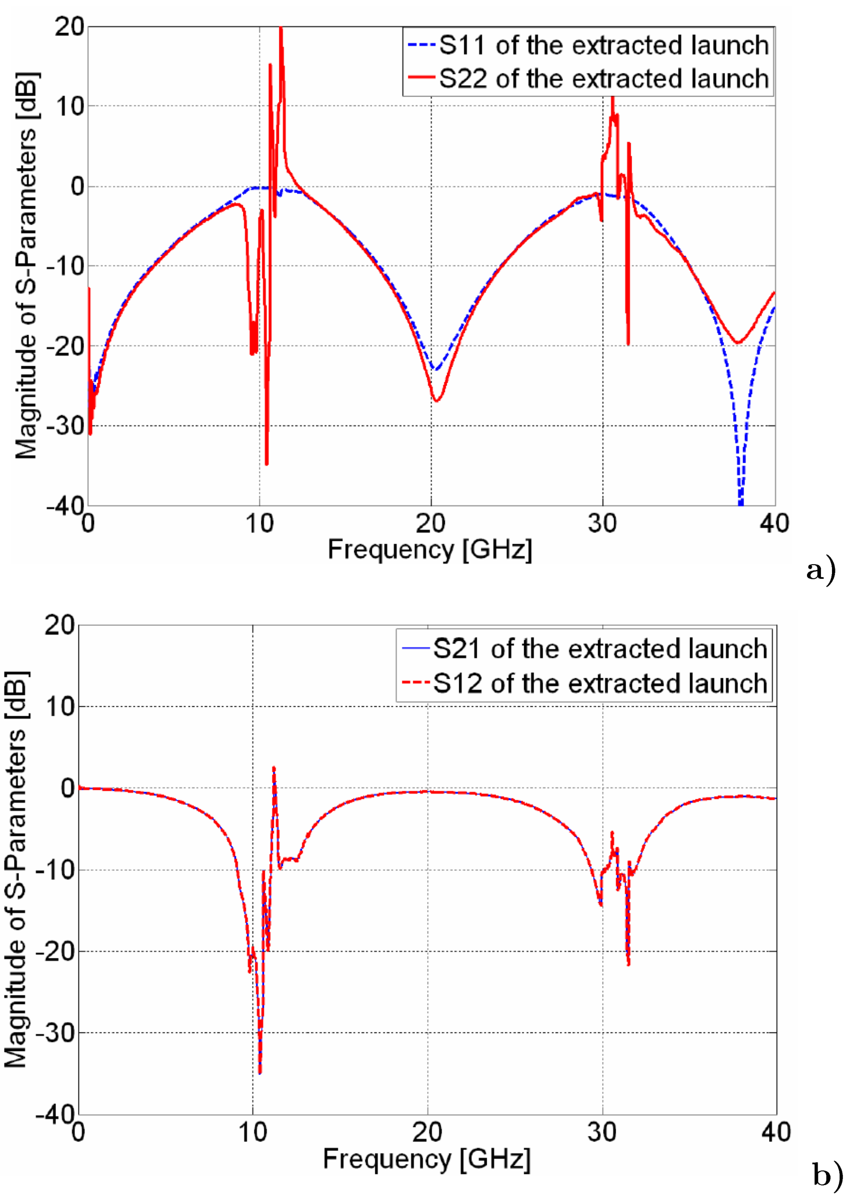


Figure 4.21 Error parameters for the signal launch (reflection a), transmission b)) extracted using 200 mil long thru and 250 mil long line standards for TRL calibration tier. The calibration algorithm obviously fails around 10 and 30 GHz (resonance frequencies of the access via stubs) [9].

In Figure 4.20 the S-parameters of the thru standard are shown measured after the 1st calibration tier. The notch in transmission around 10 and 30 GHz due to access via stub resonances can be clearly seen (stub length 91.8 mil, $f_{\lambda/4} \sim 10\,\mathrm{GHz}$). This thru standard is used for the proposed two-tier calibration method where the error parameters (S-parameters) of the signal launches could be obtained due to the difference of both calibration tiers. Results from this process for the signal launch extraction are presented in Figure 4.21. As can be seen, the error parameters of the launch are not passive in the range of 10 GHz and 30 GHz which is a clear indication that the calibration algorithm failed. The next Section gives possible reasons for this failure.

4.4.3. Analysis of Via Stub Effects

In a simplistic way the failure of the TRL with via stubs can be easily explained with the equivalent circuit of Figure 4.22. When the via stubs act as shorts at their resonance frequencies, they dominate the response of the standards, i.e. thru, reflect, and line standards all appear as shorts. Hence, the TRL algorithm becomes singular. However, there is still some transmission in the measurement data even at the resonance frequencies so it is not entirely clear why the failure is so complete and relatively broadband (several GHz). Possible reasons here could be the manufacturing tolerances whose effects are not taken into account in the equivalent circuit models (Figure 4.22)

As mentioned in the previous Section, an important condition for the TRL calibration is that the line standard has to be electrically longer than the thru with respect to the considered calibration bandwidth. In order to examine this requirement the unwrapped phases of the transmission of the measured thru and several line standards were considered (Figure 4.23).

It is obvious that the line standard 1 and 2 are no more electrically longer than the thru at 10 GHz. Line standard 1 is almost as long as the thru in the range of 31 GHz. In Figure 4.24 it is shown that for all three lines the effective phase difference of $20° < \Delta\varphi_{eff} < 160°$ - known as condition for the design of the thru and line standards and as limitation for the calibration bandwidth - is not kept in the desired calibration bandwidths [59]. It is important to note that in case of line 1 standard this is partly due to the fact that it was not designed for usage below 12 GHz. Nevertheless, for all other line standards (2 and 3) available on the test board, the violation of the phase difference criterion below 12 GHz is critical. To investigate this calibration issue further S-parameters obtained from a circuit simulator using the simple equivalent circuit model of Figure 4.22 were used as data sets for the TRL algorithm. The results from this investigation have shown that phase difference violations do occur albeit with a much smaller bandwidth (100 MHz).

Based on these results one came to the conclusions that the via stub effect compromises TRL calibration viability

- due to extremely low transmission at notch frequencies,
- large phase dispersion in the vicinity of the high Q notches violates the phase separation requirement,
- is aggravated by variations in the signal launch due to manufacturing tolerances.

To summarize, this study has shown that the proposed launch cannot be de-embedded over the full TRL bandwidth (10 MHz – 40 GHz) using the available calibration algorithm due to the quarter wavelength resonances of the via stubs. The mechanical precision and dielectric uniformity needed to make such an approach

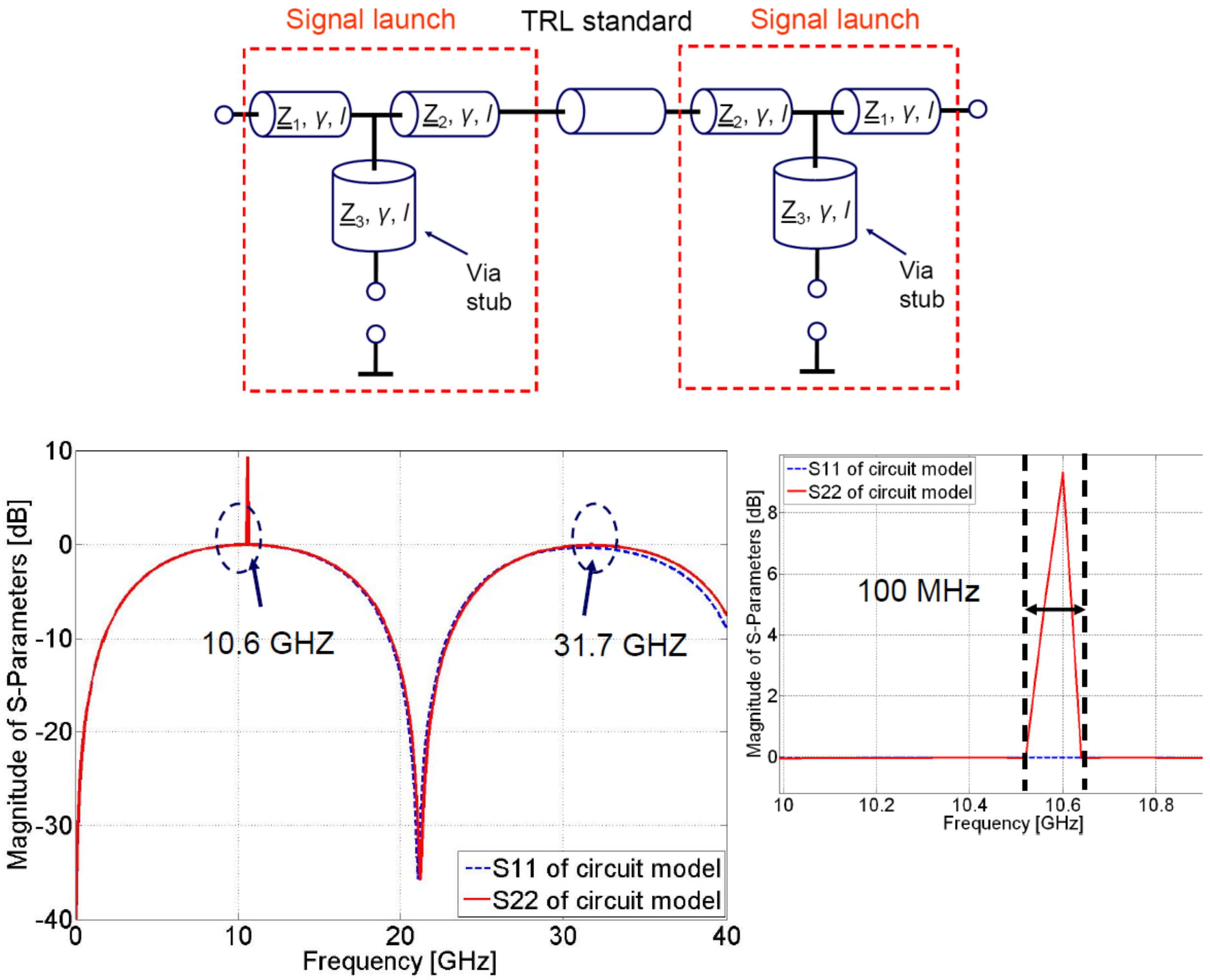


Figure 4.22 First order equivalent circuit for signal launch and TRL calibration with access via stubs (Z_1= 50 Ω, Z_2= 50 Ω, Z_3= 20 Ω, l_1= 25 mil, l_2= 100 mil, l_3= 145 mil). The passivity violation is present even if circuit model parameters are used for extraction. The resonance bandwidth is reduced but not completely removed [9].

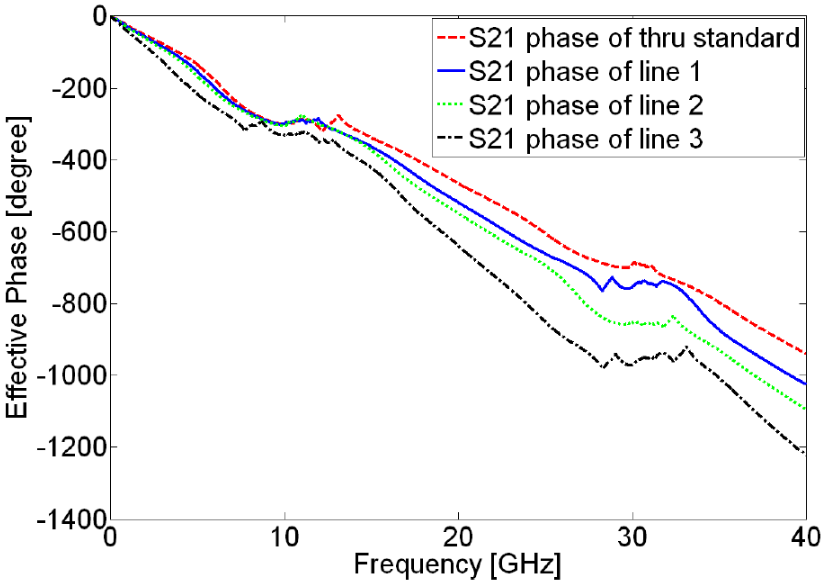


Figure 4.23 The phases of the thru and line standards overlap in the range of 10 GHz and are very close-up at 30 GHz. The TRL algorithm fails and cannot extract the error boxes correctly [9].

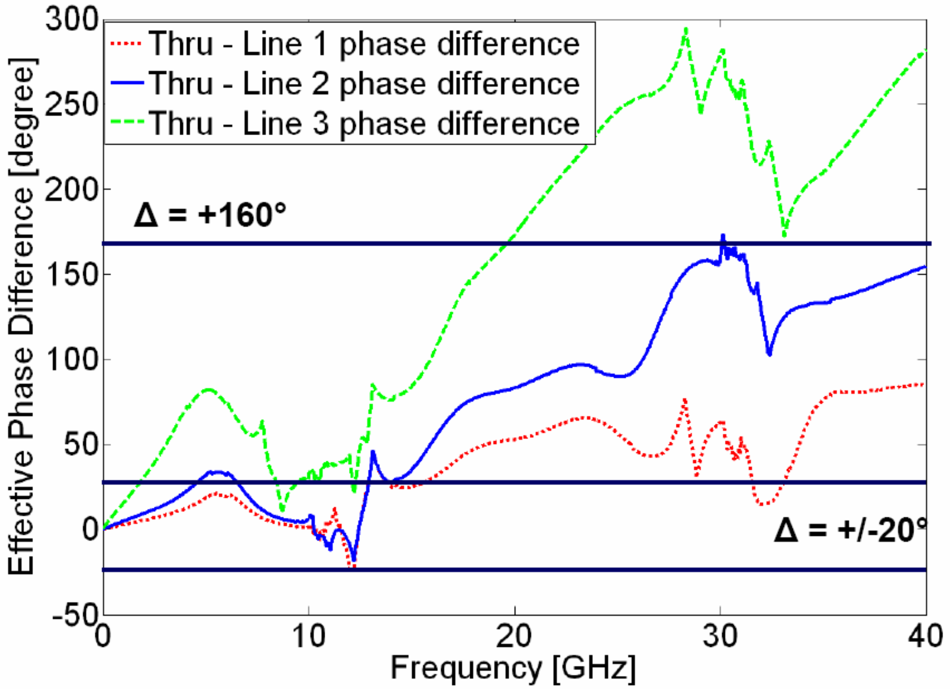


Figure 4.24 Effective phase difference of 200 mil long thru standard and ~250 mil (Line 1), ~280 mil (Line 2) and ~450 mil (Line 3) long lines. Here, the longer line standards violate the effective phase limit at 10 GHz too [9].

feasible is not obtainable in printed circuit board fabrication as currently practiced. In the next Section some specific mitigation strategies are suggested.

4.4.4. Mitigation of Via Stub Effects

When digital link structures are implemented on multilayer PCBs, a common technique called "backdrilling" is typically applied as an additional manufacturing step for reducing the via stub effect. This method is a mechanical challenge which requires accurate knowledge of the board stack-up and a precision drill press or milling machine. When the backdrilling is not desirable, more expensive buried/blind vias can be used or fewer signal layers have to be utilized for signal routing. Also the notch in the transmission can be shifted to higher frequencies by improving the return current path of the via when ground vias are placed closer to the signal via or by increasing the via antipad diameter. The latter techniques offer only small perturbations of the notch frequencies and only severe reductions in stub length are effective in moving the resonances out of the frequency bands of interest.

Since backdrilling is often more cost-effective and thus preferred, an attempt was made to derive an empiric formula which might help to relate the stub resonance frequency (F_{notch}) and the stub length in mil ($Stub\_length$). The ratio shown in Figure 4.25 was computed from a full-wave model excited by "lumped ports" (two 100 Ohm ports each in parallel for one microstrip line end on the top side of the PCB) to mimic the surface probe launch; at the stripline end a waveguide port was used.

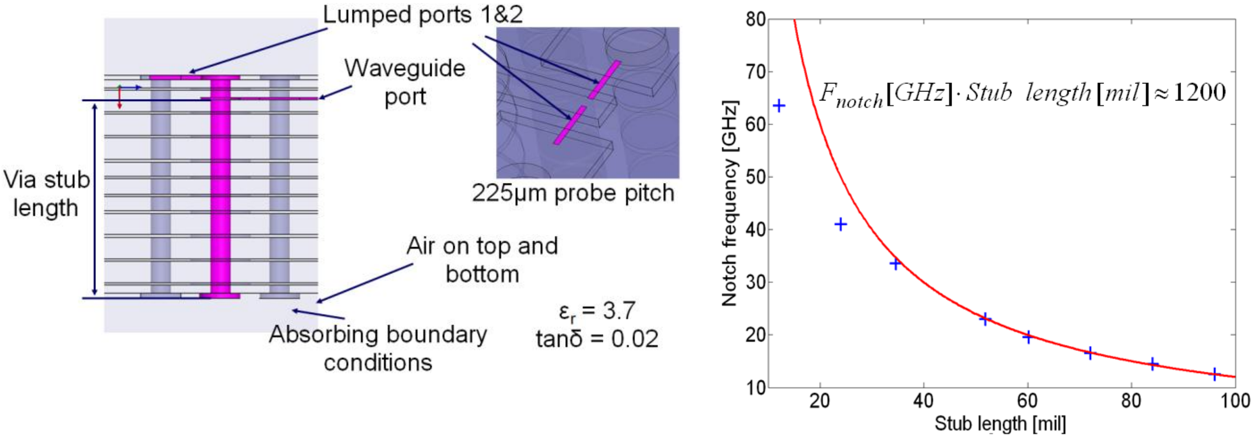


Figure 4.25 Full-wave simulation model of the signal launch nominal case [113]. The notch frequency in the transmission can be estimated from the ratio of the via stub length and the constant extracted from the full-wave models [9].

For this specific PCB layout of the signal launch, a mitigation of the via stub effect could be achieved by launching the test signal from the bottom side (Figure 4.26). The extracted error parameters of a probe launch routing signals to the first signal layer (the first signal layer counting from the top to the bottom board side) measured from the bottom board side have been correlated to simulation data obtained by a full-wave model excited from the board surface with a coaxial wave-guide port in form of a probe tip. In this case the stub effect was shifted beyond 30 GHz and as shown in Figure 4.26 good correlation to the model was obtained.

Results from the full-wave analysis showed that the calibration bandwidth can be extended when the via stub effect is reduced or even removed as follows:

- Backdrilling of the signal via stub for shifting the stub resonance frequency beyond the calibration bandwidth. The maximal length of the via stub for shifting the notch frequency beyond the calibration bandwidth can be estimated from Figure 4.25 for the presented launch.

Using the recessed probe launch technique after removal of the upper PCB layers and disconnecting the via stub from the signal launch pads (Figure 4.27). This approach is explained in the next Section.

In general, in this Section it was shown that for the suggested launch the via stubs can be kept as short as possible when measuring from the top or the bottom PCB side depending on the signal layer that is measured. The full-wave simulations of the backdrilled launch and the recessed launch have shown how the via stub issue can be avoided. Further investigations with regard to the recessed probing are made in the next Sections.

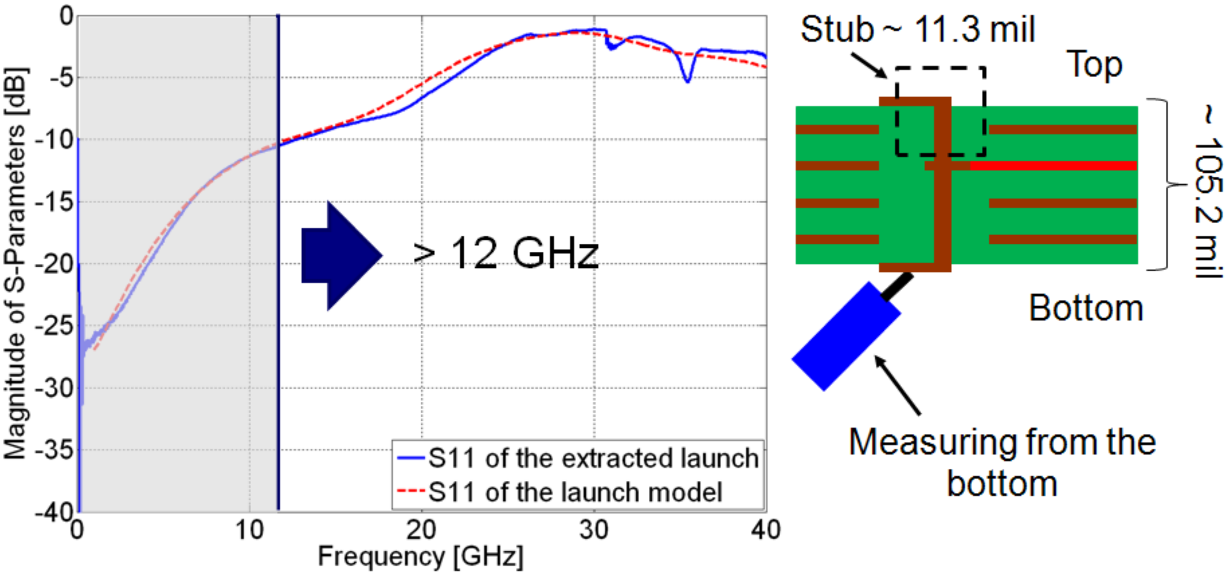


Figure 4.26 Extracted error parameters when measuring from the bottom side. The used line standards are designed for the calibration bandwidth beyond 12 GHz - the extracted launch S-parameters correlate well to the used full wave model [9].

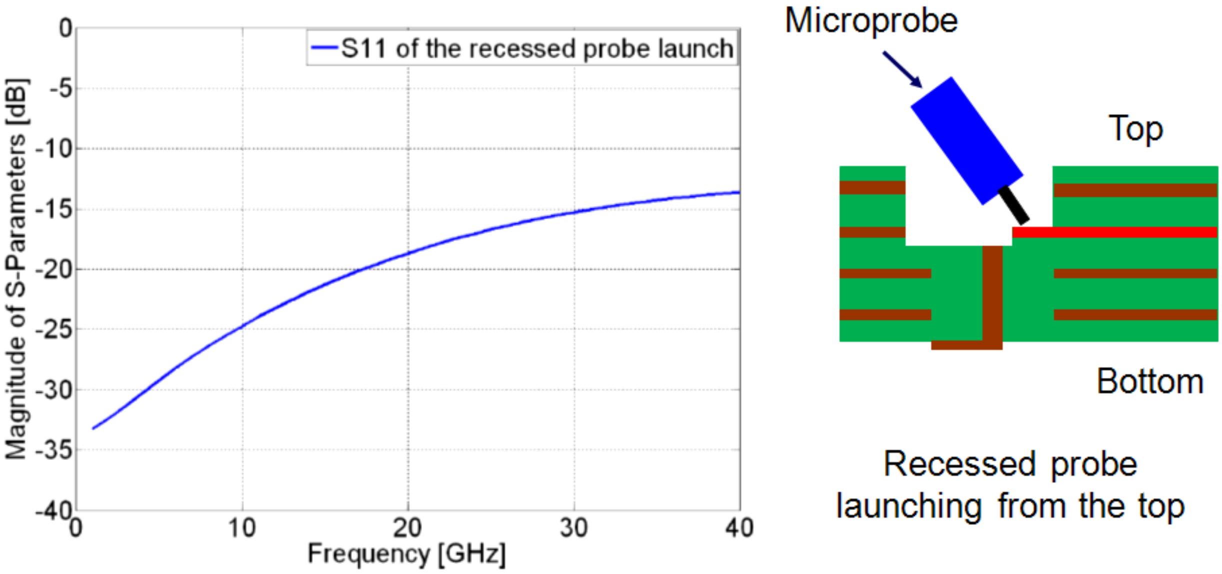


Figure 4.27 S-parameters from the full-wave simulation model of the recessed probe launch. Here, the access via is no longer needed for launching of the test signal into the test structure (strip line) [9].

4.5. The Concept of the Recessed Probe Launch (RPL)

As presented in Section 2.1 access vias are most commonly used for connecting of surface probe launches and connectors with internal PCB structures. As shown in Section 4.3, removing the impact of a signal launch and the associated signal access via from the frequency response of the device under test (DUT) is a complicated process which usually relies on de-embedding techniques. The validity of this procedure assumes that corresponding “DUT” and “calibration” structures behave identically, which is often not achievable due to existing mechanical tolerances in PCB manufacturing (manufacturing tolerances of ±10 % are expected). The limitations due to these tolerances were discussed in Section 4.3. where an attempt to de-embed on-surface probe launches with access vias by applying a TRL calibration algorithm failed. Here, the concept of an alternative recessed probe launch technique presented for the first time in [23] is reviewed.

The main advantage of the recessed probe launch (RPL) technique is the elimination of access vias for connections to internal PCB structures (Figure 4.28). After precise milling of the upper board layers, microprobes can be positioned close to the DUT, which allows high frequency measurements of PCB structures. In the following Section, the layouts of three different launches are presented and the milling procedure needed for exposing the embedded probe contact structures is explained.

4.5.1. Preparation and Access

The preparation and layout of a milled recessed probe launch (RPL) is shown in Figure 4.29. In the following, three alternative RPL design types are presented - the regular (Figure 4.30), the combined (allowing surface probing without milling, Figure 4.31) and the embedded recessed probe launch (Figure 4.32). Additionally the required milling technique is described in detail.

The regular RPL depicted in Figure 4.30 was used for the investigations in [7], [23], and [108], where the dimensions of the launch and the milled cavity size were described. Milling the overlaying layers from the PCB stack-up provides access for an RF microprobe which can be directly placed on the terminus of the stripline. In addition, two copper pads on the signal layer connected to nearby ground vias ensure the continuity of return current paths for the microprobe. These ground vias are only partially milled away during the cavity formation.

The combined recessed probe launch is presented in Figure 4.31. As discussed in [9], the combined launch can be used either for on-surface probing or - after milling the access via and disconnecting the residual via stub from the signal launch pads - as a regular recessed probe launch. For this purpose two ground pads are embedded on the signal layer similar to the regular RPL. The advantage of this combined launch technique is that depending on the accessed signal layer one can choose to connect the

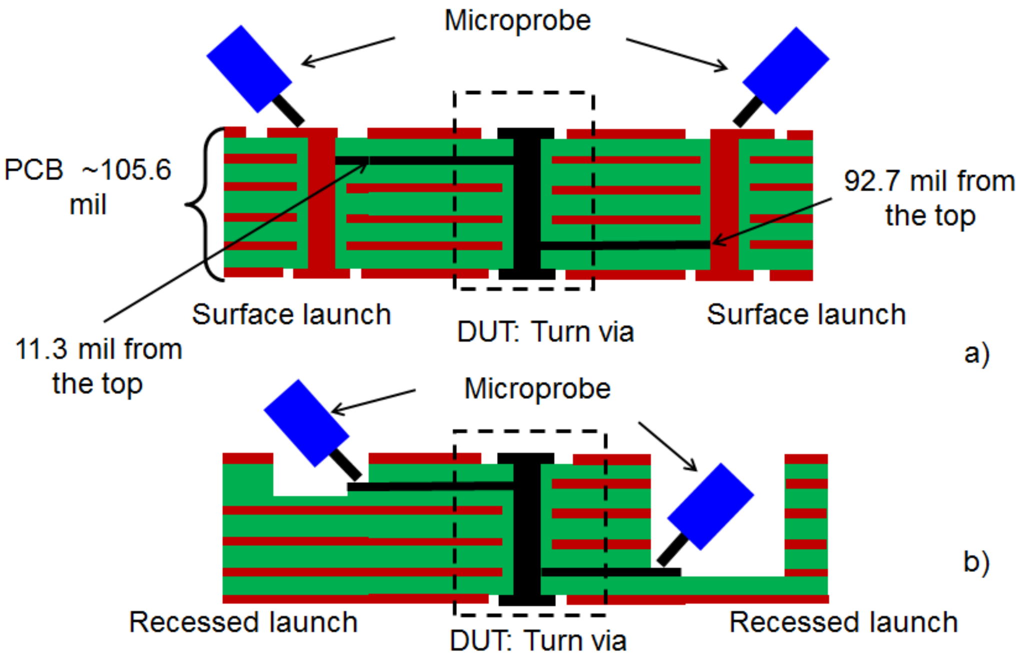


Figure 4.28 Comparison of surface launch techniques - in contrast to the common surface probe launch (a) in case of the recessed probe launch (b) the access via is completely removed and the stripline on the signal layer can be directly connected. Recess probing from both sides is also possible which is more convenient for milling but less convenient for probing because one sided recessing also requires large cavities to clear the probe shafts [14].

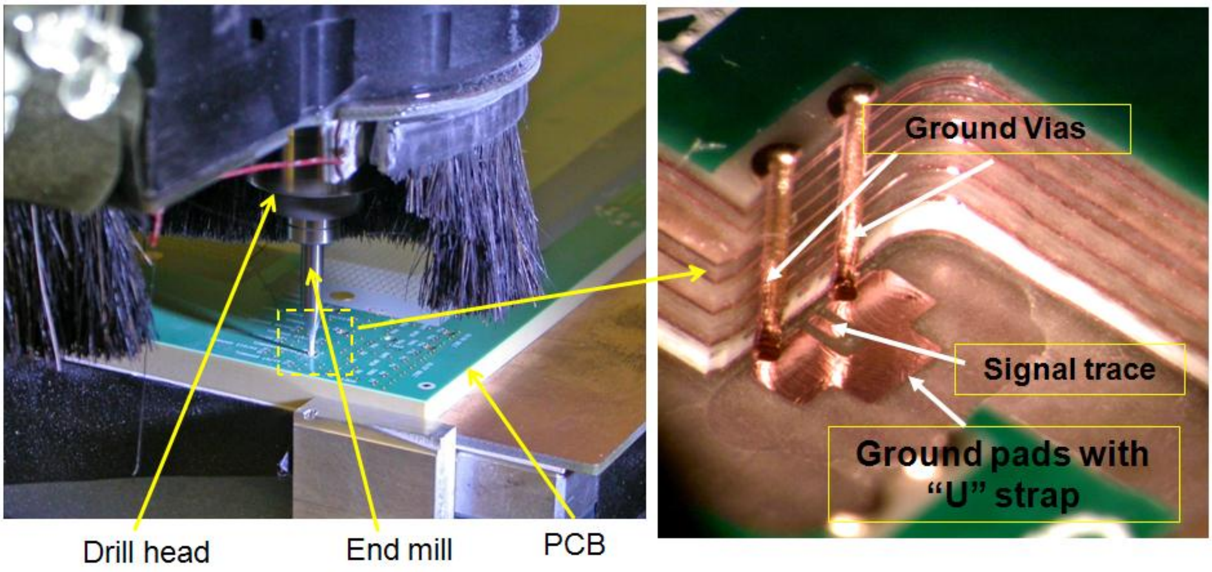


Figure 4.29 For the preparation of the recessed probe launches, end mills are used to expose the stripline in the signal layer. The z-axis milling precision of the machine has to be better than 0.5 mil for 1oz (1oz = 0.0311 kg) copper. Spindle speeds range from 20k-50k revolutions per minute (RPM) depending on the cutter diameter [15]. A pair of ground vias with copper pads on the signal layer (layer with the exposed stripline) provide the return current path for the ground tips of a GSG - microprobe. The "u"-strap structure allows the option of GS-or SG-microprobes albeit with some performance penalty [7].

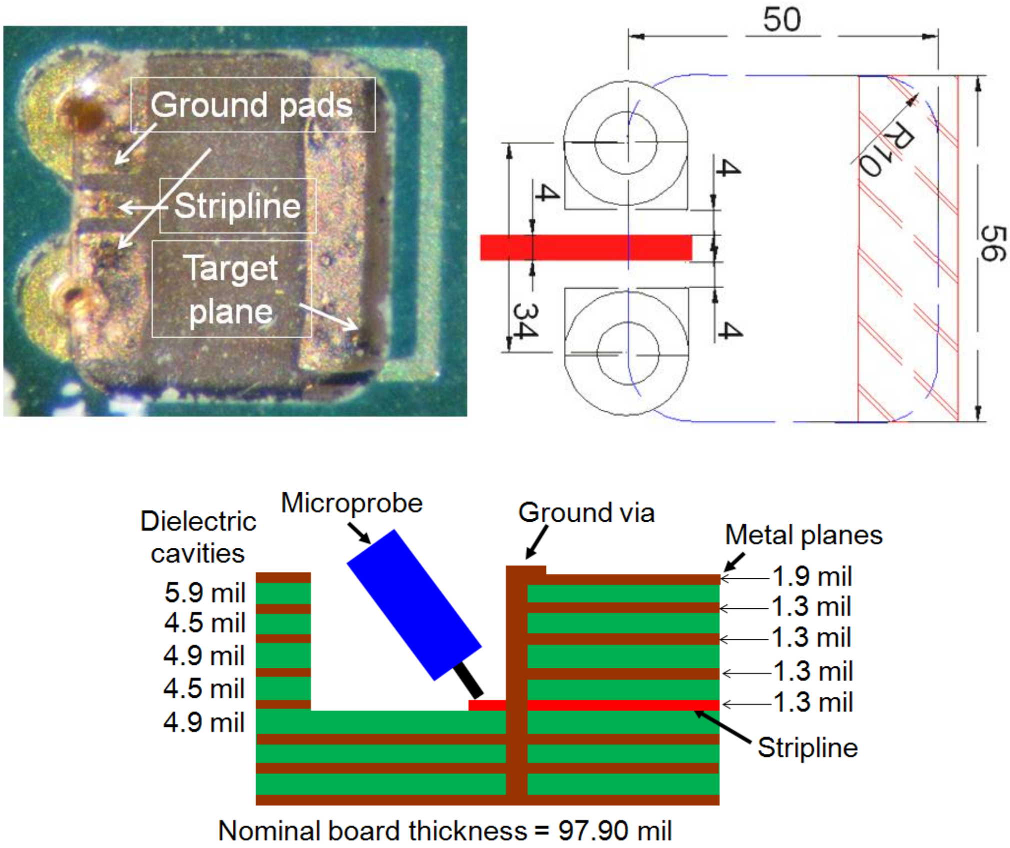


Figure 4.30 The recessed probe launch ready to be connected with GSG microprobe. All upper layers are milled away and thus the stripline can be directly contacted by a GSG microprobe. The two ground vias placed nearby are connected to the copper pads on the signal layer which provide the ground paths for the probe tip return currents [7].

microprobe from the bottom or the top board side in order to have a shorter via stub in the signal transmission path if recessed probing is not desired (Section 4.4).

An alternative embedded recessed probe launch is shown in Figure 4.32. This embedded launch option can be used in actual board designs if space exists to accommodate one (preferably two) GND vias in close proximity to a stripline that might need to be accessed. If such a need arises, the latent diagnostic capability can be exercised by milling a cavity and sectioning the stripline to create a recessed launch that can access either proximal or distal branches of the severed stripline. If this capability is not exercised, the presence of the GND vias does not materially perturb the behavior of the stripline. In contrast to the launch which was already presented in [23] here quadratic ground pads are utilized for ensuring larger probe skating region and thus to reduce the probing effort. With the aim to verify the parasitic effects of the RPL along a continuous stripline, full wave simulations have been carried out for this modification, too. The results have shown that the minimum gap between the stripline and the ground pads has to be at least 4 mil. The results from the influence of the quadratic ground pads and of the RPL by itself on the link performance are summarized in the next Section.

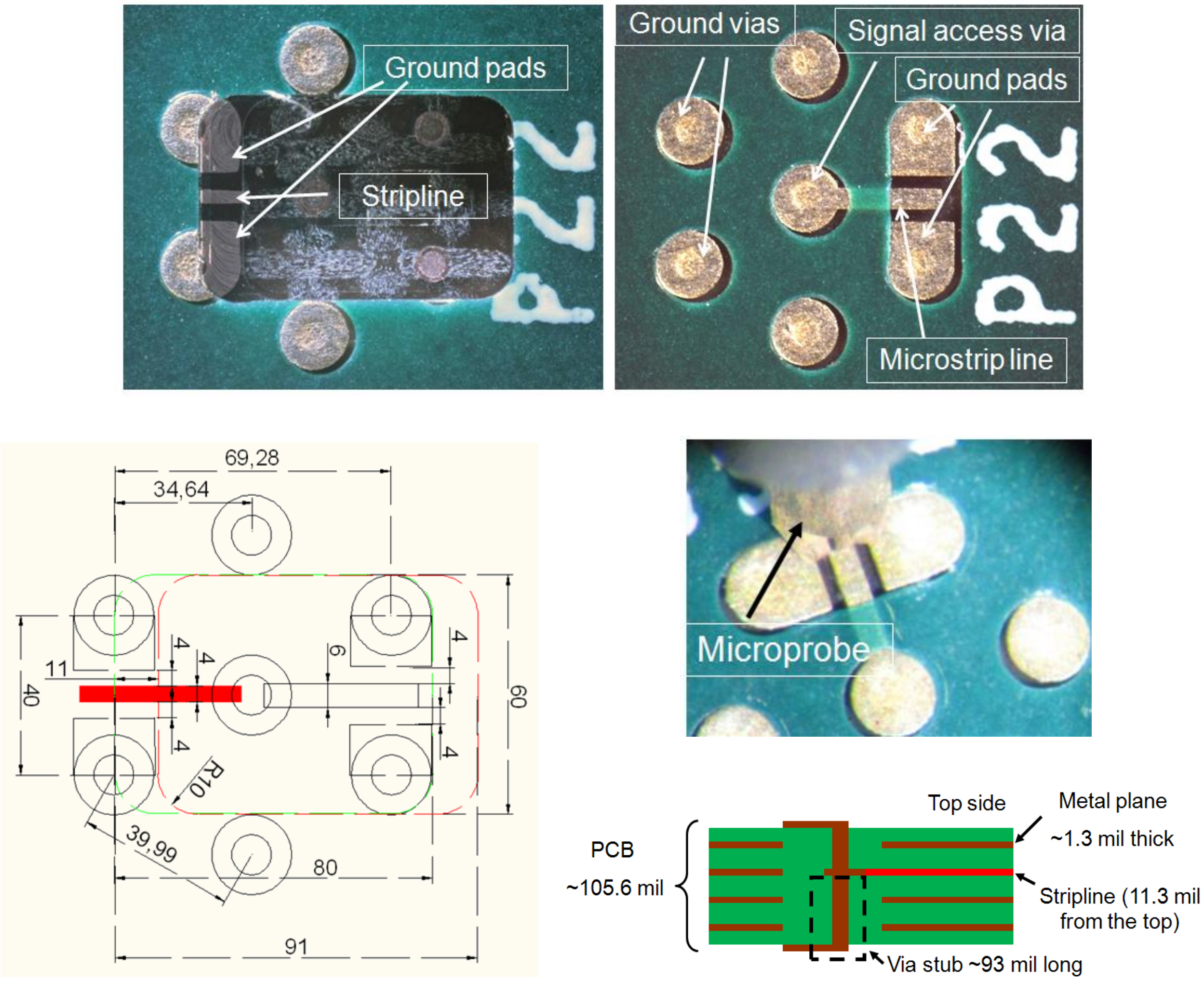


Figure 4.31 The combined recessed probe launch layout: The launch can be used either for on-surface probing by connecting the probe to the microstrip on the top/ bottom board side, or after milling away of the overlaying layers, for recessed probing [9].

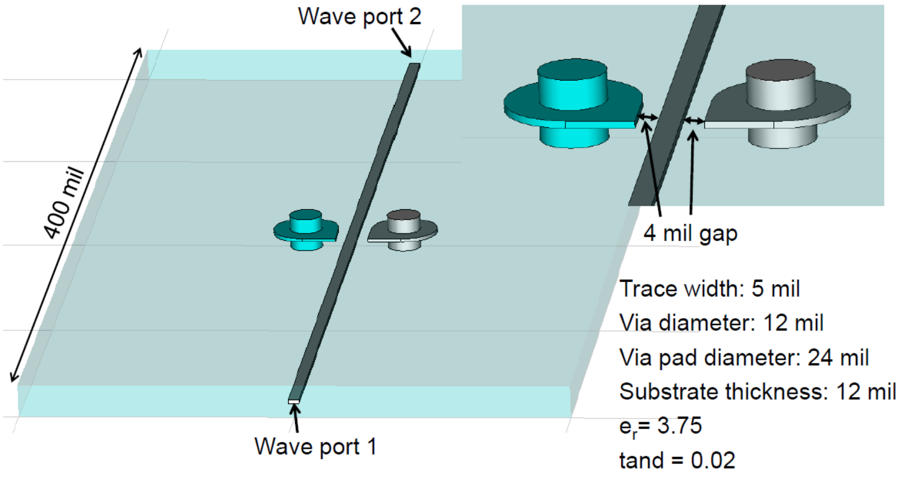


Figure 4.32 Full-wave model of the embedded recessed probe launch. The effect of the quadratic ground pads on 400 mil long stripline is investigated and the gap between the stripline and the ground pads is varied [111].

For the preparation of the RPL, a milling machine with a spindle speed of at least 10k - 20k revolutions per minute (RPM) is required depending on the diameter of the cutter [23]. Removal of the overlying layers without compromising the signal layer traces requires z-axis precision to be better than 0.5 mil, mainly constrained by the thickness of the copper layers which can range from 0.7 - 1.3 mil. High resolution visual access is required to ensure complete removal of the overlying dielectric as residual layers as thin as 0.1 mils can interfere with probe contact. Achieving these tight tolerances usually requires a representative portion of the PCB to be cross-sectioned and polished to verify the actual internal board structure which often deviates from the nominal PCB stack-up dimensions. Carbide end mills changed frequently help keep the cutting edges sharp so that the milled copper traces and pads on the signal layer have smooth surfaces to avoid possible snagging of the microprobe tips. Another method for estimation of the “real” milling depth for accessing the desired signal layer is the design of metal targets (small planes) on the signal layer of interest closer to the signal launch as depicted in Figure 4.30. The drawing of the cavity to be milled is illustrated in Figure 4.30, where the milling area overlaps the metal plane (target plane). Starting the milling of the launch from this region avoids the accidental cutting of the signal trace in case of large tolerances in the PCB stack-up. Furthermore, as shown in Figure 4.31 the cavity of the combined RPL consists of two composite cuts (each measures 60 x 80 mils with 10 mil radius corners). The first cavity (green) is the shallower one and exposes the copper metallurgy on the desired signal layer. The second cavity (red) is translated by 11 mils and cuts 1.5 - 2 mils deeper to sever the stripline trace from the signal pad and the signal via.

As shown in Figure 4.33, microprobes with steep angles of 45° are used to minimize the size of cavity required for rear side probe clearance [24]. Excessively large cavities can invite the generation of parasitic resonances.

The next Section presents electrical performance analyses of the recessed probe technique based on full-wave modeling backed up with hardware measurements.

4.6. Electrical Performance Analysis of the RPL

In Section 4.3, it was shown that tolerances in the PCB manufacturing process have a detrimental effect on the design of surface launches and thus accurate calibration and de-embedding become a challenge. Here, this issue is viewed from two different aspects - to design a signal launch with negligible parasitic effects, and, if necessary, to calibrate/de-embed the signal launch if its contribution to the measured data cannot be neglected. The first aspect is considered in the investigations of the electrical performance of the RPL with regard to a -20 dB return loss limit which corresponds to the maximum reflection of 50 Ω ± 5 Ω stripline in a 50 Ω system. Here, the goal is to design a signal launch which does not exceed this bandwidth limit up to frequencies

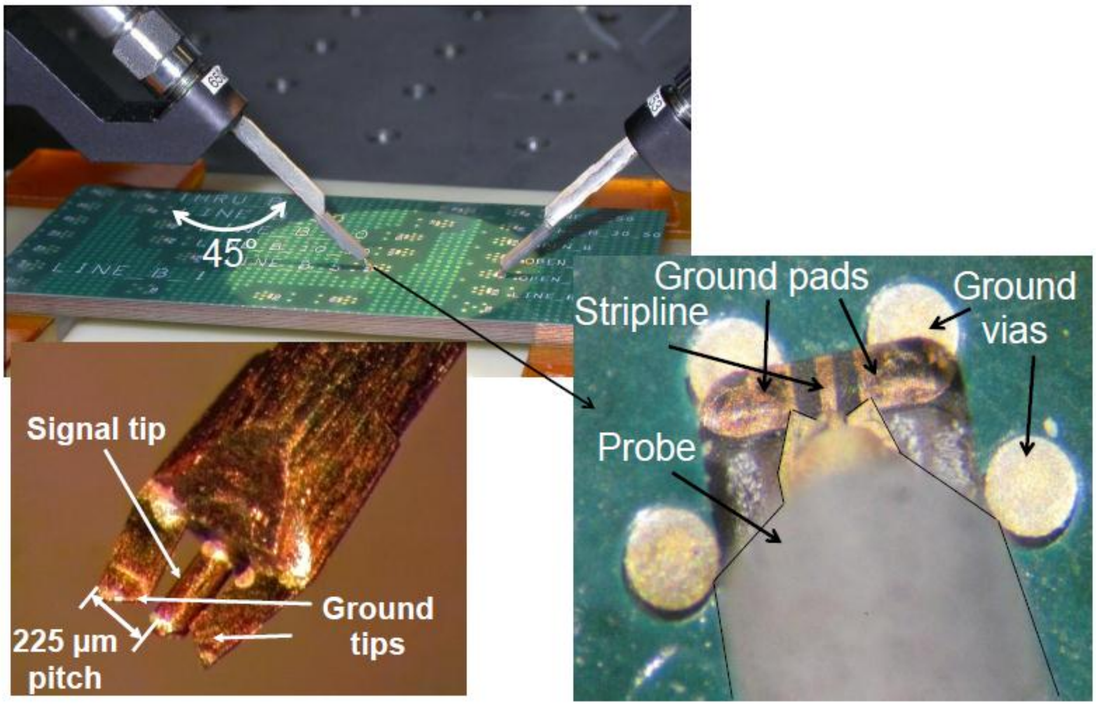


Figure 4.33 A milled recessed probe launch connected with GSG-microprobes. For accessing the exposed launch microprobes with an angle of 45° are required [8].

that are commensurate with today's high speed digital interfaces (10 Gbit/s and higher). In addition, the launch can be calibrated/de-embedded e.g. using the TRL calibration method which further reduces its impact on measurement results.

4.6.1. Transmission Characteristics of the RPL

In order to extract S-parameters of the RPLs and thus to investigate their electrical performance, single-ended TRL calibration standards were designed on a multilayer printed circuit board with "identical" signal launches at each end. Line lengths of 200 and 250 mil were used for the TRL calibration in the bandwidth between 10 GHz and 40 GHz [8], [47], [59], [112]. For the reflect standard, the lines were simply left open. The calibration board contains in total 18 metal layers (12 potential ground planes and 6 signal layers) with Nelco4000-13 (ε_r = 3.7, tanδ=0.008, [104]) as the dielectric. The calibration standards were measured using microprobes with 225 µm pitch (signal-to-ground distance, Picoprobe Model 40A DS-style GSG-225) which were calibrated using the SOLT (Short-Open-Load-Thru) calibration standards on an alumina substrate (CS-5). Following the procedure explained in [8], the error parameters of the milled RPLs were extracted by applying a two-tier calibration method (Figure 4.34). In the 1st tier the effects from the VNA hardware were removed by the SOLT calibration and the reference plane was shifted to the probe tips. In the 2nd tier the TRL standards were used for the extraction of the error parameters (S-parameters) of the milled RPLs

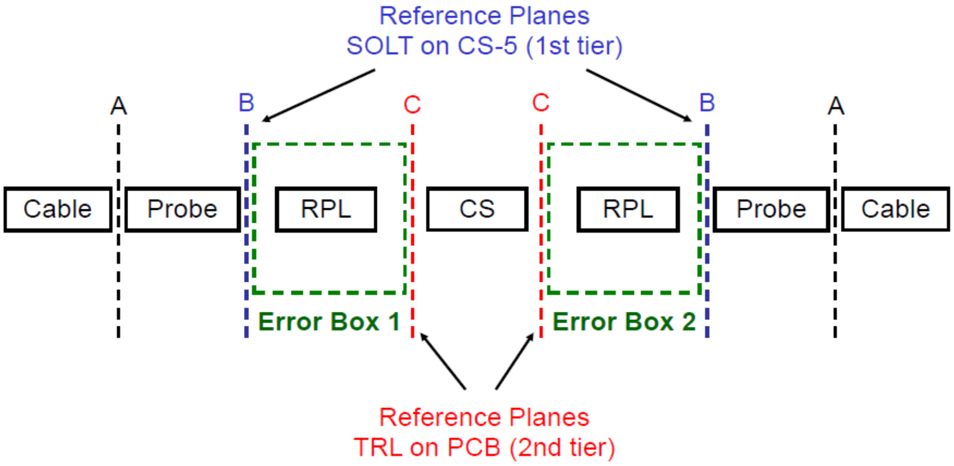


Figure 4.34 Connectivity of the extracted error boxes of the two RPLs. An initial 1st tier calibration is required for the removal of the measurement error due to the measurement hardware – VNA, cables and the microprobes. The second tier was used for the extraction of error boxes [9].

where - after the 2^{nd} calibration tier - the reference plane is shifted in the middle of the thru standard [47].

In order to validate the extracted error parameters, an attempt was made to capture the probe parasitics on the PCB using the probe tip model as depicted in Figure 4.35. The extracted reflection and transmission parameters are correlated to the computed data obtained by the full-wave model as shown in Figure 4.36 and Figure A.7.24 (in the Appendix A.7). As shown there, the extracted and computed S-parameters correlate well in the investigated calibration bandwidth. As can be seen, the worst case return loss of -14 dB and insertion loss of -0.57 dB were obtained at 40 GHz. Hence, the model with the microprobe excitation can be used for the characterization of the designed RPL. Here, it is important to note that the characteristic impedance of the used stripline corresponds to 48 Ω at 40 GHz and it represents the reference impedance for the computed S-parameters.

With help of full-wave 3D models and microprobe based measurements, the RPL was scrutinized in [7], [23], [108]. The comparison between models with GS (ground-signal) and GSG (ground-signal-ground) port excitations (probe + RPL models or lumped ports + RPL) lead to the conclusion that the nominal RPL is mostly applicable to GSG-microprobe configurations where the probe parasitics (~60 - 70 pH, [24]) are reduced by providing additional return current paths thus achieving the highest bandwidths. The time domain analysis of a probe connected to the RPL has shown that the discontinuity is mainly inductive [108]. In Figure 4.36 and Figure A.7.24 (in the Appendix A.7) the correlation of the lumped model (75 pH) to the extracted S-parameters of the RPL designed on the calibration board are shown. To achieve better correlation with respect to the transmission parameters (Figure A.7.24 in the Appendix A.7) the material losses have to be included into the model.

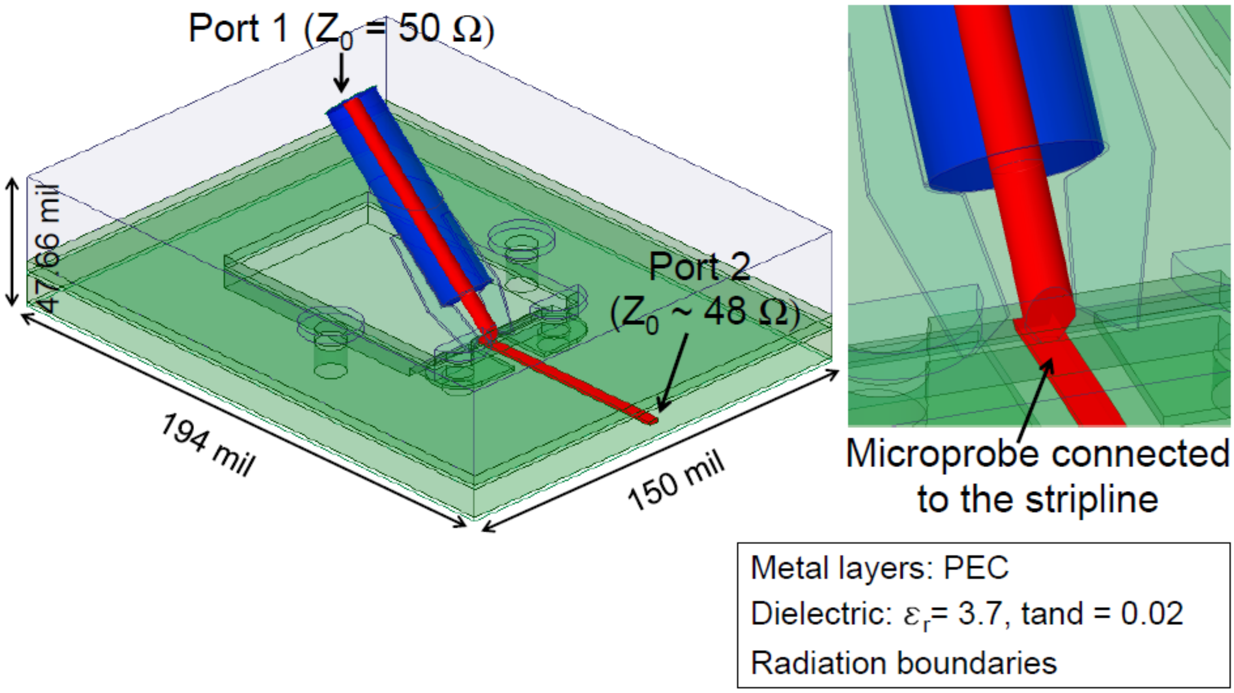


Figure 4.35 Full-wave model of a milled recessed probe launch [113]. The stripline is connected with a short microprobe model. The computed S-parameters correspond to the extracted S-parameters of one RPL on the test board by the TRL calibration procedure [14].

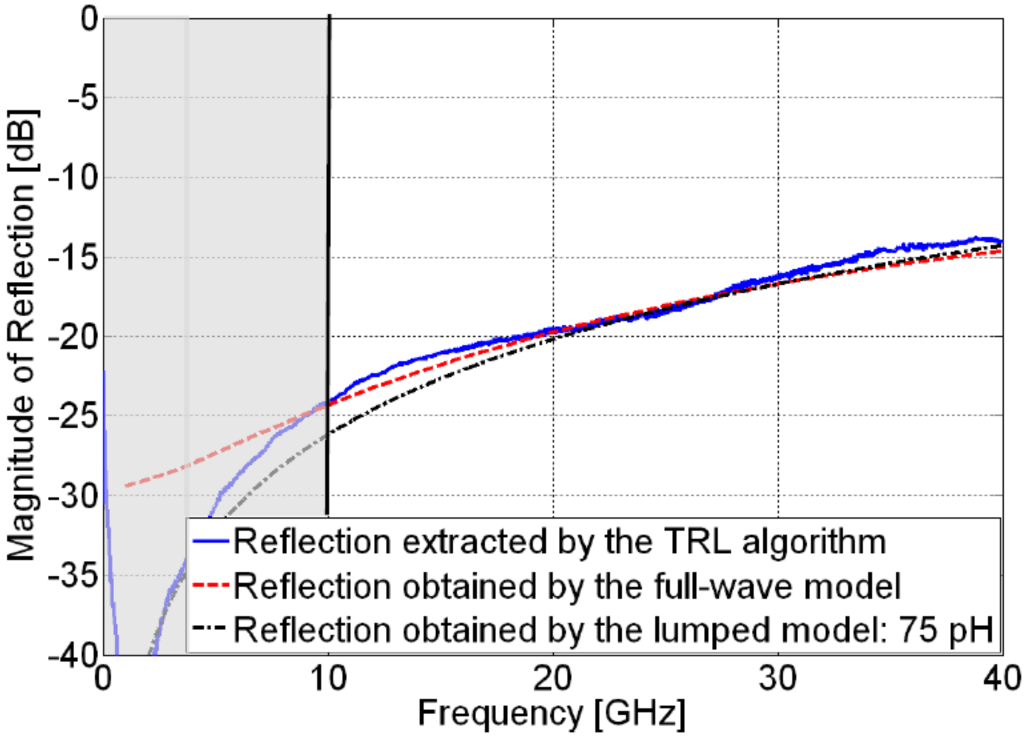


Figure 4.36 The extracted reflection parameters of the measured RPL correlate well in the calibration bandwidth between 10 GHz and 40 GHz. The S-parameters obtained from the full-wave model are related to the stripline impedance which corresponds to 48 Ω. The lumped model parameters are also normalized to 48 Ω [14].

4.6.2. Effect of Probe Placement

In the next step, sensitivity of the electrical performance of the RPL to probe tip positioning is studied with the help of the full-wave model depicted in Figure 4.35. This investigation represents a realistic scenario where due to the skating of the microprobe, the probe tips can contact the exposed stripline either closer to the stripline end or to the milled face of the cavity. As depicted in Figure 4.37 the -20 dB limit of the RPL is extended by 14 GHz in comparison to the nominal probe positioning (blue circles) when the probe is connected closer to the milled edge (+4 mil shift) and thus far from the stripline end. Comparing the reflections from the connection closer to the stripline end (-2 mil) and close to the milled edge (+4 mil) a -20 dB bandwidth variation of 18 GHz can be seen. Thus, when performing the measurements of the TRL calibration standards one has to precisely position the probe tips to reduce the effect of probe placement variations. These results show that the probe placement has a noticeable effect on the launch performance.

4.6.3. Effect of Cavity Size

The effect of the variations of the milled cavity was investigated with the full-wave model (Figure 4.35) and the obtained results are illustrated in Figure 4.38. As expected in case of the shorter coplanar waveguide-to-stripline transition (-4 mil shift in y-axis) the launch bandwidth is extended by 6 GHz. In Figure 4.39, two launches are shown where the exposed coplanar waveguides differ in length. The step response of these launches measured with microprobes is shown in Figure 4.40, where the launch A with longer coplanar waveguide-to-stripline transition represents the larger discontinuity of 65 pH. In order to achieve the best launch performance, the goal of the milling might be to remove less than 50% of the ground via barrels in y-axis. Thus the length of the CPW region can be minimized in order to reduce the CPW-to-stripline mismatch (the PCB is optimized for stripline impedance, the grounded CPW formed by cavity milling has higher characteristic impedance than this of the stripline) and to improve the launch measurement bandwidth (launch B, 29 pH). In practice, this is limited by mechanical tolerances between via drill placement and trace geometry and the need for probe skating.

4.6.4. Effect of Stripline Stub and Ground Plane Reference

In [7] it was found, that stripline ends should be kept short (Figure 4.41) and that u-straps (both ground vias are connected by a metallic shape in the form of a “u” to ensure connection of GS probe configuration, Figure 4.42) and further ground vias do not affect the RPL bandwidth. Single-ended striplines - each 978 mil long - that had “identical” RPLs at each stripline end had been measured in the frequency range from 10 MHz up to 40 GHz using a 2-port vector network analyzer (Anritsu 37397D). Microprobes with 225 µm pitch (signal-to-ground distance, GGB Picoprobe Model 40A

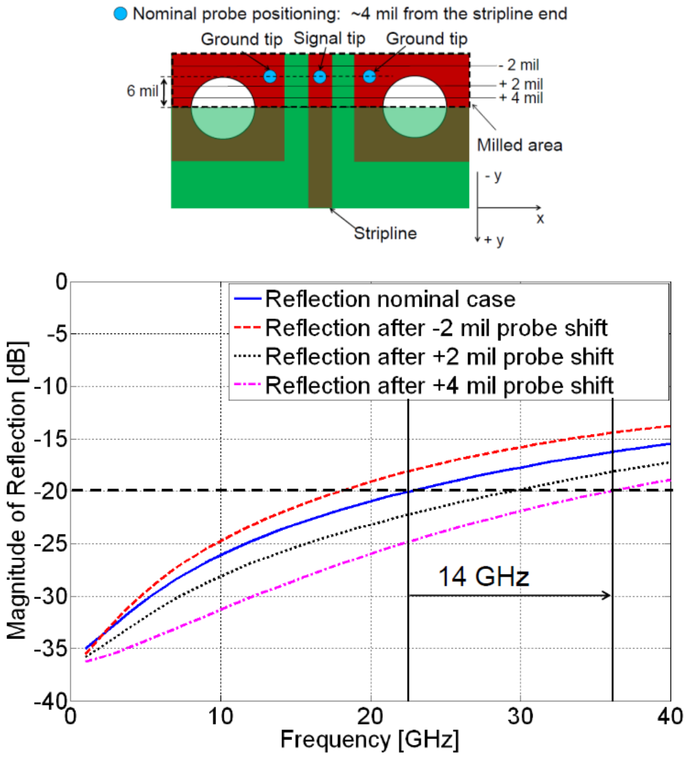


Figure 4.37 Reflection parameters computed with the full-wave model [113] showing the dependency on the probe positioning. Considering the nominal case (-20 dB at 22 GHz) when the microprobe tip is placed closer to the not exposed stripline region the -20 dB bandwidth limit is extended by ~14 GHz [14].

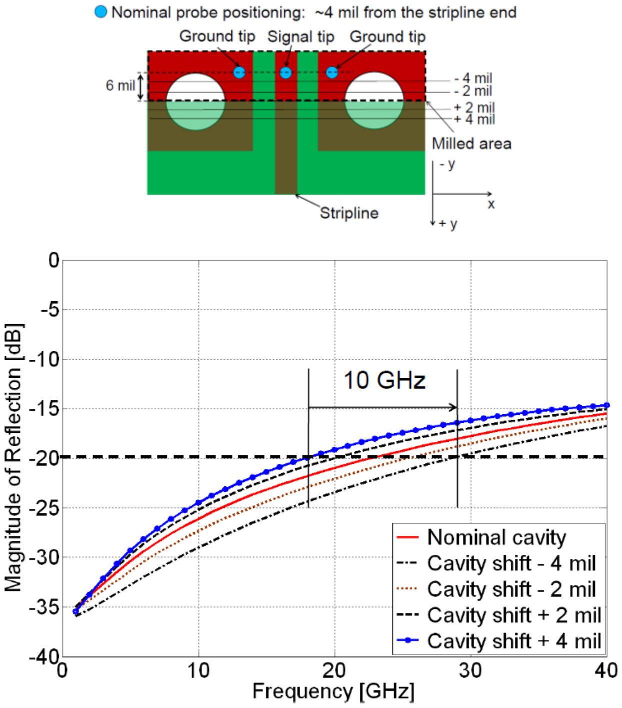


Figure 4.38 Reflection parameters computed with the full-wave model [113] showing the dependency on the milled cavity shift. Considering the nominal case (-20 dB at 22 GHz) when the milled region is reduced in y-axis, the launch bandwidth is extended by approximately 6 GHz [14].

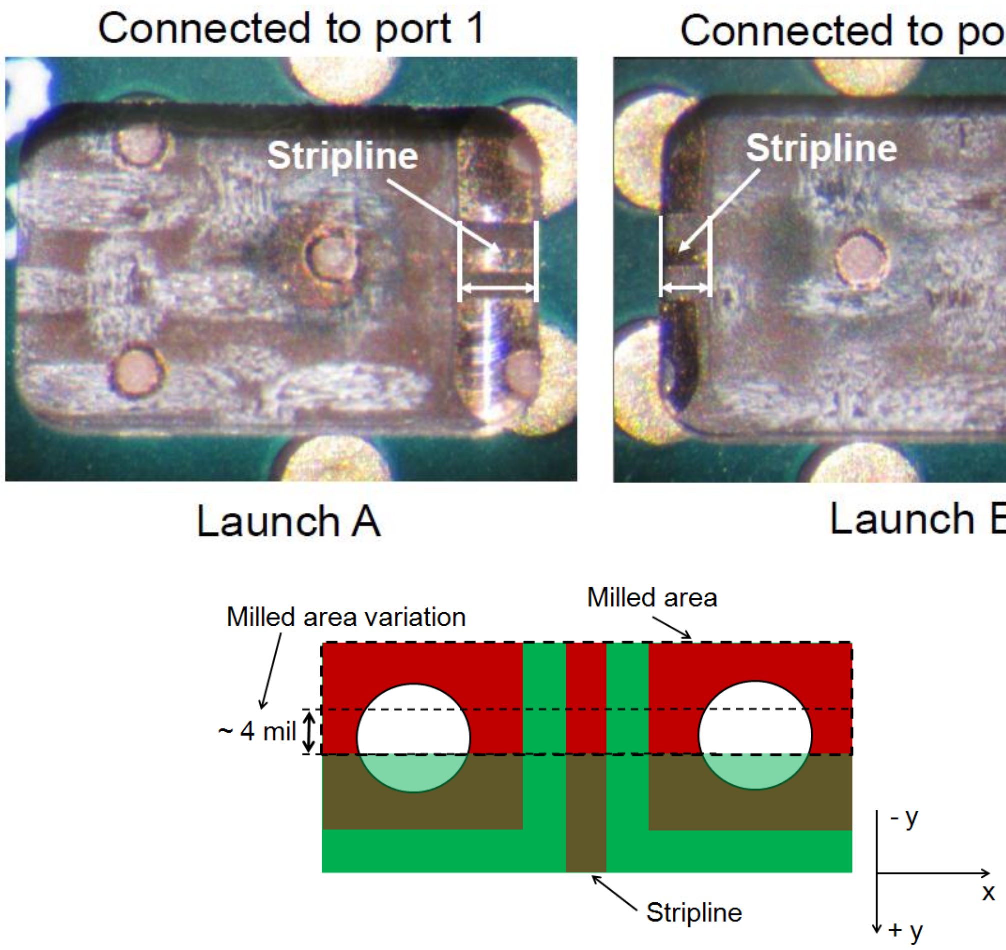


Figure 4.39 Milled cavity variations on the designed test board. Here, the 250 mil long line standard cavities are shown. In the left cavity the exposed stripline (microstrip) is approximately 4 mil longer than the stripline end in the right cavity [14].

DS-style GSG-225) had been applied to the single-ended measurements of the implemented launch variations. A 2-port Short-Open-Load-Thru calibration (SOLT) was performed prior to the measurements using the calibration standard (CS-5, [24]) provided by the microprobe manufacturer for reduction of the probe parasitics present in the measurement data.

Here, further investigations are performed to fully explore the dependencies of the RPL on the stub length and the ground plane reference. With the help of full-wave models, the effect of the stripline stub seen in the measurements is reproduced considering the nominal RPL (Figure 4.35) where only the stub length is varied and parameters as the probe positioning and milled cavity size are kept constant. As can be seen from the reflection parameters (Figure 4.43) the best launch performance is obtained in case of the 15 mil longer stripline stub. This is in agreement with the theory that the open stub behaves capacitively and thus is expected to compensate the

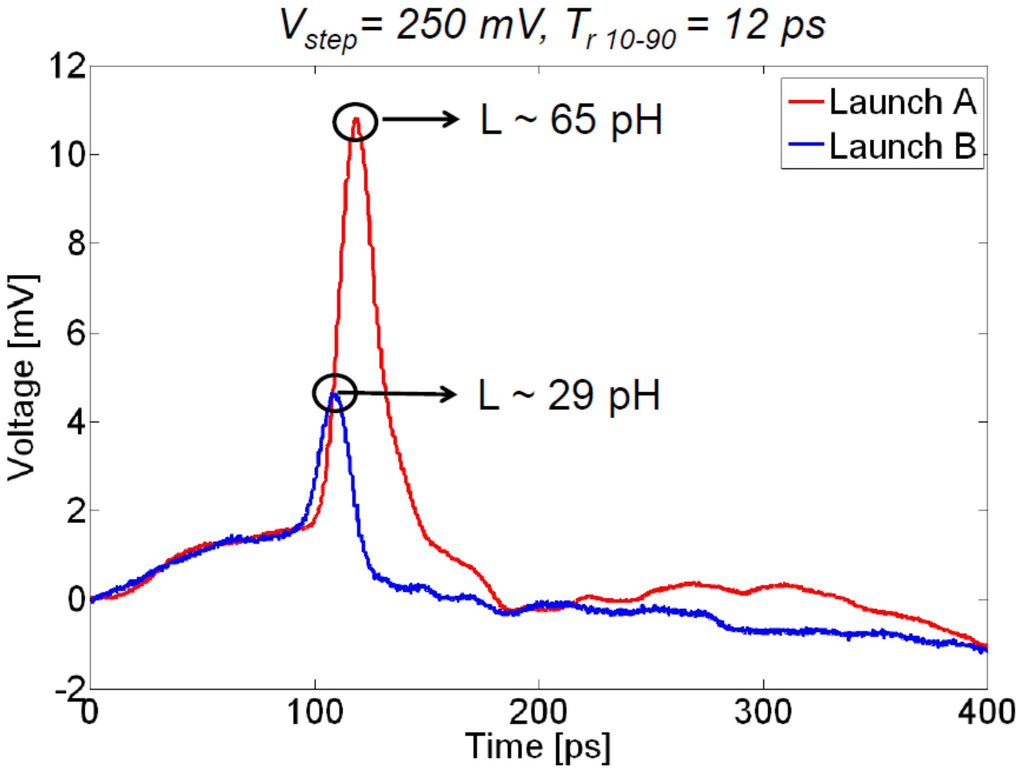


Figure 4.40 Step responses of two RPLs obtained with a time domain reflectometry. The launch B with shorter microstrip-to-stripline transition behaves less inductive [14].

inductive behavior of the RPL in a certain frequency bandwidth depending on the stub length. The simulation model with 30 mil long stripline stub has shown that indeed excessively long stripline stubs reduce the applicable bandwidth of the RPL. In comparison, the initial results obtained from the microprobe based measurements have shown that the stripline ends should be kept as short as possible in order to achieve the best launch performance (-27 dB from DC up to 40 GHz, [7]). Our current explanation is that in the measurements not all sensitivities were under control, but it is clear the RPL is sensitive to stripline stub variations and that an appropriate stripline stub length might improve the RPL measurement bandwidth. Furthermore, the design of an RPL with appropriate stripline stub length represents a complex problem due to the fact that the launch performance also depends on the probe placement and the milled cavity size, as shown in previous Sections.

The effect of adding additional ground vias and an “u”-strap on the RPL end were explored with help of the full-wave model (Figure 4.35). As illustrated in Figure 4.44, the launch bandwidth is less sensitive to these modifications. Adding two additional ground vias or a “u”-strap does not improve the launch performance. Similar results were obtained from the microprobe measurements of the modified RPLs. As depicted in Figure 4.42 the launch measurement bandwidth up to 40 GHz is not materially affected by these enhancements [7].

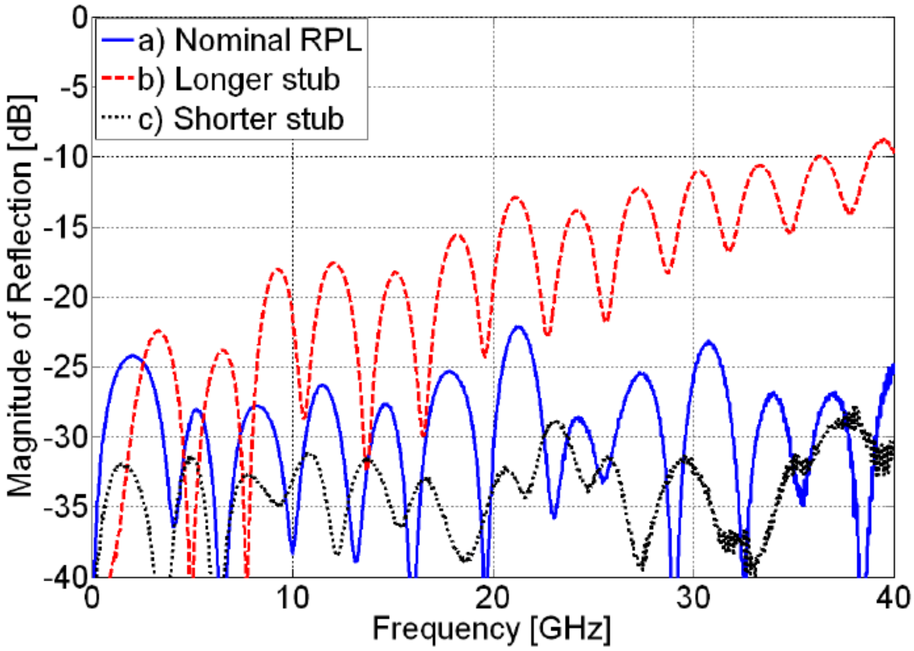


Figure 4.41 Measured reflection coefficients of the RPL configurations (978 mil long striplines that had identical RPLs at each end) with different stub lengths as presented in [7]. The beneficial effect of having a shorter stub can be seen. The longer stripline stub degrades the launch performance

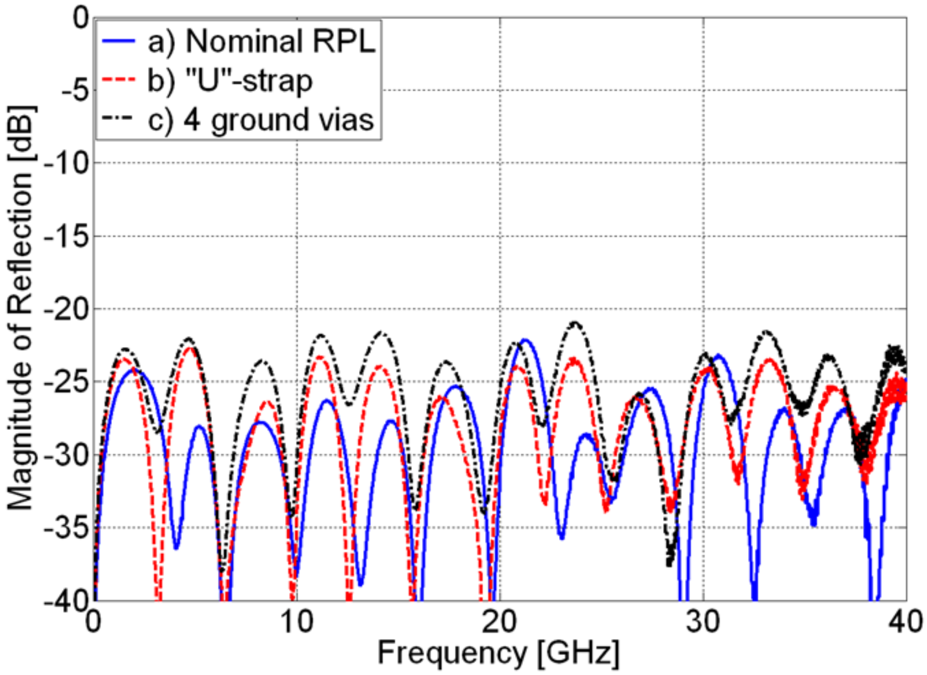


Figure 4.42 Measured reflection coefficients of the RPL configurations (978 mil long striplines that had identical RPLs at each end) with “u”-strap and two additional ground vias as presented in [7]. Obviously, no beneficial effect of having “u”-strap or using more ground vias can be seen.

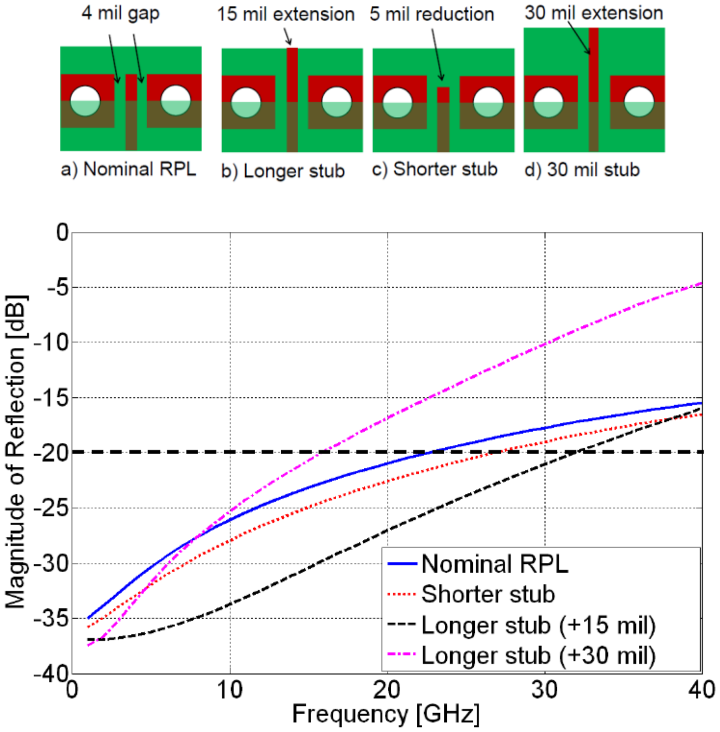


Figure 4.43 Computed reflection coefficients of the RPL configurations with different stripline stub lengths using full-wave models [113]. In the case of the 15 mil long stub the best launch performance is achieved [14].

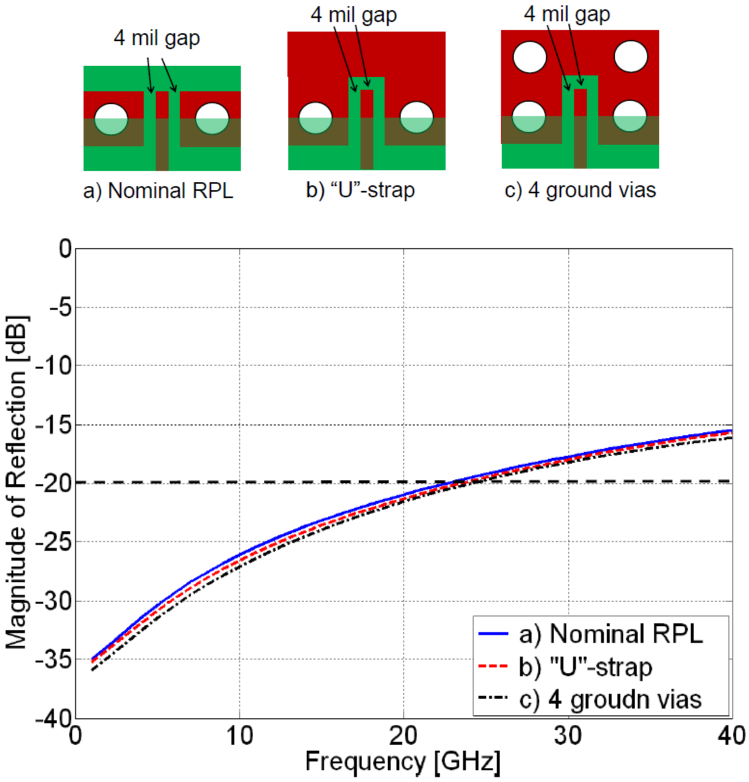


Figure 4.44 Computed reflection coefficients of the RPL configurations with "u-strap" and two additional ground vias using full-wave models [113]. No beneficial effect of having "u"-strap or using more ground vias can be seen [14].

4.6.5. Effect of Microstrip Width

In [108] a suggestion for the bandwidth extension of the RPL was made. By using larger ground pads on the signal layer (increasing the trace capacitance by decreasing the gap size) the probe parasitics were compensated and the measurement bandwidth was extended by approx. 12 GHz. As presented in the previous Section, the RPL contains a typical coplanar waveguide-to-stripline transition. Similar scenarios were investigated previously and can be found in the literature (e.g. [114] - [116]) with the difference that the designs are mainly applicable to limited bandwidth applications and the return loss of -20 dB is typically not required. Here, using the techniques shown in [114], [117] - [120] an RPL with smoother transition from the CPW (coplanar waveguide) and the stripline for the entire bandwidth up to 40 GHz was designed. In Figure 4.45 the dimensions of the optimized RPL and the computed S-parameters obtained by the modified full-wave model are shown (Figure 4.35). For this launch the milled cavity has to be larger and patterning of the fine 1 mil gap is problematical. Hence, two additional ground vias are needed to ensure better return current paths and to reduce the loop inductance. As can be seen for S_{11} (Figure 4.45), the -20 dB limit is not exceeded in the frequency bandwidth up to 40 GHz and for the transmission a maximum loss of -0.83 dB at 40 GHz is obtained.

4.6.6. Effect of Port Type Excitation

As discussed in [108] the launch behavior is affected by the microprobe tip configuration: GS or GSG (Figure 4.46). Obviously, when GS probes are applied to the RPL the -20 dB limit is reduced. The best launch performance is obtained when the launch is excited by lumped ports. This is an indicator that the RPL performance is affected by the probe tip parasitics even if it has been calibrated prior to that. These parasitics can be reduced if the microprobes are calibrated on the same substrate used in the RPL design. As mentioned for the measurements, the microprobes were calibrated on the alumina substrate CS-5 ($\varepsilon_r = 9.8$). In Figure 4.47 an approach for extension of the RPL measurement bandwidth is suggested where the microprobe tip is modified using 10 mil extension of low loss dielectric material ($\varepsilon_r = 3.5$, $\tan\delta = 0.003$). With help of this modification the reflection is kept below -20 dB without any optimization of the launch design in the entire bandwidth up to 40 GHz and the maximum transmission loss of -0.46 dB is obtained (Figure 4.48).

4.6.7. Transmission Characteristic of the Embedded RPL

The embedded RPL was investigated applying full-wave 3D models in [23]. For the studies here the launch was modified adding quadratic ground pads which can improve the probe skating. Results from the influence of the gap size on the link transmission characteristics are shown in Figure 4.49. As expected, the return loss increases when the via to line separation decreases. For a 4 mil gap the maximum reflection at 40 GHz

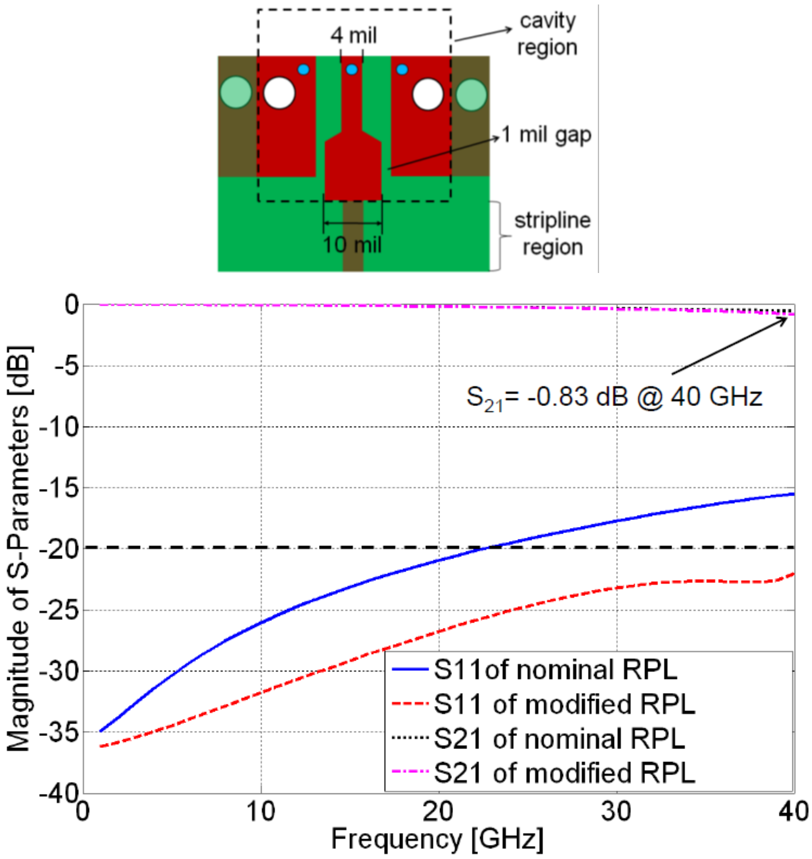


Figure 4.45 S-parameters of the optimized recessed probe launch computed with a full-wave model [113]. The -20 dB limit is not exceeded over the entire bandwidth up to 40 GHz. The maximum insertion loss of -0.83 dB is obtained at 40 GHz [14].

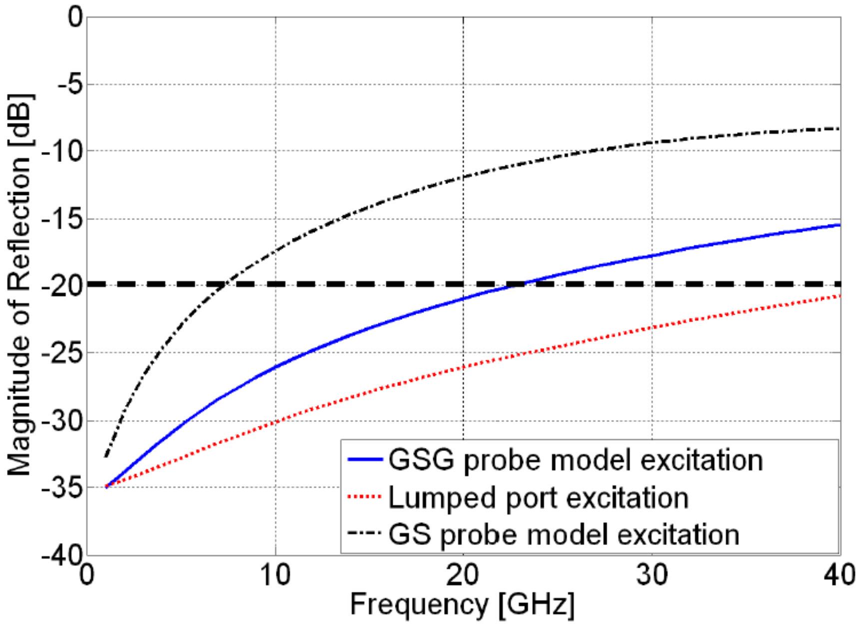


Figure 4.46 S-parameters of the same RPL computed with different port excitations. The best launch performance is obtained when using lumped port excitation where parasitic effects from the microprobe are not taken into account. The RPL is best suited for measurements with GSG microprobes [14].

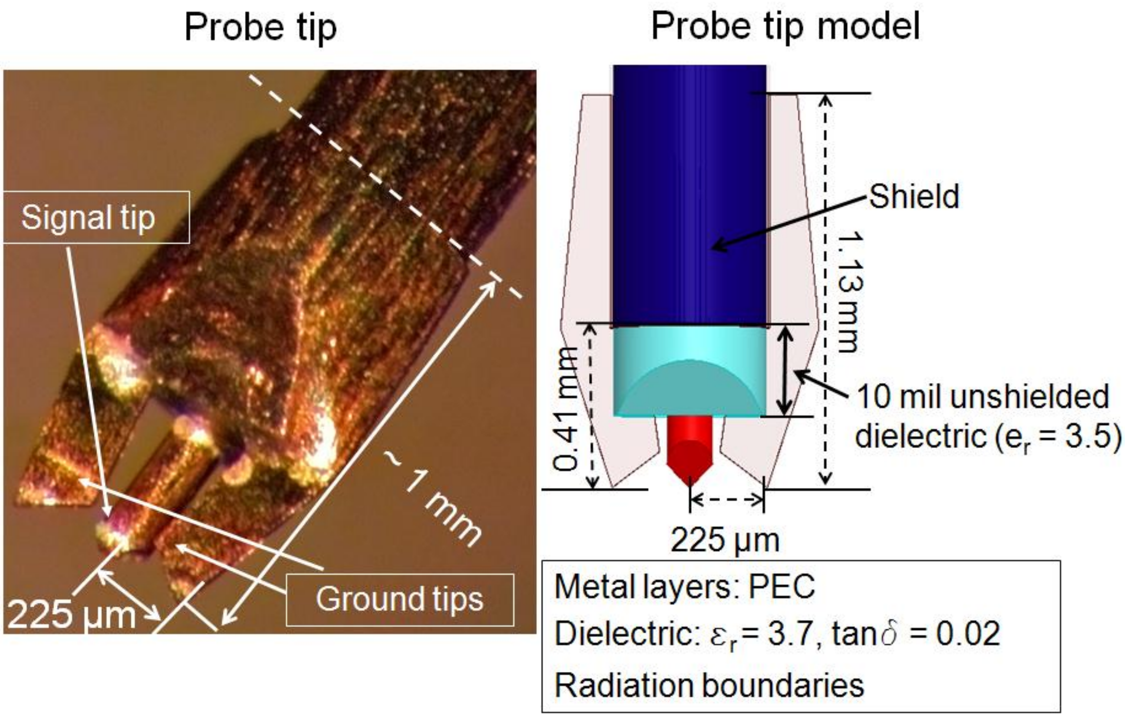


Figure 4.47 On the left: Picture of magnified GSG-probe tip with a 225 µm signal-to-ground pitch. On the right: Modified GSG probe tip used for the extension of the RPL applicable bandwidth [14].

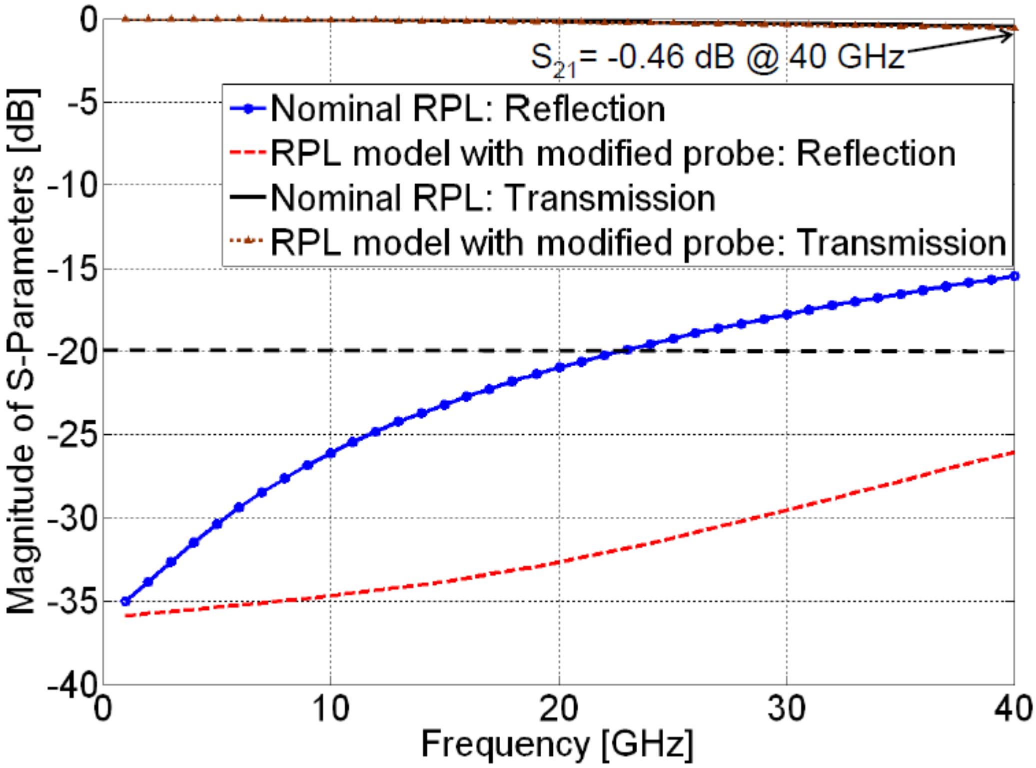


Figure 4.48 Computed S-parameters obtained by using the modified microprobe model and not optimized RPL. The -20 dB limit is not exceeded over the entire frequency range up to 40 GHz. A maximum insertion loss of -0.46 dB is obtained at 40 GHz [14].

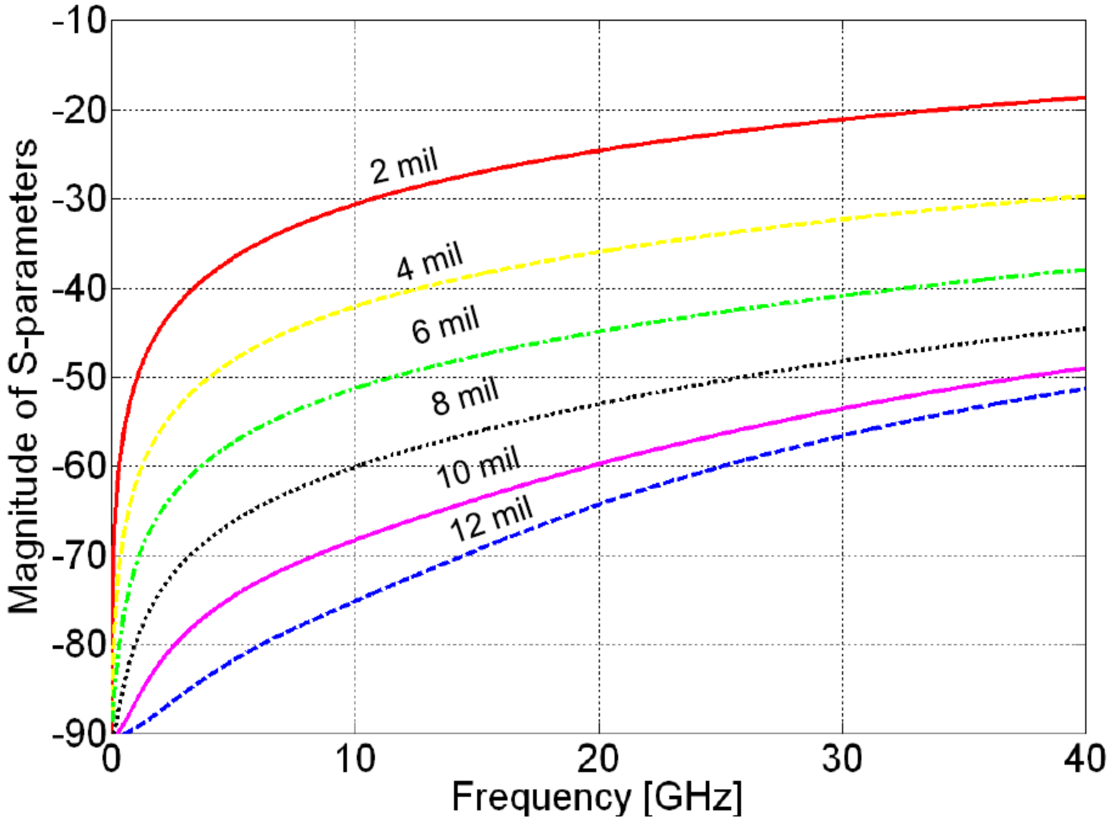


Figure 4.49 Reflection of a continuous link depending on the gap between the quadratic ground pad and the stripline. Obviously, when increasing the gap the reflection decreases [23].

is below -28 dB, which is acceptable considering the fact that maximum reflection of a 50 Ohm transmission line at the quarter wavelength resonance frequency corresponds to -20 dB by manufacturing tolerances of ±10 %.

In the next Section, results from the application of the recessed probe launch to the measurement of a single stub via and of stripline structures are shown.

4.7. Comparison to Measurements

In order to illustrate the electrical performance of the RPL applied to realistic measurement scenarios, this Section presents measurements of a single stub via on a multilayer PCB (18 metal layers, $\varepsilon_r = 3.7$, Figure 4.50). For these measurements, GSG-microprobes were used which were calibrated between 10 MHz and 40 GHz on an alumina substrate (CS-5, $\varepsilon_r = 9.8$, [24]) using an SOLT calibration algorithm. On the same PCB, TRL calibration standards with RPLs were designed and measured using the same probe calibration in order to extract the effect of the RPLs from the measured S-parameters of the single stub via using de-embedding. A comparison of the single stub via measurement with and without de-embedding of the signal launches is shown

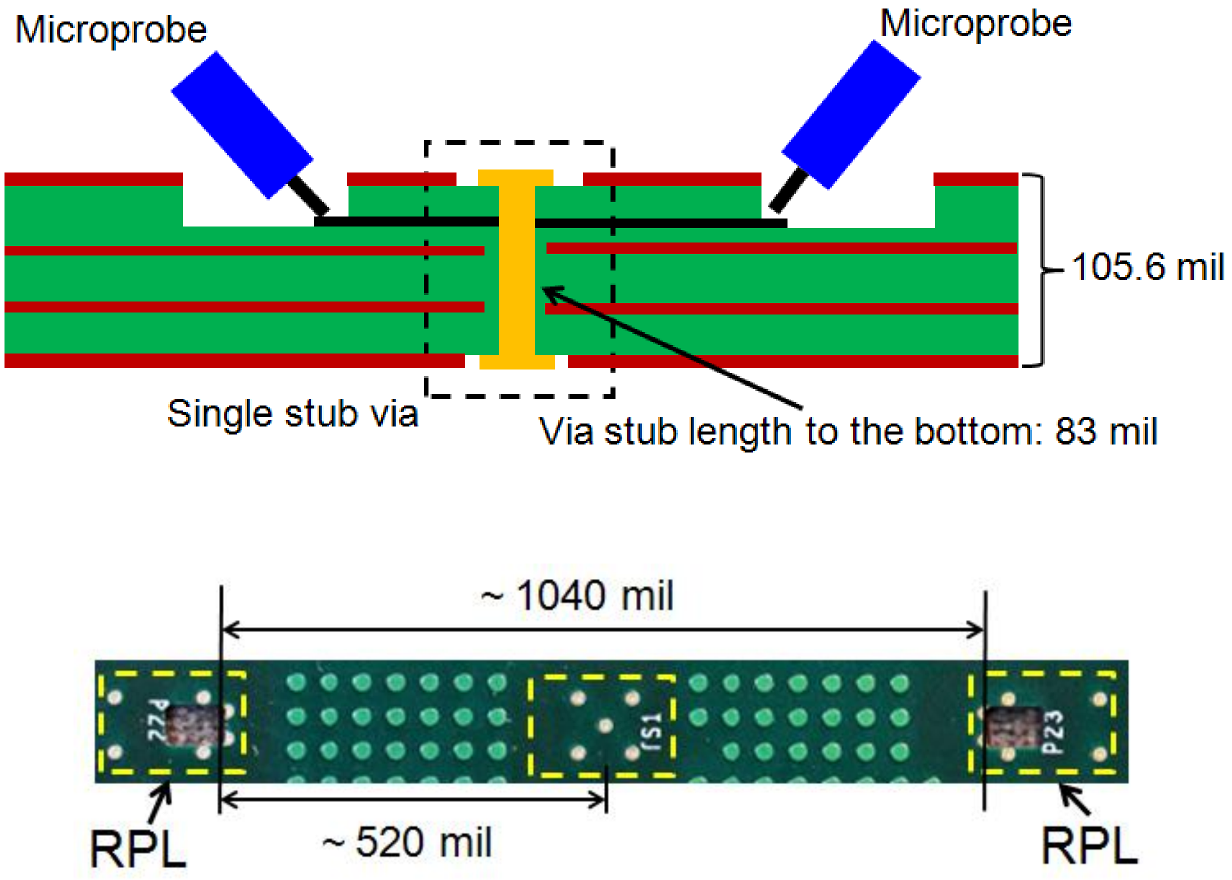


Figure 4.50 Sketch of measurement set up. A single stub via is surrounded by 4 ground vias in a multilayer PCB (18 metal layers, $\varepsilon_r = 3.7$). The via stub effect is measured using two RPLs [14].

in Figure 4.51 and Figure 4.52. The effect of the via stub can be clearly seen in the measured transmission parameters. The stub resonance appears in form of the deep notch (additional notches are expected at the odd harmonics). Differences in the S-parameters are obtained for the bandwidth beyond 20 GHz. For the reflection parameters, the resonances at 32 GHz and 36 GHz are less distinctive after de-embedding of the RPLs. In order to explore this, a so called “embedding” was performed (additional parasitic inductances of 40 pH were added to the RPLs). The transparency of the RPL was explored in case of the single stub via (Figure 4.50) where the RPL performance was degraded by embedding of 40 pH at both RPLs (Figure 4.53). In this scenario, the transmission characteristics of the stub via dominate the frequency response and the eye opening is reduced mainly by the via stub.

These investigations show that the RPL technique can be used for most digital (broadband) applications even without the need of launch de-embedding. If it is desired to extend the measurement bandwidth, the signal launches have to be de-embedded/calibrated and in this case the issues shown in Section 4.3 will play a role again.

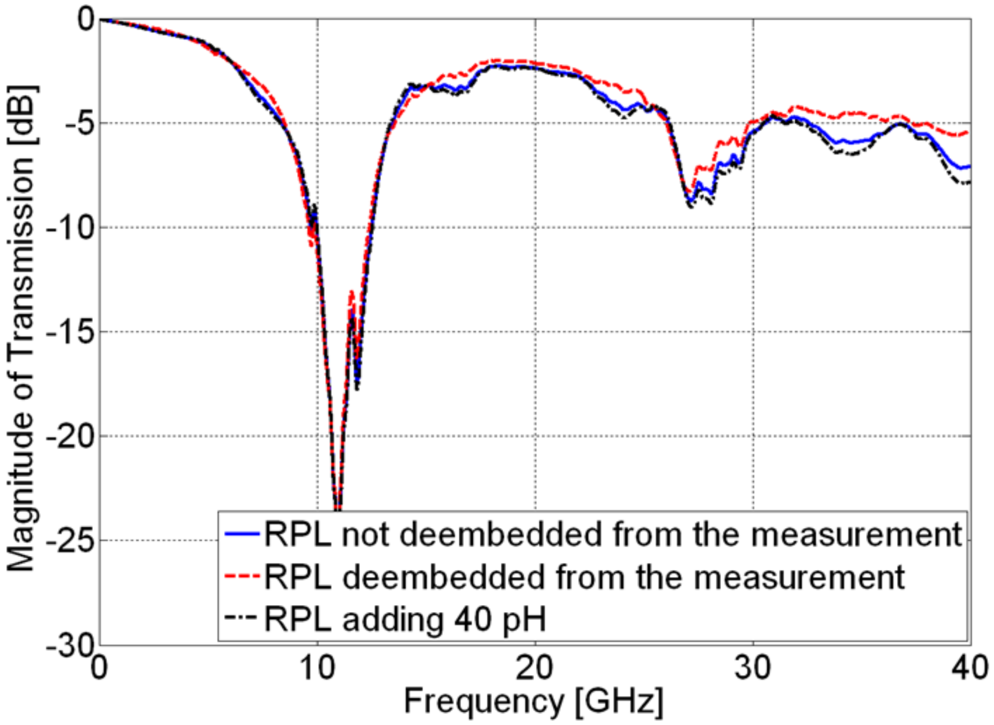


Figure 4.51 Comparison of transmission parameters of a single stub via obtained by measurement applying the RPL technique. The effect of de-embedding the launch is more distinctive for the bandwidth beyond 20 GHz. The embedding (adding) of 40 pH to the RPLs degrades the transmission characteristics beyond 20 GHz [14].

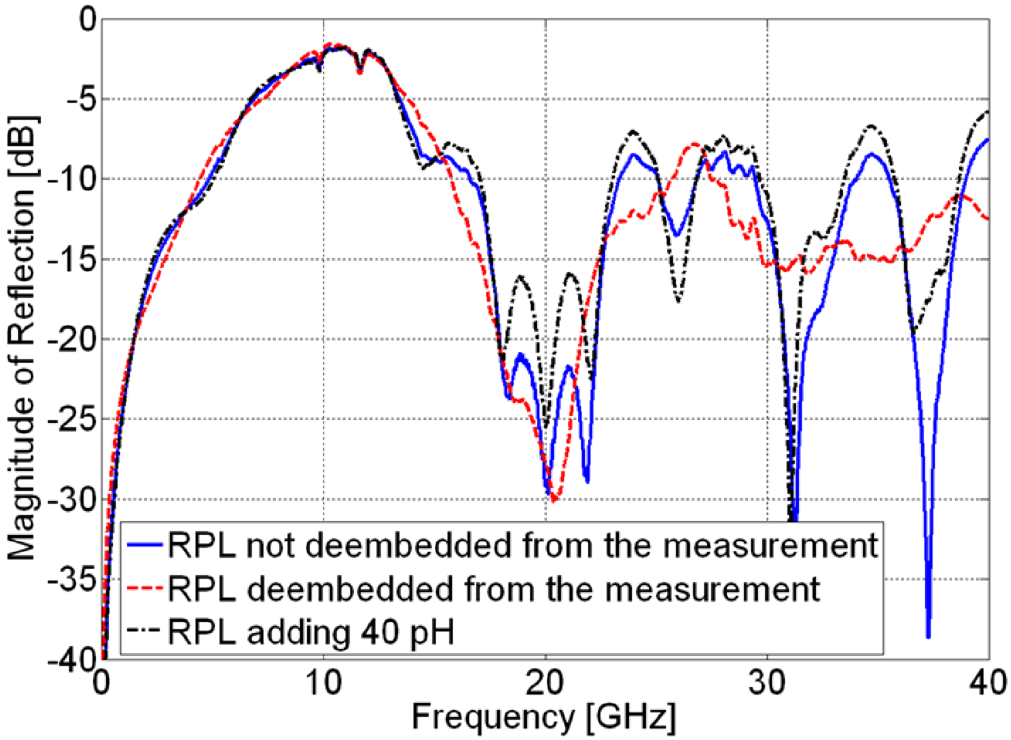


Figure 4.52 Comparison of reflection parameters of a single stub via obtained by measurement applying the RPL technique. The effect of de-embedding the launch can be clearly seen in the bandwidth beyond 20 GHz. The embedding (adding) of 40 pH to the RPLs degrades the via response in the bandwidth beyond 19 GHz [14].

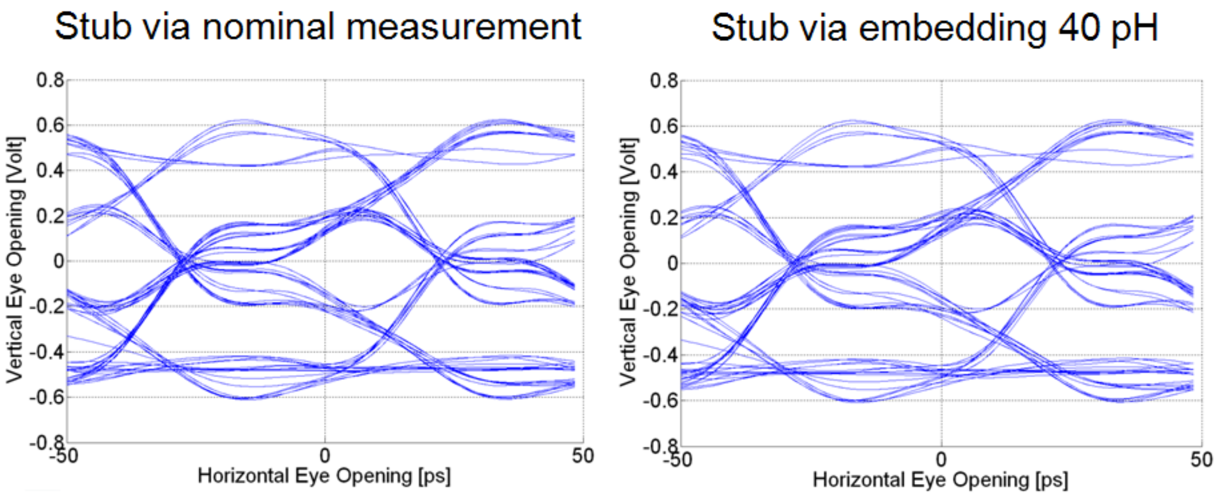


Figure 4.53 Eye diagrams calculated from the transmission parameters of the single stub via measured with microprobes. A 256 bit pseudo random binary signal with a data rate of 20 Gbit/s and 10 ps rise time was used for the calculation. The eye diagram is not influenced even if the RPL performance is degraded by embedding (adding) of 40 pH to both RPLs [14].

4.8. Summary

In this Chapter, some alternative microprobe based measurement techniques applicable to crosstalk investigations of dense via array structures have been studied. For this purpose, conventional one- and two-tier calibration procedures were used applying commercial and custom-made calibration substrates. The obtained results were compared to S-parameter data computed with full-wave 3D models where adequate correlation up to 40 GHz was achieved.

In addition, the comparison of different calibration procedures have shown that the two-tier mixed calibration method using the proposed multilayer custom-made substrates presents an alternative procedure for these where commercial alumina substrates were used in the bandwidth up to 30 GHz. In order to extend the applicable bandwidth of the multilayer substrates, for manufacturing of the proposed terminations more precise soldering technique and reduction of the PCB manufacturing tolerances are needed. As presented for the bandwidth below 30 GHz, the probing technique using the custom-made substrates is more preferable for measurement set ups where the test boards have been mounted vertically.

The attempt for calibration of on-surface microprobe launches with access via stubs using TRL calibration algorithm failed in the area of via stub resonance frequencies and the calibration in the full bandwidth was not reliable. The manufacturing tolerances and the total reflection at the via stub resonance have been detected as possible reason for that behavior.

Previous investigations of the RPL technique pointed out that the launch behaves mainly inductive. Using the TRL calibration technique and dedicated calibration standards S-parameters of the designed RPL were extracted and correlated to ones computed by full-wave 3D models. Good correlation was obtained in the calibration bandwidth between 10 GHz and 40 GHz. Based on these results, the models were used for characterization and validation of electrical performance of the RPL. Using the step response approximation, the parasitic inductance of the RPL has been estimated. For the nominal RPL (Figure 4.35) it corresponds to approx. 42 pH (voltage step = 1 V, $t_{r20\text{-}80}$ = 10 ps). Applying the same procedure to the S-parameters obtained from the investigations of the other launch dependencies, the observed variations of the launch inductance were as follows:

- stripline stub length (Figure 4.43): parasitic inductance between 35 pH and 10 pH,
- probe positioning (Figure 4.37): parasitic inductance between 50 pH and 23 pH,
- cavity size (Figure 4.38): parasitic inductance between 50 pH and 32 pH.

Based on these results and the time domain measurements (Figure 4.40) the launch parasitic inductance is expected to be in the range of 40 pH ± 25 pH for the geometries and GSG probe tip configurations investigated within the frame of the work.

The application of the proposed RPL to single stub via measurements let one to conclude that the suggested RPL might even be used with data rates up to 20 Gbit/s without requiring de-embedding.

5. Custom-Made Interposer for Multiport Measurements

In Chapter 2 some typical measurement issues and challenges in dense via arrays were discussed. In this Chapter, a novel multiport probing fixture for high frequency measurements of such dense via array structures is presented as a possible solution. The mechanical set up and custom-made clamping hardware needed for proper positioning of the probing fixture are described. Using a two-tier calibration technique and custom calibration substrates, error parameters for the probing fixture are extracted and used to de-embed them from measurements of digital links. The S-parameters of digital links obtained with the probing fixture are then compared to S-parameters measured using commercial RF microprobes. Full-wave models are used for validation of the electrical performance of the designed interposers. Layout modifications are suggested for improvement of the measurement bandwidth.

The layout and the manufacturing of the presented interposers were done by the High-Speed I/O Subsystems and Packaging Group at the IBM T. J. Watson Research Center, Yorktown Heights, New York, USA.

5.1. Measurement Challenges in Dense Via Arrays

Dense via arrays located under chip packages and in backplane connector footprints route hundreds to thousands of signal and power traces in very close proximity where the crosstalk between adjacent channels can become the main factor limiting reliable signal transmission on multilayer PCBs [11], [121] - [123]. Due to their complex crosstalk behavior, dense via array structures appear as the bottleneck in high speed digital link systems and thus require careful attention during link design [124]. Typically, package engineers tend to use low-loss dielectrics, smooth copper, innovative via-hole techniques and new connector technologies [92], [125] in order to extend the link bandwidth. With the help of 3D full-wave and/or semi-analytical models, dense via array structures are explored under different scenarios to identify the key bandwidth limitation issues [17], [126].

For validation of the simulation results, multiport measurements of test structures are needed as shown in Chapter 2 (Figure 2.2). As discussed there, simultaneous physical access to adjacent vias in a dense array can be problematical. Typically, test

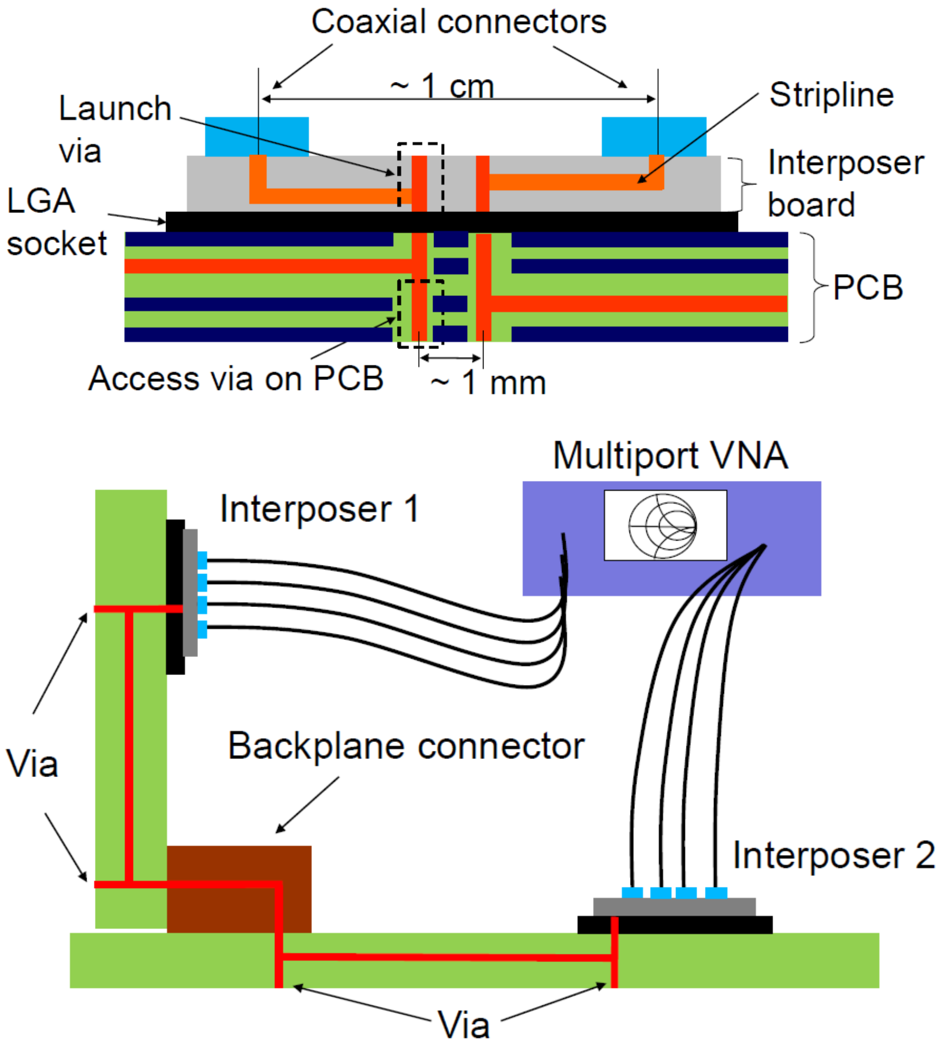


Figure 5.1 The concept of the probing fixture: A signal pitch transformation from 1 cm to 1 mm is needed when the test signal is launched by surface mounted connectors on a multilayer printed circuit board [15].

signals from e.g. a multiport VNA are launched into the DUT (device under test) using either surface mounted connectors or RF microprobes contacting the vias directly. Nevertheless, commercial cable end reliefs, microprobe configurations and dedicated DUT dimensions often present spatial restrictions when multiport measurements have to be performed in dense via structures. In this Chapter, a novel probing fixture is presented which ensures the connections of up to 12 measurement ports and additionally overcomes these spatial restrictions when signal launching in tightly packed via arrays (e.g. 1 mm pitch) is desired.

The idea of a multiport probing fixture (interposer) is illustrated in Figure 5.1. As can be seen for the signal pitch conversion from approximately 1 cm to 1 mm a multilayer interposer with surface mounted coaxial connectors on its top side connected to launch via array is used. The interposer is plugged in a land grid array (LGA) socket which ensures the signal transition from the access via array to the test structure underneath. A typical measurement scenario is shown where two interposers are applied to a digital link measurement (Figure 5.1). Results from similar application of the interposer to digital link measurements are shown later on in Section 5.7.

The following Sections elaborate on this multiport probing fixture. The mechanical set up and the design of the interposer were presented for the first time in [13], [15]. A description of the calibration hardware and de-embedding procedure needed for the extraction of the measurement fixture from the measurements were presented there. Initial results from the electrical performance analyses of the interposer and comparison to microprobe based measurements of digital links were shown in [13]. In the last Section of this Chapter some design modifications are suggested which might improve the measurement bandwidth of the interposer structure.

5.2. Layout and Mechanical Set up

Two basic designs of the 12-port interposer were implemented on a multilayer printed circuit board with SMP (SubMiniature Push-on) and SMA (SubMiniature version A) connectors on the top side (Figure 5.2 and Figure 5.3); they shared the same stack-up: 20 metal layers (12 ground planes and 8 potential signal layers which were labeled as S3, S5, S7, S9, S12, S14, S16, S18 going from top to bottom) using Nelco N4000-13 (ε_r = 3.7, tanδ=0.008, [104]) as the dielectric. The difference between the two types of interposers are the connector type on the top board side, the length of the signal traces routing the test signal to the access via arrays, and the signal layers utilized in the multilayer PCB. On the SMP interposer the test signals are routed on signal layers 7 (S7) and 9 (S9) in contrast to the SMA where signal layers 3 (S3) and 5 (S5) are used (Figure 5.4). The different signal levels were required in order to mill cavities that were used to accommodate the land grid array (LGA) socket. The LGA socket used for the signal transition from the interposer to the device under test is shown in Figure 5.5. As can be seen there, the socket consists of a plastic frame (36 mm x 36 mm) within which 1155 metal loaded elastomeric buttons are located on a 1 mm grid. The socket is centered on the test board by two precision metal locating pins on two opposite corners. The inner dimensions of the socket are the same as those of the probing fixture (36 mm x 36 mm).

The SMP interposer is shown in Figure 5.2 with 12 top side SMP adapters present which are connected through access vias to the striplines on the appropriate signal layers. The signal traces are routed to the 12 through vias (signal vias) in the launch via array in a manner that attempts to minimize coupling. The launch via array consists of 10x10 vias (88 ground and 12 signal through vias) on a 1 mm grid. The footprint of the launch via array is shown in Figure 5.2. As depicted, the signal-to-signal pitch of two adjacent signal vias is either 2 mm in a row/column or 1.46 mm in a diagonal.

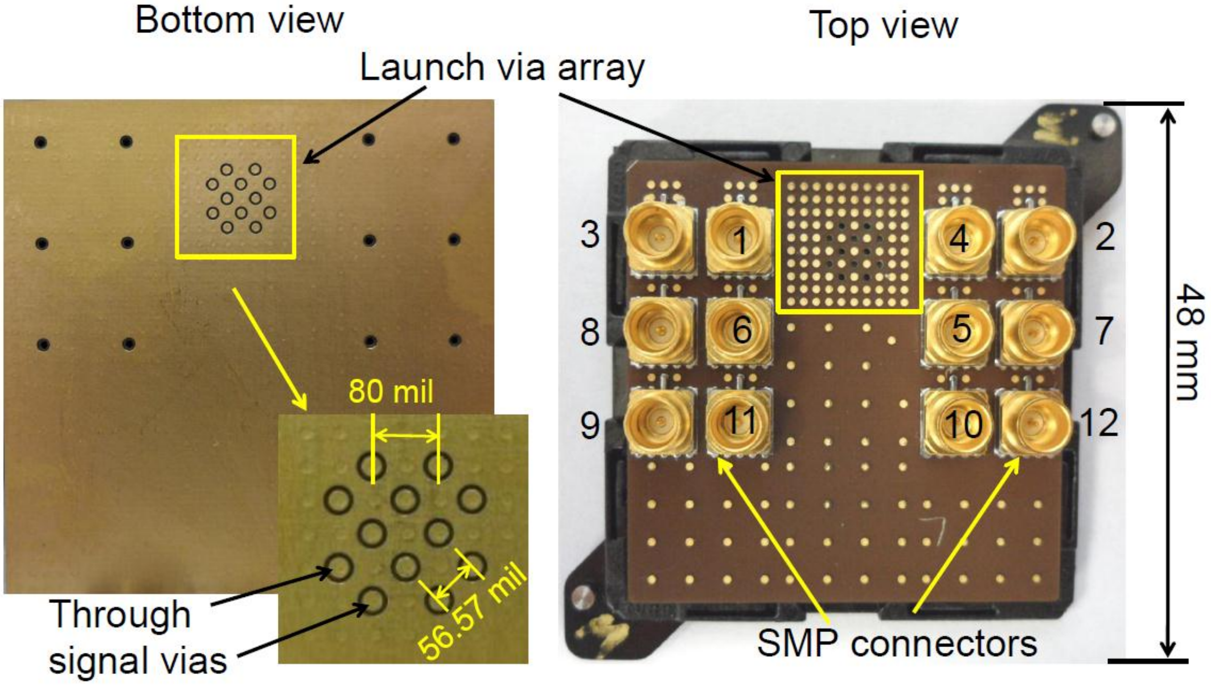


Figure 5.2 Bottom and top view of a 12-port probing fixture: the SMP connectors are connected by striplines to the launch via array in the middle of the edge of the multilayer printed circuit board. The minimum signal pitch is 56.56 mil in a diagonal and 80 mil in a column/row [15].

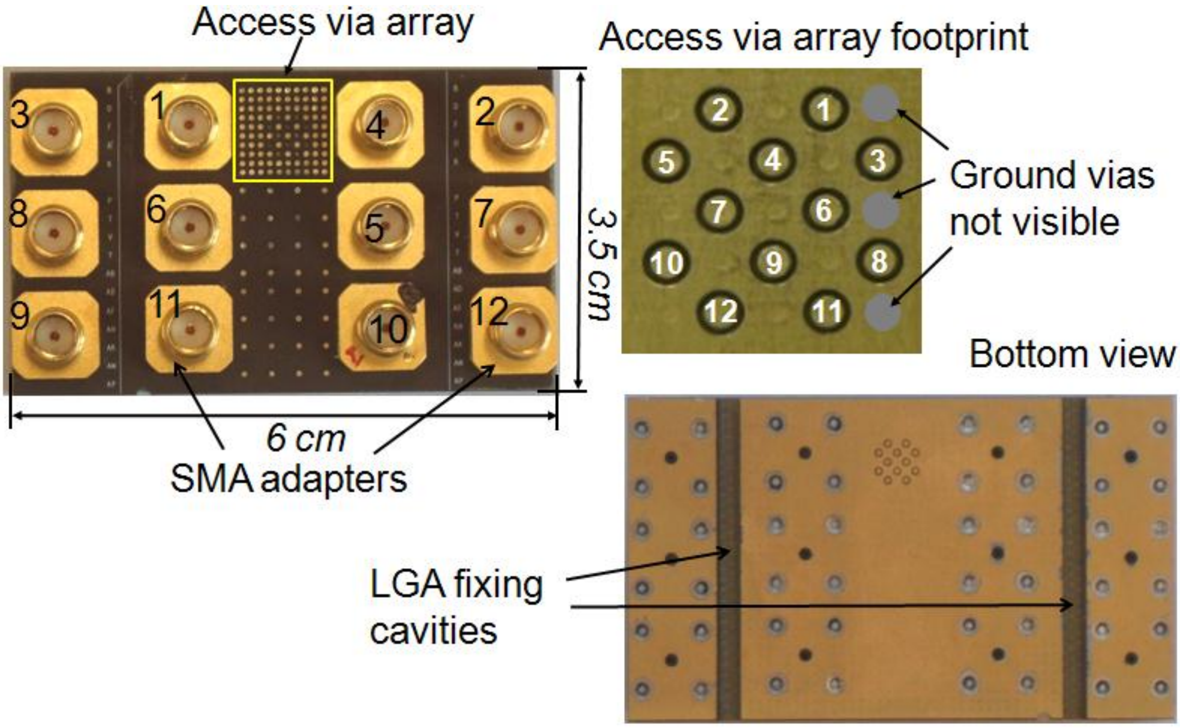


Figure 5.3 12-port SMA interposer with an access via array in the middle of the upper board edge. On the bottom side two cavities are milled to enable mating of the interposer into the LGA socket. The signal pitch is the same as for the SMP interposer [13], [15].

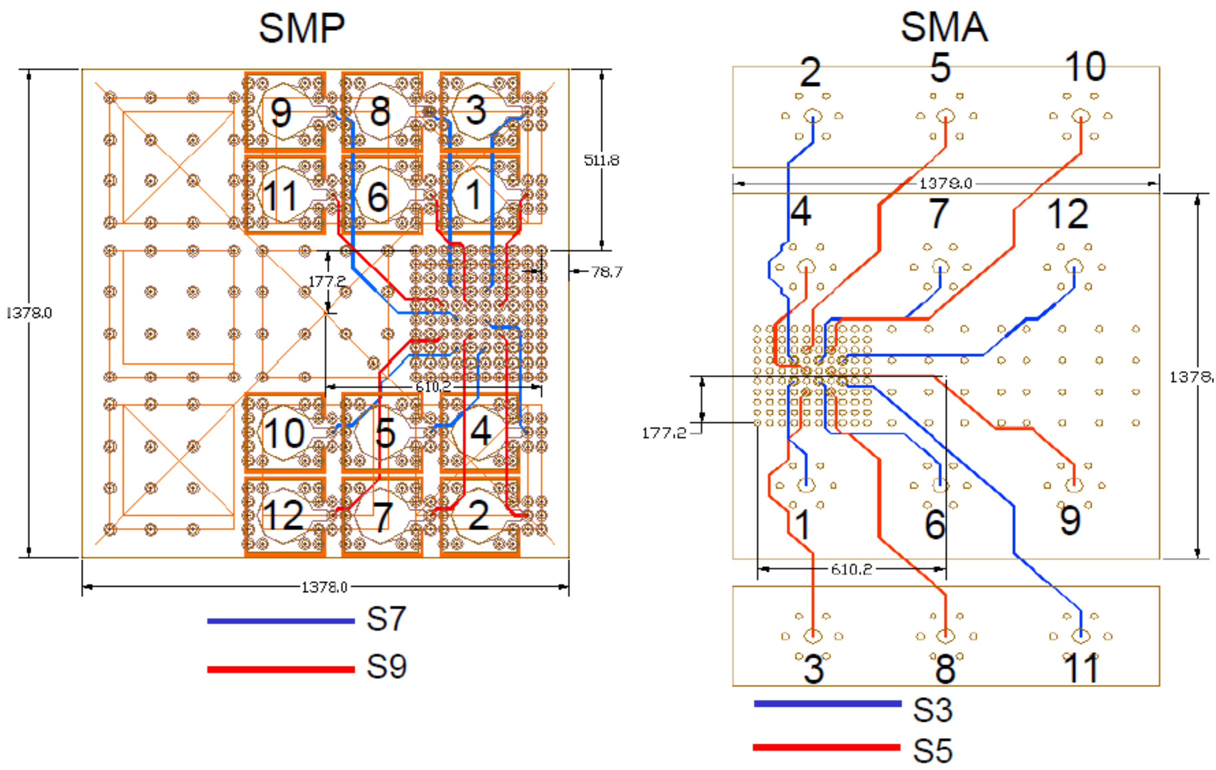


Figure 5.4 Layout of an SMP and SMA interposers with the access via array in the middle of the edge of the PCB. In case of the SMA interposer the upper signal layers S3 and S5 are used. Due to the dimensions of the SMA connectors the interposer board is larger than the SMP board [13], [15].

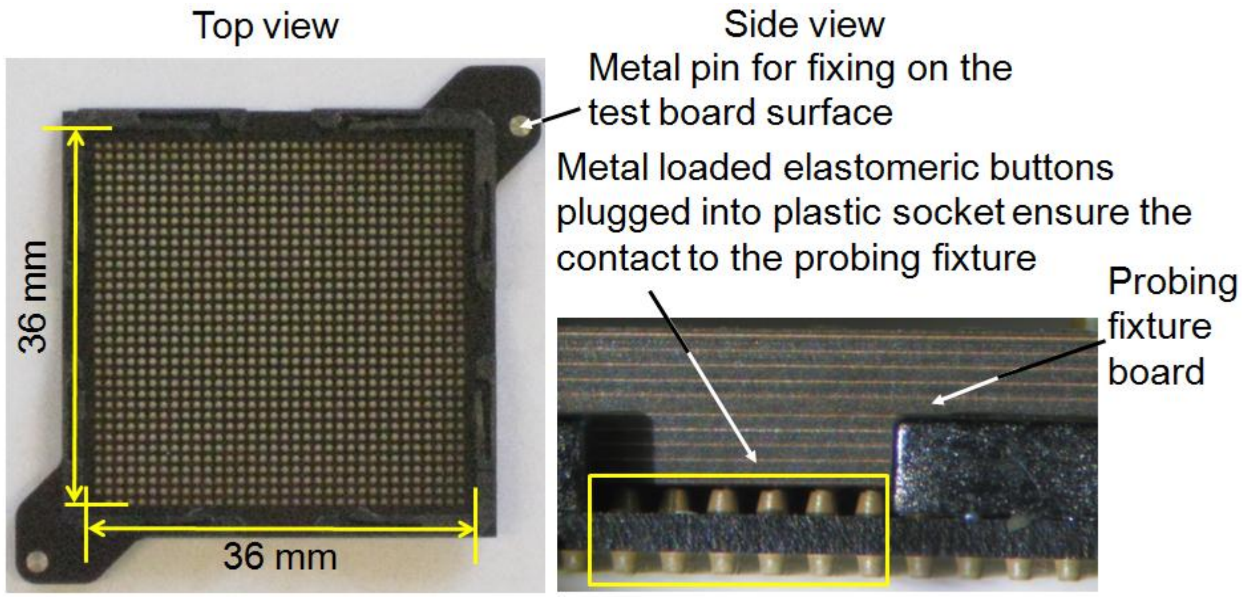


Figure 5.5 The Land Grid Array (LGA) contains 1155 pins in a 1 mm grid plugged into a plastic frame. The socket pins ensure the transition of the test signals from the probing fixture to the device under test [15].

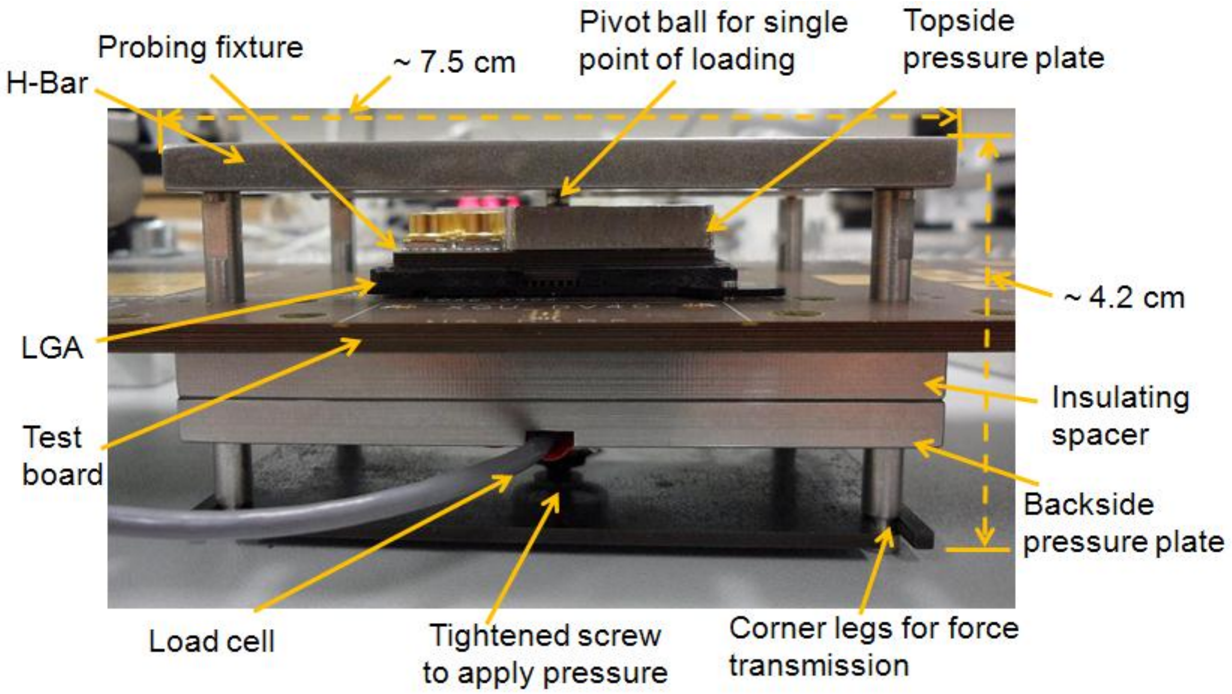


Figure 5.6 Mechanical set up of an SMP interposer connected to a test board. Mechanical pressure is applied by a screw on the bottom plate (7.5 cm x 5.5 cm) and transmitted to the top H-bar by a four corner legs, from the top the force is forwarded by a metal ball to another pressure plate (7.5 cm x 5.5 cm) placed on the interposer which is plugged into the plastic frame of the LGA [15].

An SMP interposer clamped down to a test board is depicted in Figure 5.6. As illustrated there, a compression screw on the bottom plate is used to apply pressure to the clamping hardware. The four corner legs transmit this force through clearance holes in the test board to a metal plate (H-bar) on the top side. The H-bar conveys this force through a small metal pivot ball which accommodates angular tilt to a pressure plate sitting on the top surface of the interposer and thereby pressing it into the LGA socket. A load cell between the back side pressure plate and the compression screw measures the total applied pressure to prevent overloading of the LGA socket. According to the vendor data sheet, the recommended loading force is in the range between 35 and 75 grams per contact [127].

It is obvious that this set up represents a difficult mechanical challenge and careful placement of all components is required in order to ensure consistent force distribution on the bottom of the LGA socket. Another effect that is expected when connecting the interposer to via array structures and the measurement cables is the mechanical expansion of the LGA plastic frame. In order to improve the robustness of the shown set up, the investigations have shown that depending on the number of the applied measurement ports and the PCB thickness a larger pivot ball might be very helpful.

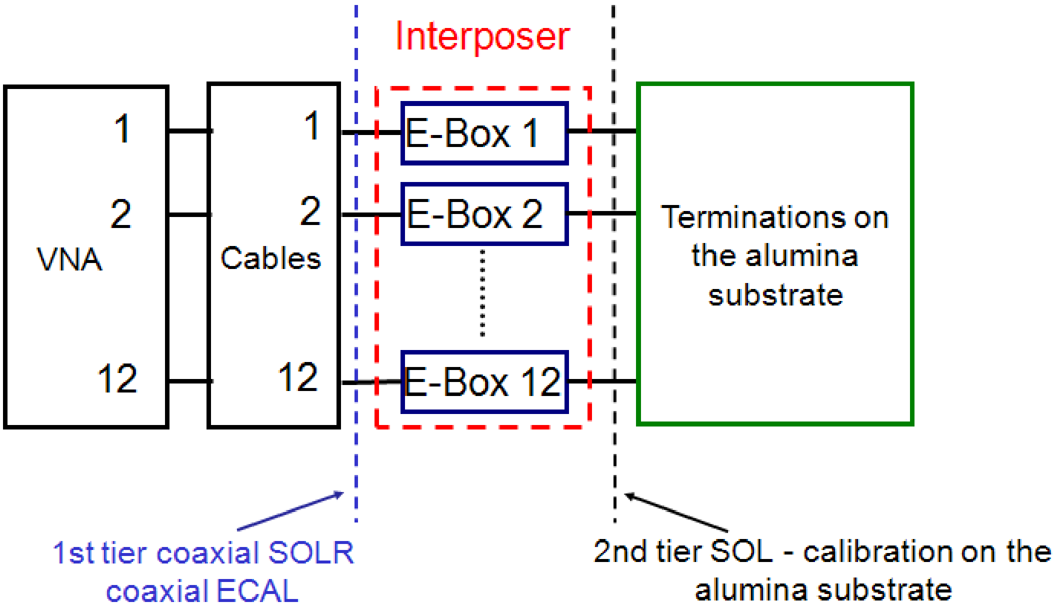


Figure 5.7 Two-tier calibration procedure for de-embedding the interposers from the measurements: For the 1st tier a coaxial SOLR [64] with an electronic calibration module is used. For the 2nd the custom-made substrates are measured with the interposers and applied to an SOL calibration algorithm [15].

5.3. Calibration Hardware

In order to remove the effect of the probing fixture on measurements, custom-made calibration substrates have been designed for its calibration. A two-tier calibration procedure (shown in Figure 5.7) first uses a coaxial electronic calibration module and a Short-Open-Load-Reciprocal (SOLR, [64]) calibration algorithm to remove the effect of cables and the VNA (Vector Network Analyzer) on the measured S-parameter data. Then, for the second tier, a common Short-Open-Load calibration algorithm is applied [121], [128] and for the de-embedding of every error box a technique suggested in [105] - [107] is chosen which was used in [8], [10]. For this purpose the “short”, “open” and “load” terminations have to be measured with the interposers and used for the second calibration tier. In the following, the design of the custom-made terminations is presented and the results from the modeling and the microprobe based measurements needed for their characterization are discussed.

In Figure 5.8 the custom-made “load”, “open” and “short” terminations implemented on an alumina substrate (Al_2O_3, $\varepsilon_r = 9.8$) are depicted. The “open” termination represents an open annulus in a gold plane on the top side of the substrate; in case of the “load” termination this annular region is filled with thin film nichrome layer (200 Ohm/sq ± 20 %). The 12 terminations on the substrate are arranged in such way that the signal pins of the LGA socket can contact the small pads in the middle of each termination. In case of the “short” termination, a 3 µm thick solid gold plane is used.

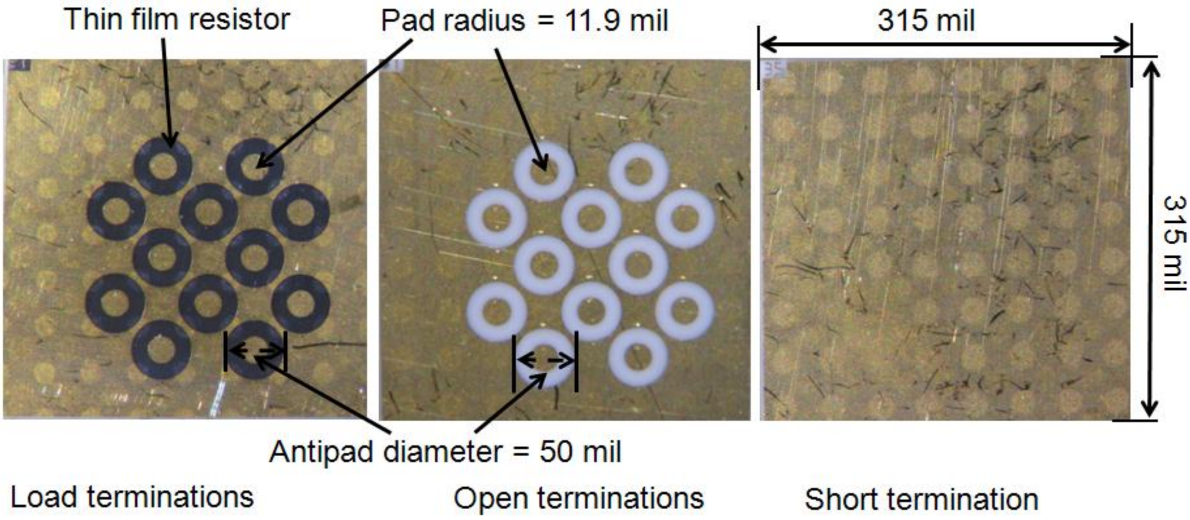


Figure 5.8 From the left to the right: Custom-made load, open and short terminations implemented on the alumina substrate (Al_2O_3, 20 mil thick, [132]). In case of the open terminations ring-shaped regions are cut out from the gold layer on the top substrate surface where in case of the load terminations the ring-shaped regions are filled with thin nichrome layer (200 Ohm/sq ±20 %) [15].

In order to de-embed the interposer from the measured data, the designed terminations have to be characterized by measurements and simulation models. Then the obtained S-parameters can be used as correction (expected) S-parameters for the SOL 2^{nd} tier calibration. The SOL algorithm requires good separation of the three standards needed for the computation of the measurement error induced by the probing fixture. Hence, before implementing the design of the three different terminations, they were investigated with help of the full-wave 3D models shown in Figure 5.9. In order to validate the expected S-parameters of the termination substrates two different port excitations were used: wave guide port on a 20 mil long coaxial extension and a 50 Ohm lumped port excitation. The initial goal for the design of the three standards was to obtain clear separation in frequency domain for the measurement bandwidth from 10 MHz to 20 GHz. As depicted in Figure 5.9 independent of the port excitation the reflection of the different terminations is clearly distinguishable for both types of port excitations.

In the next step, the designed terminations were measured with microprobes (Picoprobe Model 40A DS-style GS- and SG- 520 µm pitch) which were initially calibrated on an alumina substrate (CS-11, $\varepsilon_r = 9.8$, [24]) delivered by the microprobe manufacturer to reduce the effect of probe parasitics on the measured data. All 12 load terminations were measured and the expected variations due to etching and sheet resistance tolerances were found. In Figure 5.10 the reflection parameters of four pads on the “load” termination are shown wand a maximum difference of 1.7 dB between pads 2 and 10 was detected.

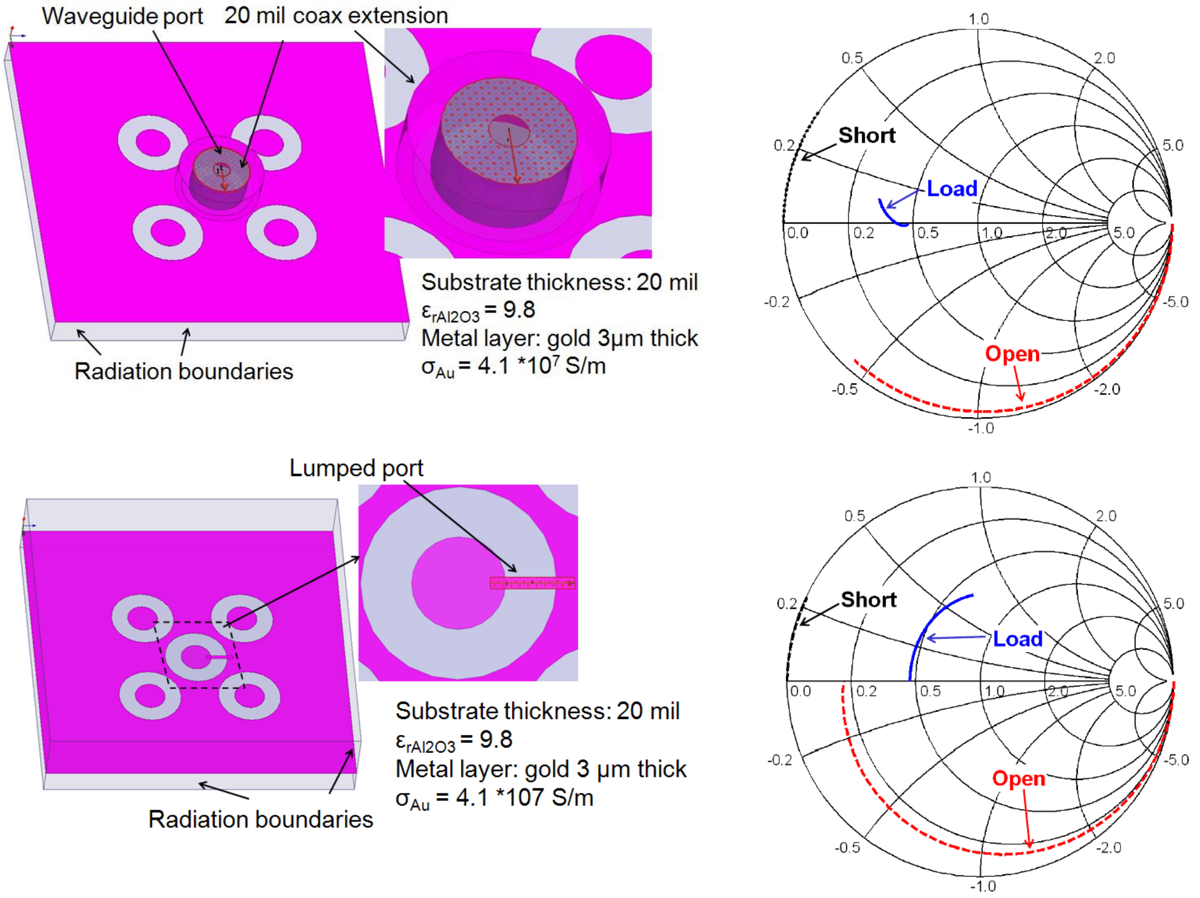


Figure 5.9 Full-wave 3D model of a termination standard. A 20 mil long coaxial extension or lumped port excitation is used for the computation of the expected substrate S-parameters in the bandwidth between 10 MHz and 20 GHz [15], [113].

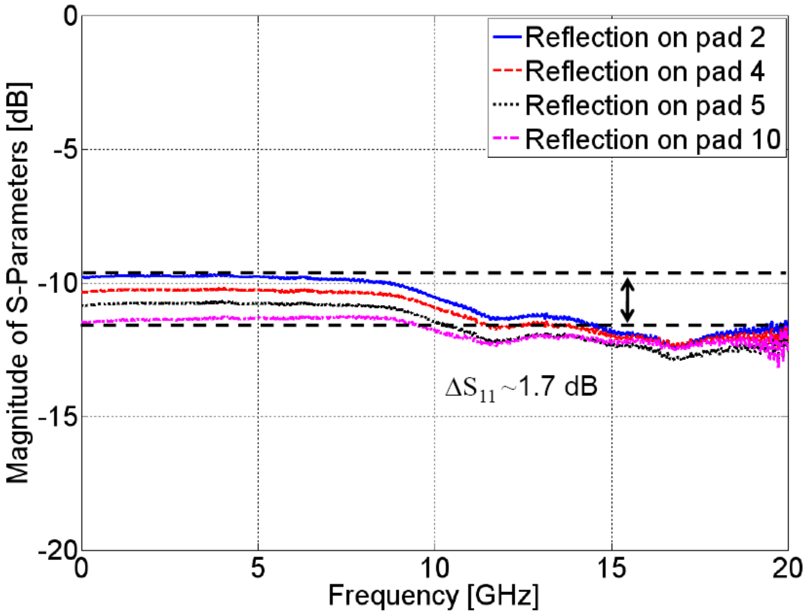


Figure 5.10 Reflection parameters of four “load” terminations obtained by measurements with microprobes. The manufacturing tolerances of the sheet resistance lead to variations of approximately 1.7 dB when comparing the reflection on pad 2 and pad 10 [15].

TABLE 5.1 DC RESISTANCE OF THE 12 TERMINATIONS ON THE DESIGNED CALIBRATION SUBSTRATE OBTAINED BY USING THE BIAS TEE PORT OF A VNA *

* The shorted probe tip delivers the DC resistance of the cable and probe (R_{short}) which is subtracted from the load terminated probe DC resistance (R) to obtain the DC resistance of the termination only.

Termination #21			
Pad Number	R [Ohm]	R_{short} [Ohm]	R - R_{short} [Ohm]
1	28.6	2.5	26.1
2	27.8	2.5	25.3
3	28.6	2.5	26.1
4	29.0	2.5	26.5
5	30.0	2.5	27.5
6	29.0	2.5	26.5
7	29.7	2.5	27.2
8	28.1	2.5	25.6
9	29.0	2.5	26.5
10	31.2	2.5	28.7
11	30.0	2.5	27.5
12	30.8	2.5	28.3

Additionally, the DC resistances of the 12 termination standards were measured with a microprobe (Picoprobe Model 40A DS-style SG-520 µm pitch) applied to one bias tee port of a VNA (Anritsu 37357D). To measure only the DC resistance of the implemented load terminations the microprobe was short circuited and thus the DC resistance of the bias tee, cables and probe were subtracted ($R_{short} = 2.5\ \Omega$). The results from this measurement method are summarized in Figure 5.11 where the variation in the measured DC resistance of the terminations amounted to 3.4 Ω. The DC resistance values are corroborated by RF measurements e.g. for pad 2 according to Figure 5.10 at 10 MHz a reflection of -9.7 dB which corresponds to reflection obtained from 25.3 Ω load. Similar correlation can be identified by considering the rest of the design terminations (pad 10, $S_{11} = -11.45$ dB, load resistance ~ 28.7 Ω).

According to the tolerances of the substrate manufacturing process [132] the thin film resistor is expected to be in the range of 200 Ohm/sq ± 20 %. Using the following formula an estimate of the DC resistance of the implemented load termination can be done [19]:

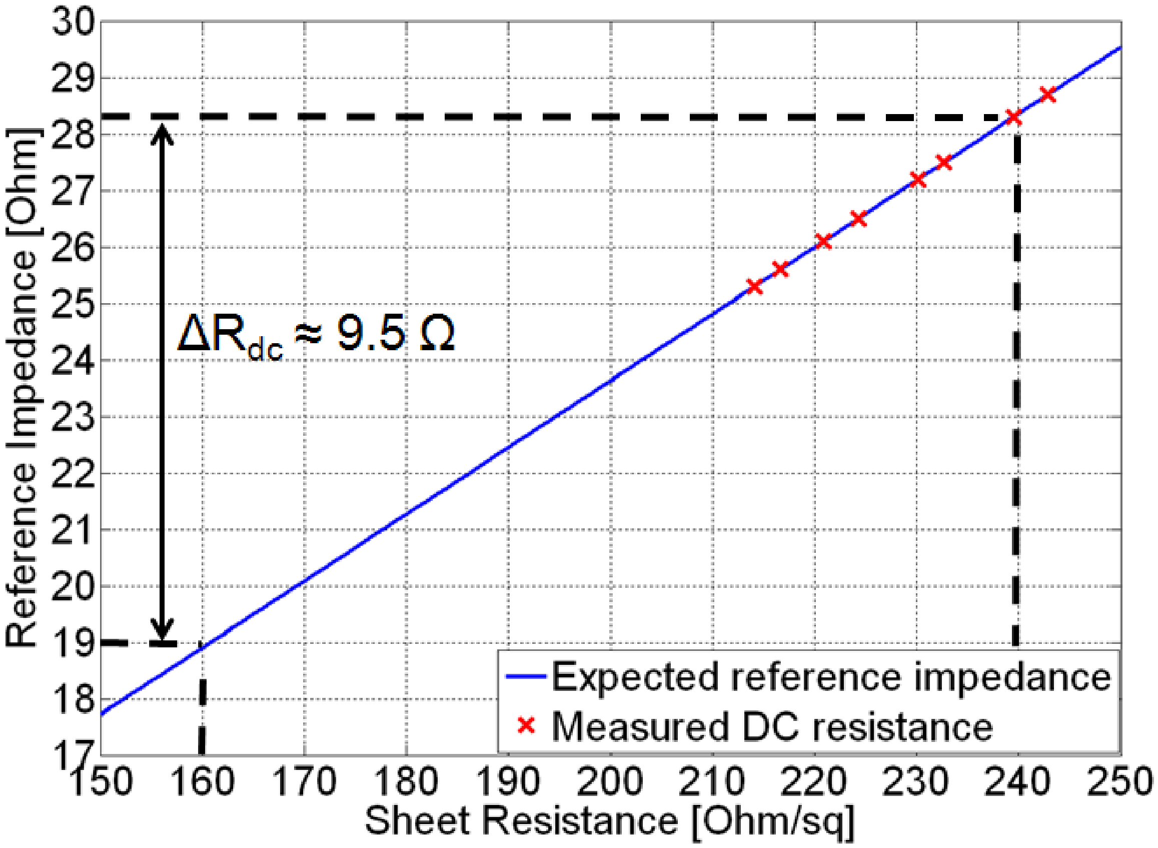


Figure 5.11 Expected variations of the DC resistance of implemented terminations on the alumina substrate considering the tolerances of the manufacturing process. The termination resistance could vary between 19 Ω and 28.4 Ω. The measured R_{DC} exceeds the expected maximum variation of the implemented terminations in the case of pad 10.

$$R_{sheet} = \frac{R_{DC} \cdot 2 \cdot \pi}{\ln\left(\frac{R_{outer}}{R_{inner}}\right)} \tag{5.1}$$

Assuming that the sheet resistance R_{sheet} corresponds to 200 Ω/sq, the inner pad radius $R_{inner} = 11.9\,\text{mil}$ and the antipad radius $R_{outer} = 25\,\text{mil}$ with respect to the maximum manufacturing tolerances of 20% for the thin film sheet resistor, one can obtain the upper and lower limits expected for the DC resistor from its nominal value (Figure 5.8). As shown in Figure 5.11 the R_{DC} varies between 19 Ω and 28.4 Ω which let one to conclude that every load standard has to be measured separately for obtaining its correction coefficients to be used later on for the calibration algorithms as explained in the next Section.

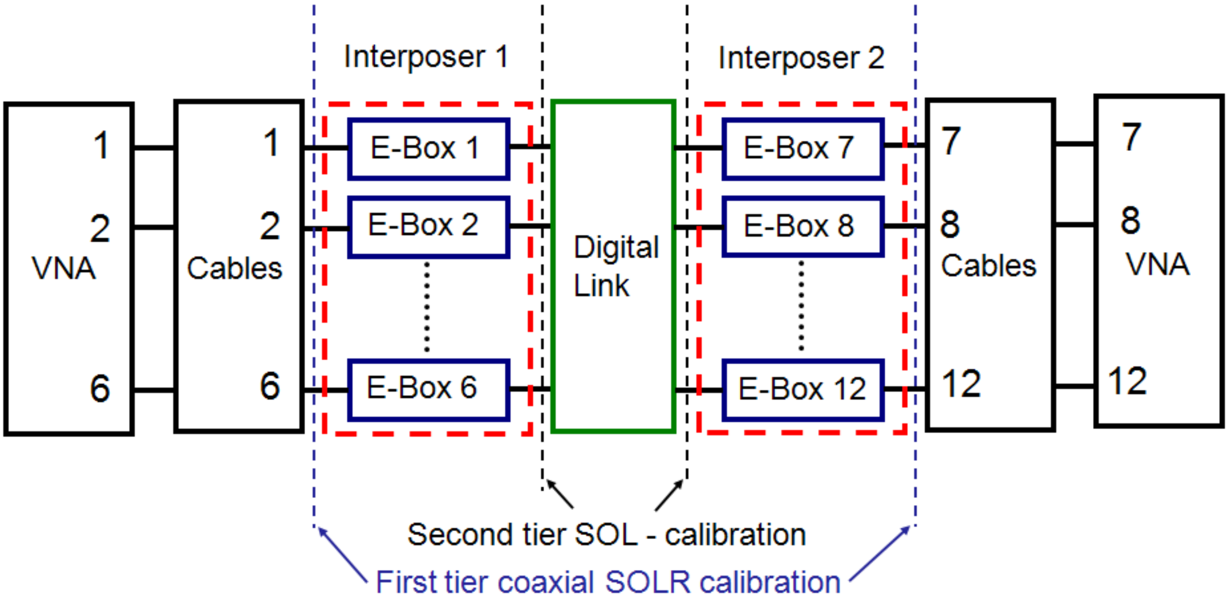


Figure 5.12 Two-tier calibration procedure for de-embedding the interposers from the measured data: For the 1st tier a coaxial SOLT with an electronic calibration module is performed. For the 2nd the custom-made substrates are measured and used for the SOL calibration algorithm [15].

5.4. Probing Fixture Calibration Procedure

For the de-embedding of the probing fixture it was assumed that the crosstalk between adjacent measurement ports is negligible. Investigations with respect to the crosstalk behavior and electrical performance of the designed probing fixtures were discussed in [13]. Results from time and frequency domain crosstalk analyses are summarized in the next Section. Under the assumption that the coupling between adjacent signal vias in the probing fixture contact array is lower than the coupling in the investigated structure every measurement port can be de-embedded individually from the measurements as depicted in Figure 5.12. For the extraction of the measurement ports the two-tier calibration method is applied and the obtained error boxes are subsequently de-embedded from the measurements performed with the cascaded probing fixtures. For the 1st tier, an ECAL module is used for the removal of the effects of cables and VNA hardware. For the 2nd calibration tier the custom-made termination substrates are measured with the interposers and used to perform an Short-Open-Load (SOL) calibration (Appendix A.2). For this purpose the calibration substrates have to be placed into one of the cells (a corner or a middle one, depending on the interposer access via array orientation) of the dedicated fixture for attaching them to the interposer access via array. As shown in Figure 5.13, the designed fixture board can utilize the same clamping hardware as presented in Section 5.2. Hence, the three

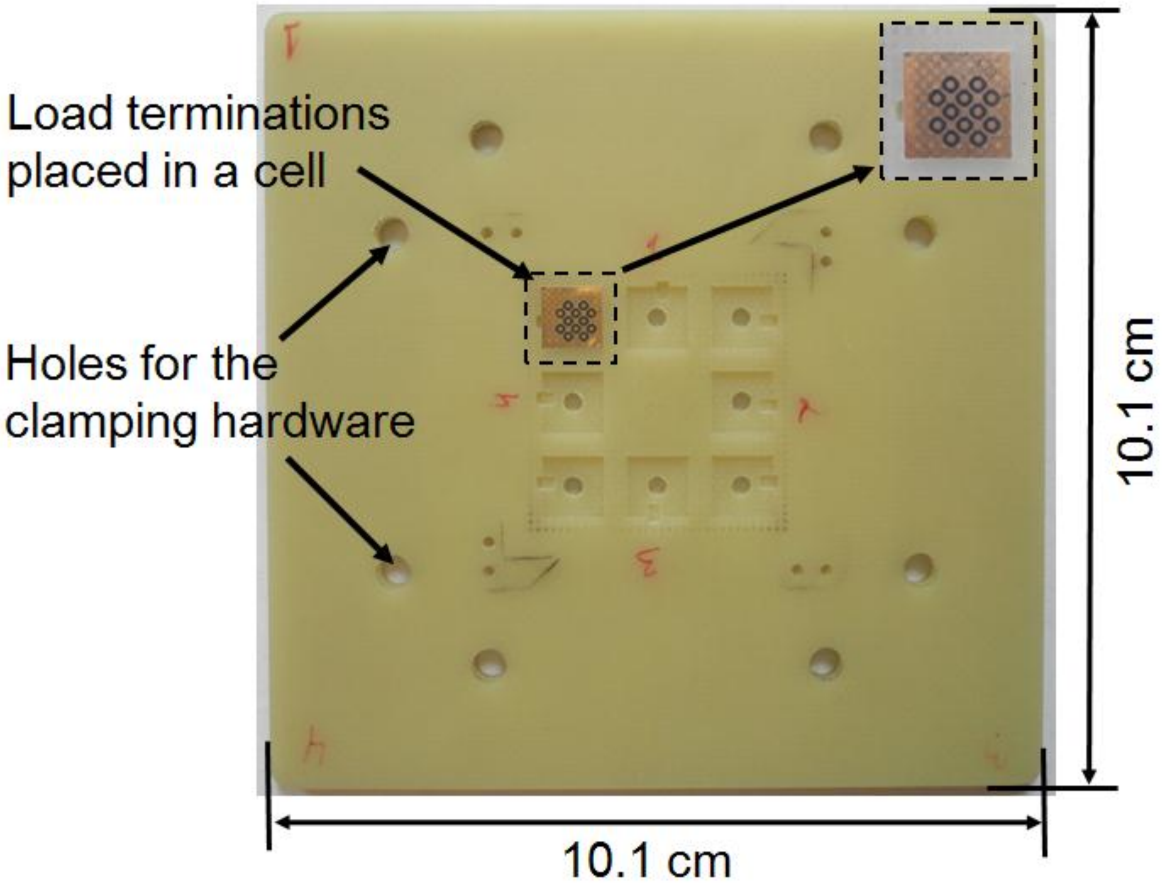


Figure 5.13 Test board for clamping the substrates to the access via array of the probe fixture. For the interposer calibration the fixture is mounted in the mechanical set-up instead of the test board. Depending on the via array orientation the termination substrate has to be placed in a corner or a middle cavity.

terminations have to be measured with the used interposer ports to extract error boxes for them.

The SOL algorithm computes the error parameters of the used measurement ports based on the independent microprobe measurements of the calibration standards. Alternatively, the computed S-parameters from the full-wave models can be used for this purpose. On the other hand, commercial vector network analyzers require for their calibration lumped models for the description of the correction parameters of commercial calibration substrates when applying them to calibration measurements. Thus, an attempt was made to derive lumped models for the custom-made load, short and open terminations measured with microprobes by fitting the corresponding S-parameters. The lumped elements which might be used instead of the measured short, open, and load terminations are shown in Figure 5.14 and Figure 5.15

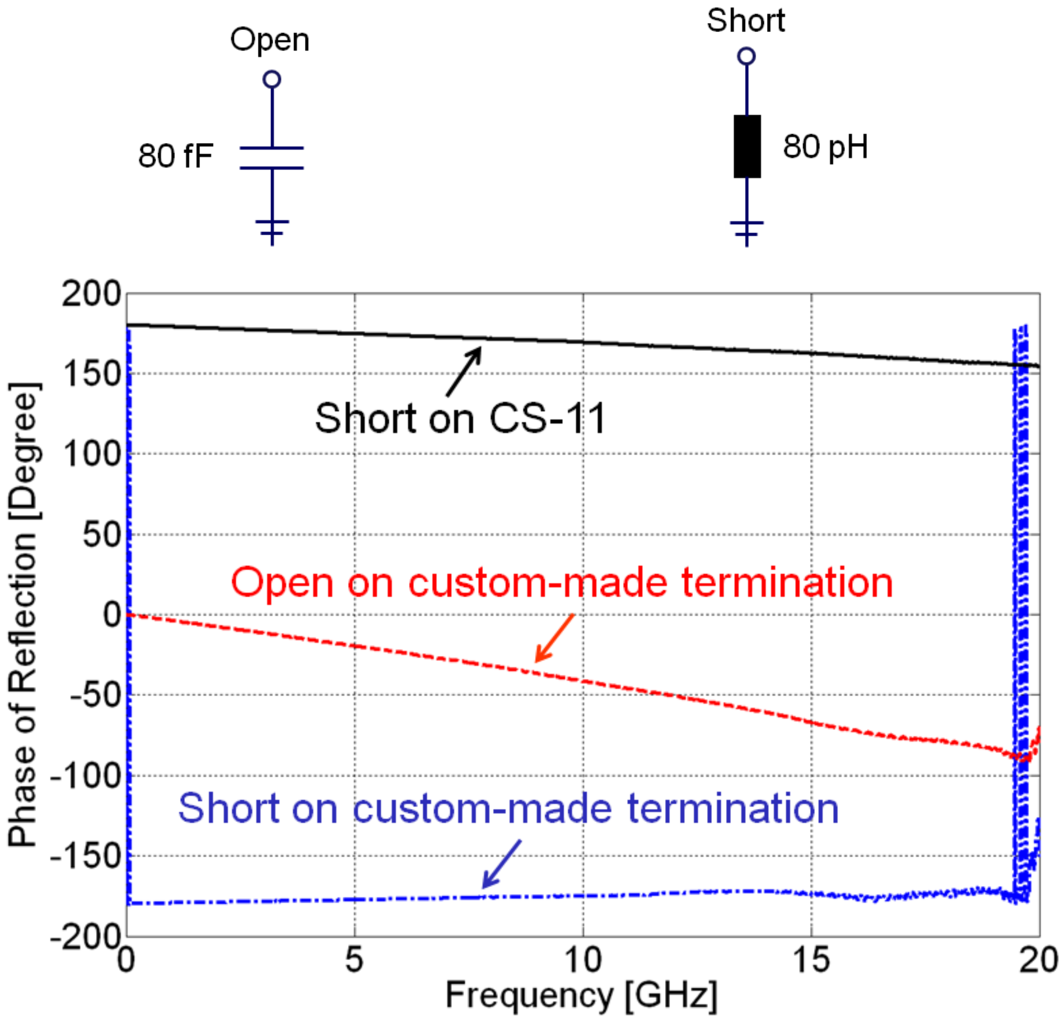


Figure 5.14 Lumped models used for characterization of the calibration substrates based on the microprobe measurements of the designed terminations. The phases of the short and open terminations designed on the custom-made substrates are obtained by microprobe measurements. The open termination behaves capacitively in the bandwidth between 30 MHz and 19.45 GHz. The short on the commercial calibration substrate CS-11 is inductive as expected.

The measurement of the “short” termination yielded a negative phase for the reflection (capacitive behavior) and not the expected positive phase (inductive behavior). As depicted in Figure 5.14 when measuring a short on a commercial calibration substrate (CS-11, $\varepsilon_r = 9.8$, [24]) with microprobes the termination behaves inductively as expected. For the modeling of the designed short termination an inductance of 80 pH was used. In order to obtain the “optimal” value for the parasitic inductance of the designed short termination and the fringing capacitance of the open termination the comparison to the “nominal” error boxes was made. For this purpose the correction parameters of the short and open terminations were computed using the lumped models shown in Figure 5.14.

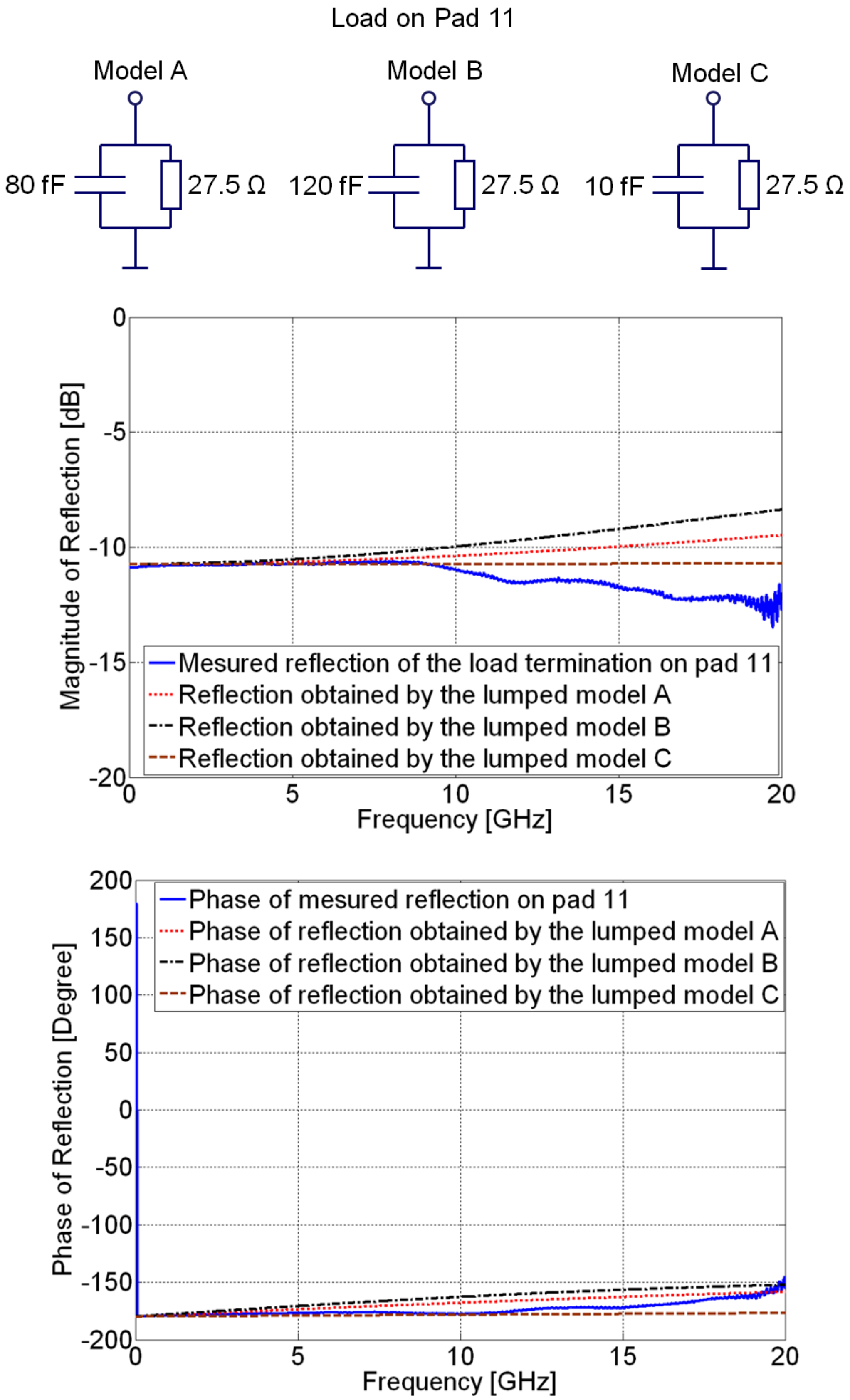


Figure 5.15 Correlation of the magnitude and phase of the measured load termination on pad 11 and variations of the lumped models for computation of the expected S-parameters of the termination.

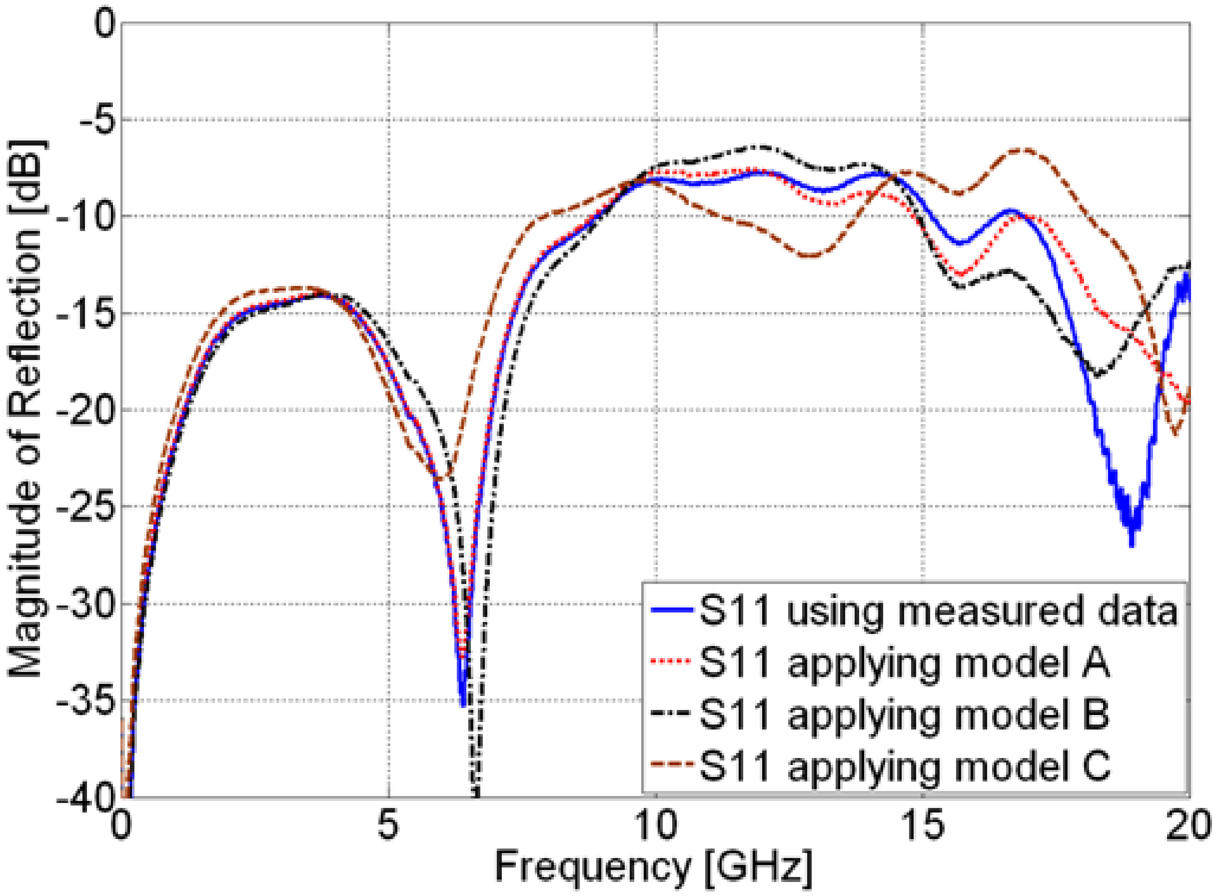


Figure 5.16 Comparison of reflections on the connector side in via 5 obtained after calibration with the measured "expected" S-parameters and the generated S-parameters from the lumped models A, B and C. The best correlation is obtained for model A.

In order to investigate the appropriate lumped model for the characterization of the load termination the three models from Figure 5.15 were applied in the calibration and thus three different error parameter sets were extracted. Error parameters in case of via 5 on the SMP interposer obtained with probe measured S-parameters are compared against those resulting from the use of lumped models (Figure 5.16) The correlation of the corresponding transmission parameters is shown in the Appendix A.8 (Figure A.8.25). As can be seen in both plots, the best correlation of the two methods was achieved in case of model A for the frequency bandwidth up to 10 - 15 GHz. Furthermore, in Figure 5.15 one can see that the parasitic capacitance of the load termination might vary between 10 fF and 120 fF. Even though the correlation to the microprobe measured S-parameters of pad 11 seems to be better in case of model C with fringing capacitance of 10 fF, considering the correlation of the error boxes from the three models to the nominal error box the fringing capacitance of 80 fF (model A) appears as an adequate value for the characterization of this parasitic behavior. Hence, the values illustrated in Figure 5.14 were chosen as the best for the de-embedding of the interposer measurement ports in case of via 5 on the SMP interposer. As explained in Section 5.3, due to the thin film resistor material manufacturing tolerances (200 Ω/sq ± 20 %), separate models for every load termination on the substrate might be needed and the DC resistance value can be in the range of 19 - 28.5 Ω. For the measured terminations on load #21 the parallel load is in the range of 26 - 29 Ω.

The results obtained from the correlation to the nominal error boxes let one conclude that the suggested models can be used as input for commercial calibration tools and that probe based measurements are only needed for the load terminations in order to determine their R_{dc}.

5.5. Electrical Performance Study

In this Section the measurement bandwidth limitations of the designed interposers which were particularly discussed in [13], [15] are presented in the time and frequency domain. A time domain reflectometer oscilloscope (Tektronix DSA 8200, voltage step = 250 mV, t_r ~ 12 ps) and a vector network analyzer (Agilent 8364C, 10 MHz - 20 GHz, Δf = 10 MHz) were used for the analysis of the electrical performance of the "load" terminated interposer measurement ports. As shown in [13] in case of via 6 the discontinuities in the signal transition path from the connector launch to the LGA contact pins are mostly capacitive. In Figure 5.17 the time domain responses of a voltage step in via 6 of the two types of interposer are presented. Similar to the results shown in [13] one can see that the largest discontinuity is represented by the transition from the LGA array to the "load" termination and thus it is expected to be the main limiting factor for the maximum achievable measurement bandwidth with these interposers.

The S-parameters of the "load" terminated interposers measured with the VNA have been obtained and transformed into time domain to correlate to the time domain measured responses. In Figure 5.18 one can observe similar behavior of the step response of via 6 e.g. the amplitude of the reflection in the LGA launch is approx. 19 % from the incident step voltage (1 V) where in the time domain measurement it is approx. 17 % (voltage step = 250 mV). Here, it is important to note that the cables used in the time domain measurements were not de-embedded and their attenuation has an additional effect on the results.

Considering the reflection on the connector side of the interposers, the SMP connector launch via induces larger reflection (13 % from the amplitude of the incident voltage step) than the one of the SMA connector (7 % from the amplitude of the incident voltage step). The reflections on the connector side obtained for via 6 of both

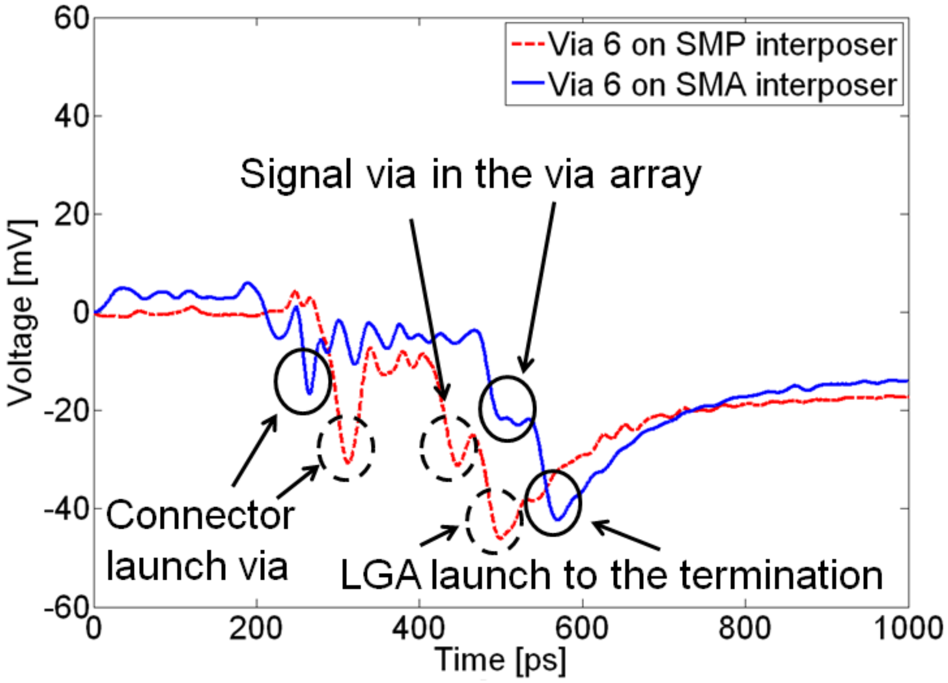


Figure 5.17 Time domain reflection measured on via 6 of the middle via array interposers with a digital sampling oscilloscope (t_r = 12 ps, voltage step = 250 mV) when the interposer is terminated with a "load" termination. The LGA contact pins represent the largest discontinuity [13].

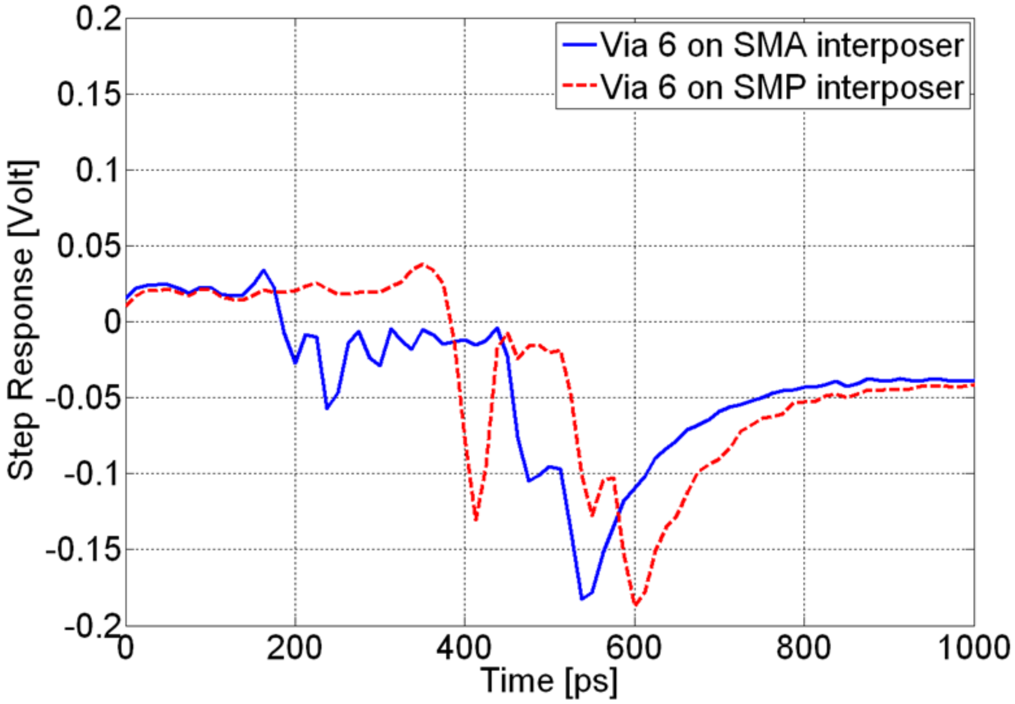


Figure 5.18 Time domain reflection of via 6 obtained by Inverse Fast Fourier Transformation (IFFT) of S-parameters of "load" terminated middle via array interposers (t_r = 12 ps, voltage step = 1 V) [13].

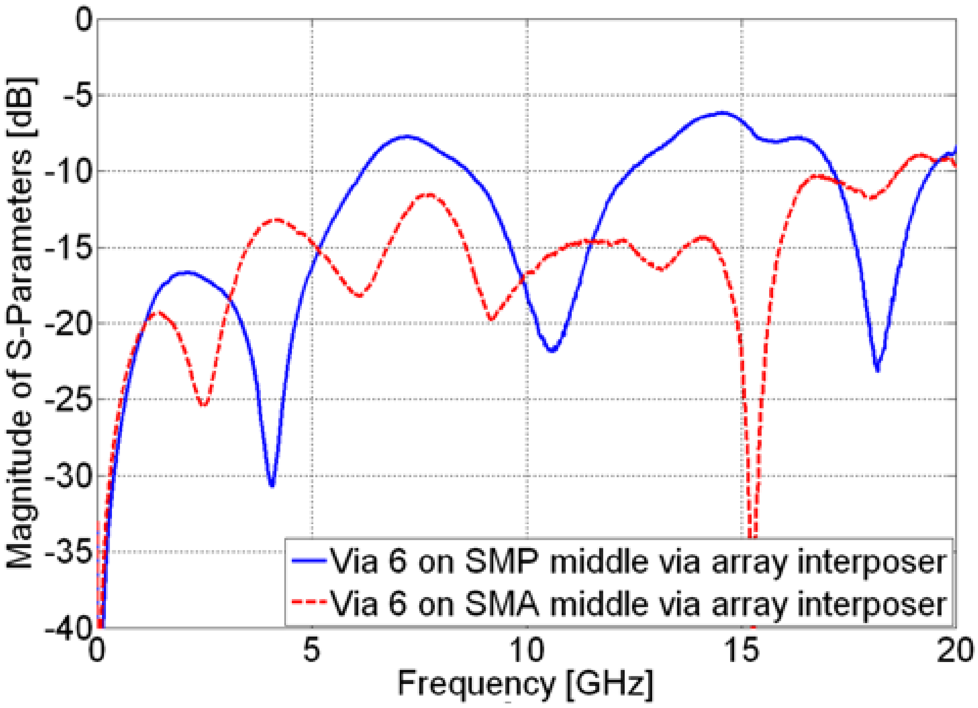


Figure 5.19 Comparison of reflections on via 6 extracted by the two-tier calibration procedure. The SMA middle via interposer shows better electrical performance.

interposers extracted from the calibration procedure in frequency domain are depicted in Figure 5.19. It is obvious that the SMA launch via has better electrical performance (~4 dB lower reflection at the quarter wave length resonance frequency) than the one of the SMP interposer. Considering the transmission parameters of both interposers the differences between the SMP and SMA type are less pronounced (Figure A.8.26 in the Appendix A.8).

Furthermore, a near-end crosstalk (NEXT) analysis has been carried out for the port pairs used later on in the link measurements using the measurement set up from the TDR measurements where the interposers were terminated with the "load" terminations. These time domain measurements have shown that the crosstalk is mainly induced in the access via array of the interposers. As depicted in Figure 5.20 and Figure A.8.27 (in the Appendix A.8) the NEXT is larger for adjacent vias in a diagonal and is reduced by a factor of six when a ground via is placed between two adjacent ports. In general considering port pairs in the access via arrays, a distance dependency was observed. NEXT is attenuated by a factor of 5 when at least one intervening ground via is present [13].

In Figure 5.21 frequency domain measurement of the near-end crosstalk (NEXT) of a via pair without an interleaving ground via (corner via array interposer footprint) is shown. Considering via pairs with one interleaving ground via (middle via array interposer, Figure A.8.28 in the Appendix A.8) NEXT is reduced by 15 – 20 dB. In

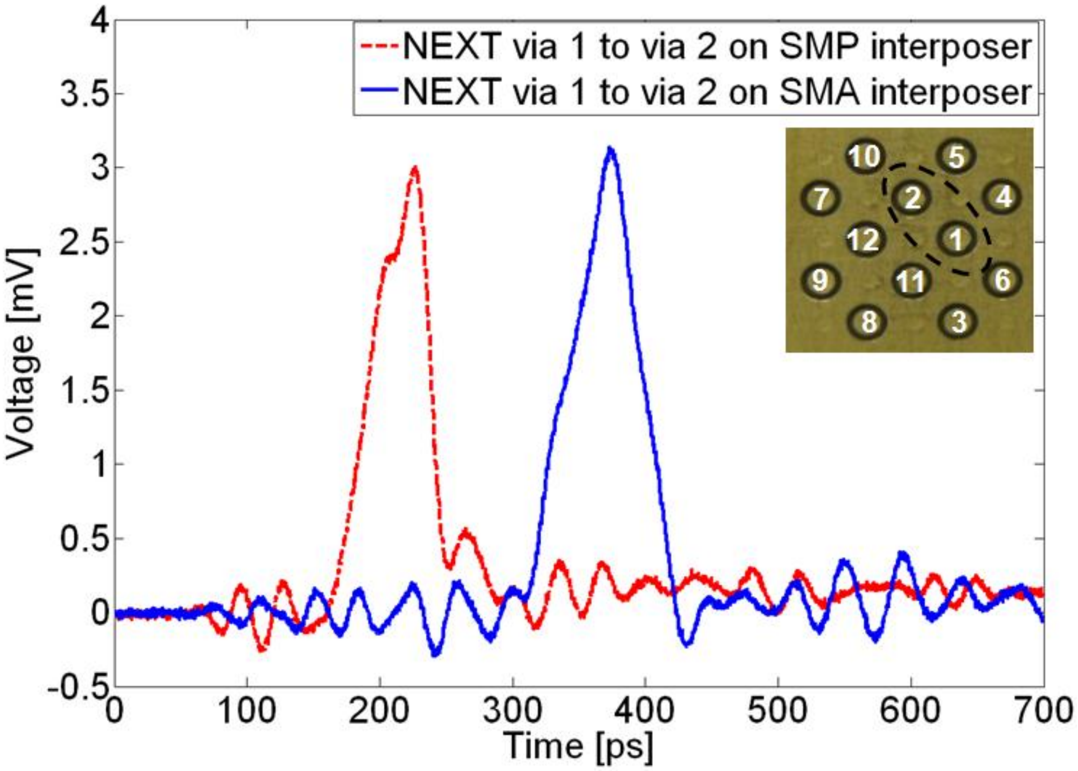


Figure 5.20 Time domain near-end crosstalk (NEXT) due to rising edge between via 1 and via 2 obtained by digital sampling oscilloscope with “load” terminated interposers [13].

Figure A.8.29 (in the Appendix A.8) the NEXT between vias 5 and 6 when two ground vias are placed in-between (middle via array interposer) falls to -65 dB where the crosstalk in the SMP interposer increases to -40 dB in the range of 15 GHz. A clear explanation for the crosstalk behavior of the SMP interposer was not found but due to the fact that the NEXT magnitude is below -40 dB (corresponds to 1 % via coupling) this effect can be neglected.

5.6. Analysis of Contact Reproducibility

In order to detect if the applied pressure present on the LGA array is sufficient to ensure reproducible interposer measurements, some mechanical and electrical tests were performed. For the mechanical tests pressure sensitive foil fixed in the area between the interposer bottom side and the LGA top side was used to obtain the force distribution when the clamping hardware is loaded with 50 kg (43 grams/contact). In Figure 5.22 the footprints of the tests with two types of SMA interposer are shown. Considering the area where the launch access via array touches the LGA pins one can see that the pressure distribution is not constant in case of the interposer with access via array in the corner of the board (corner via array interposer) whereas in case of the interposer with the access via array in the middle of the board edge (middle via array interposer) the pressure is more uniform.

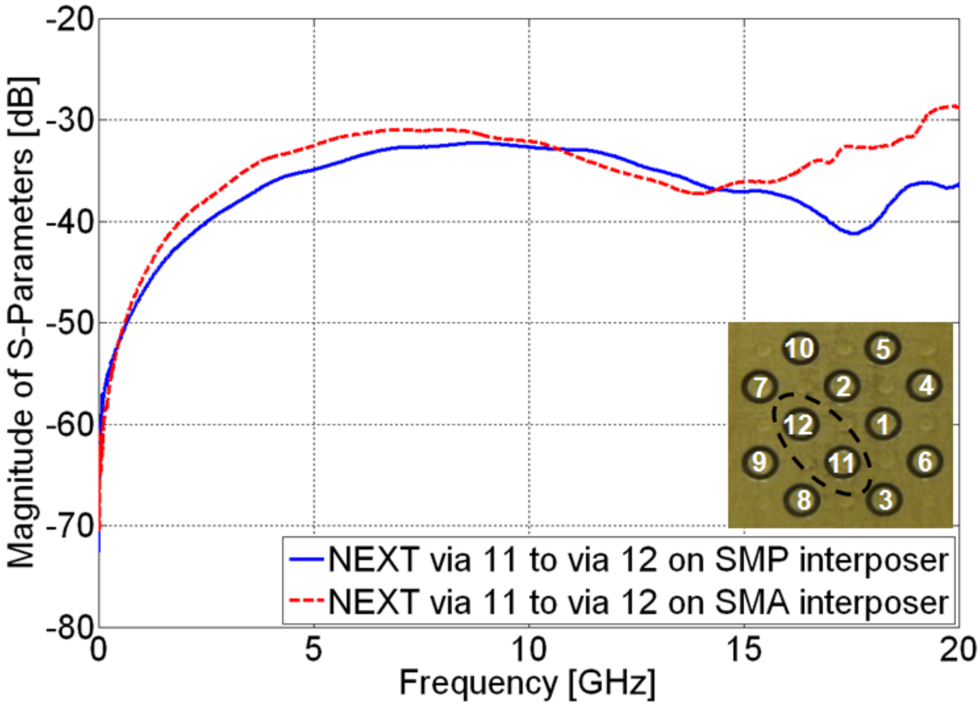
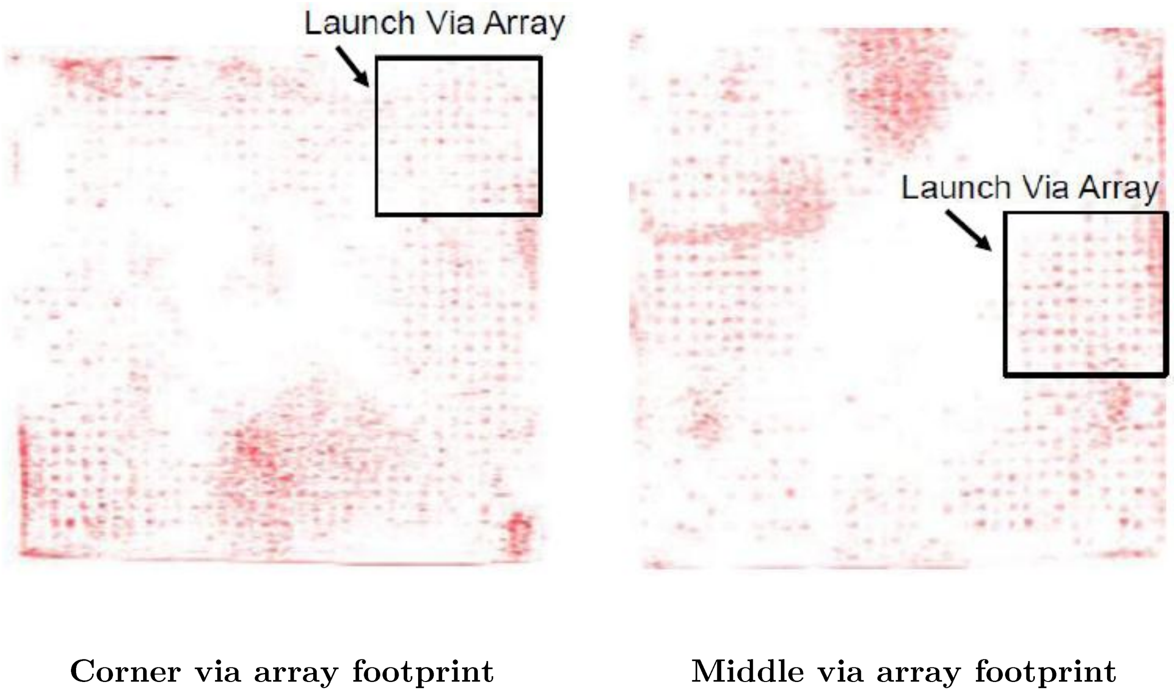


Figure 5.21 NEXT of via 11 to via 12 in the via arrays placed in the corner of the SMP and SMA interposer boards. In both cases the crosstalk is in the range of -30 dB [13].



Corner via array footprint **Middle via array footprint**

Figure 5.22 Pressure displacement of pressure sensitive foil. The footprints of the corner via array and middle via array SMA interposers illustrate that the pressure in case of the middle via array interposer is more uniform [133].

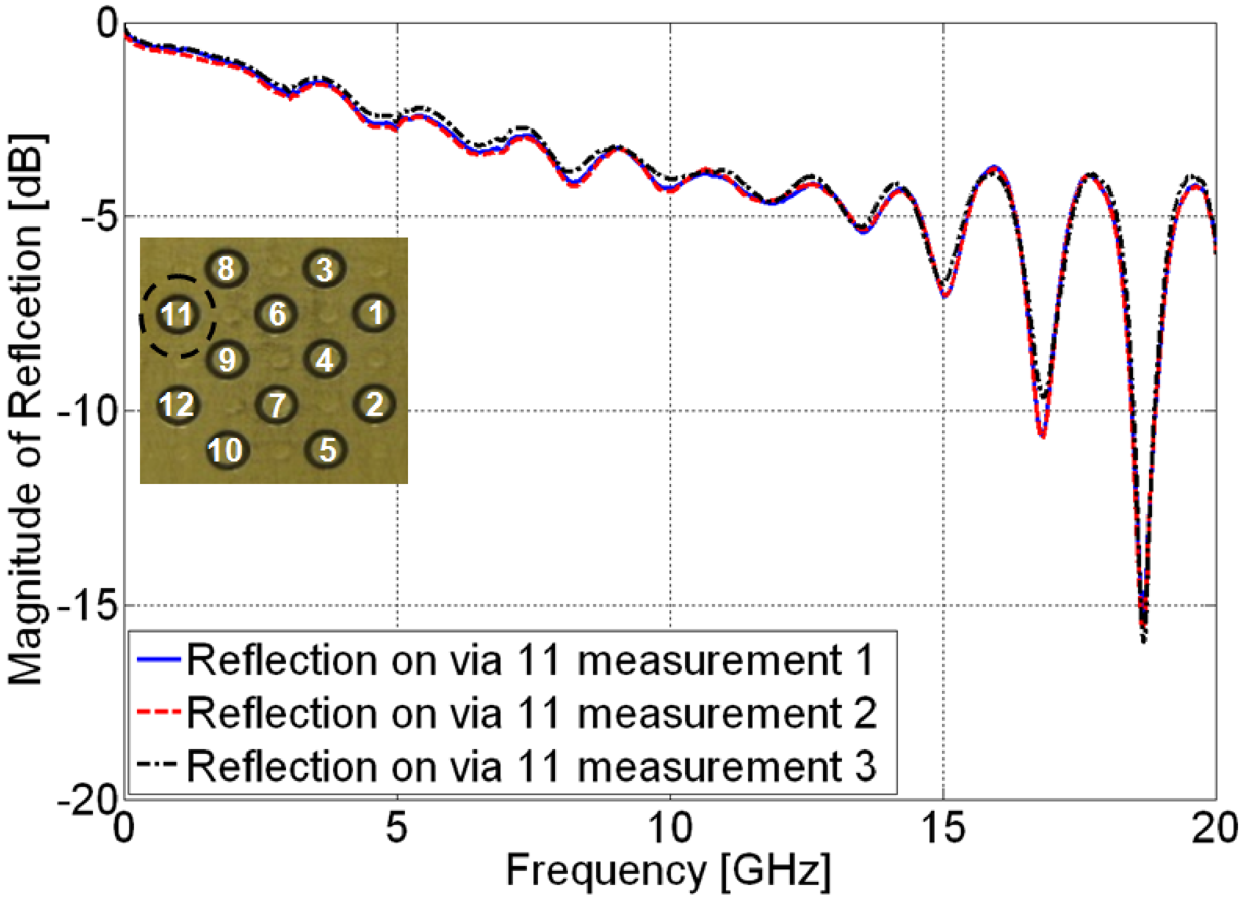


Figure 5.23 Reflection parameters obtained by three times repeated measurements on “short” terminated via 11 in the corner via array SMP interposer. Adequate repeatability is obtained for the three measurements [13], [133].

In that regard measurements with the SMP interposers connected to the short termination were performed with the aim to investigate the connection repeatability in case of the 50 kg loading. The measurements were repeated three times in the frequency bandwidth up to 20 GHz. In Figure 5.23 adequate repeatability can be detected mostly in case of the middle via array interposer. These results reinforced the conclusions taken from the test with the pressure sensitive foil that the force distribution in case of the interposers with the access via array placed in the corner of the PCB is not equally distributed [133].

The termination with the short was chosen due to the fact that a small shift of the contact pins will not affect the measurement repeatability noticeably. On the other

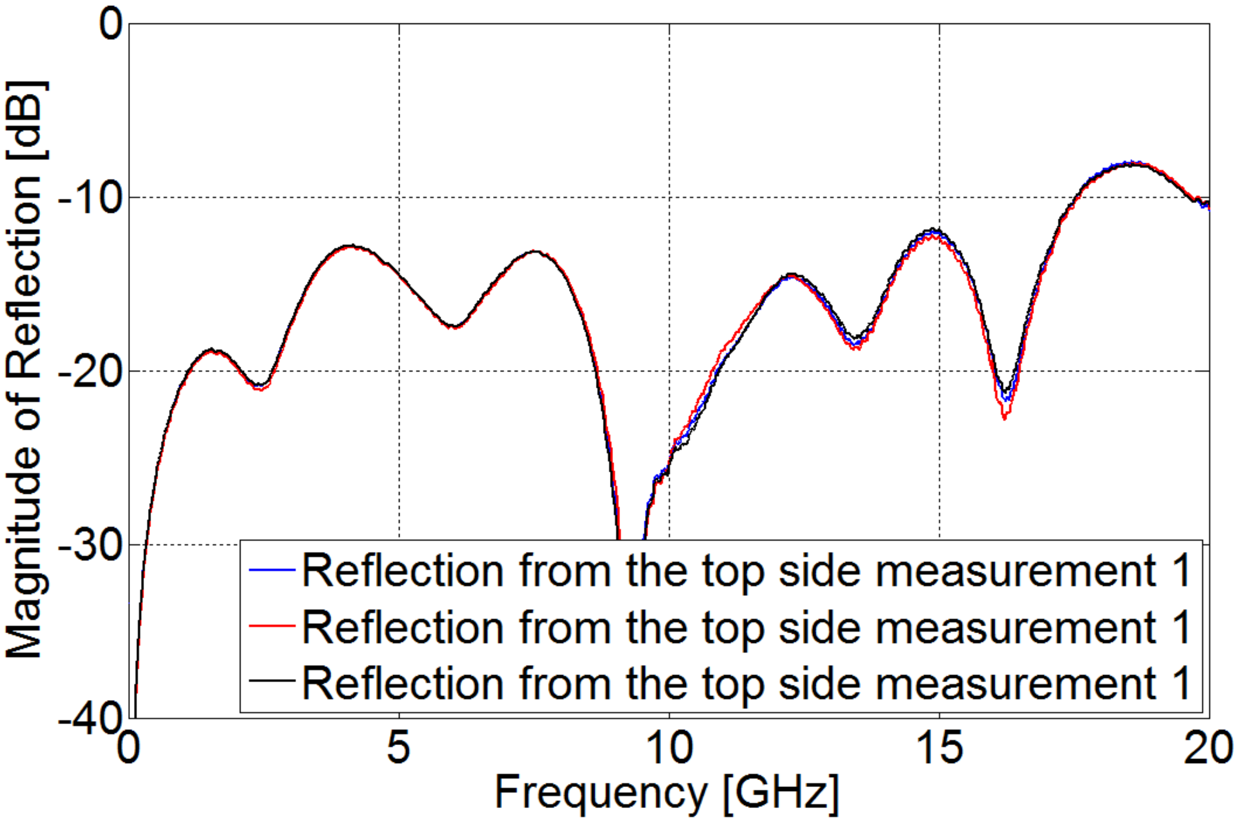


Figure 5.24 Reflection parameter of the connector side (via 7) on the middle via array SMA interposer extracted from three times repeated calibration measurements. Adequate repeatability is obtained for the three measurements [13], [133].

hand the load and open terminations were not used for this study because shifting of the signal contact pins caused by the clamping of the interposers will have an influence on the value of the parasitic capacitances in the ring shaped region of the both terminations. Hence, the electromagnetic field in that region will be affected by the change of the parasitics and the measured response will contain effects not only from the amount of the loading pressure but also from the tolerances of the positioning of the contact pins in the LGA array induced by the clamping hardware.

In general the mechanical and electrical tests illustrated the difficulty in ensuring uniform pressure in an LGA which requires an optimization of the mechanical clamping. The results from the investigations using the present clamping hardware with respect to the repeatability have shown that the applied pressure has to be not less than 40 grams/contact. As depicted in Figure 5.24 this loading pressure is a good compromise e.g. when extracting the error parameter (reflection from the connector side) of via 7 in the middle via array SMA interposer. Good correlation can be seen in case of the reflection from the SMA connector side in the entire bandwidth up to 20 GHz. In order to prove the validity of these investigations, measurements of digital links performed with the interposers were compared to microprobe based measurements of the same links as shown in Section 5.7.

5.7. Correlation to Microprobe Measurements

In the following results from the application of the interposers to link measurements in the bandwidth from 10 MHz to 20 GHz are presented. Several test digital link structures were designed on a multilayer PCB with the aim to evaluate both types of interposers to obtain their maximum applicable measurement bandwidth. The structures represent long striplines (~ 5120 mil long) connecting the signal vias of two access via arrays which route the signals either on signal layers S1 or on signal layer S6 (Figure 5.25). Multiport measurements in the link structures with the interposers were performed and results compared to microprobe based measurements (Figure 5.26). For this purpose the links were measured in the bandwidth between 10 MHz and 20 GHz using commercial microprobes (Picoprobe Model 40A DS-style GS- and SG-225 µm pitch) connected to a multiport VNA (Agilent 8364C).

Initial results from the comparison of 4-port SMP and SMA interposer measurements to microprobe based measurements of the same links were shown in [13]. Here, further four port digital link measurements were performed using both types of interposer. Similar to the results presented in [13] no distinguishable differences between the measurements performed with both types of interposers were detected in the bandwidth up to 15 GHz. In case of links with vias routing signals on signal layer 1 (via 6) good correlation to probe measurements was obtained in the bandwidth up to 10 - 15 GHz (Figure 5.27 and Figure 5.28). The adequate correlation bandwidth reduces to 8 - 12 GHz in case of links with vias routing signals on signal layer 6 (via 12, Figure 5.29 and Figure 5.30). A NEXT comparison to probe measurements is shown in Figure 5.31. As expected the correlation is not as good as with regard to the probe based measurements. Considering the fact that the main crosstalk is induced due to the common coupled via lengths of the adjacent vias in the array it is expected that the crosstalk in the interposer access via array is larger (86 mil common coupled length of the vias on the SMP interposer or ~ 111 mil common coupled via length of the vias on the SMA interposer + 67 mil length of one LGA contact pin) than the one in the vias in the test structure (common coupled via length in the test board ~ 100 mil). To be able to measure crosstalk with the present interposer hardware, the common coupled length of the investigated via array structure should be larger than ~ 180 mil. In other words the thickness of the interposer board has to be smaller in order to reduce the common coupled length of the adjacent vias in the interposer access via array when shorter coupled vias have to be measured.

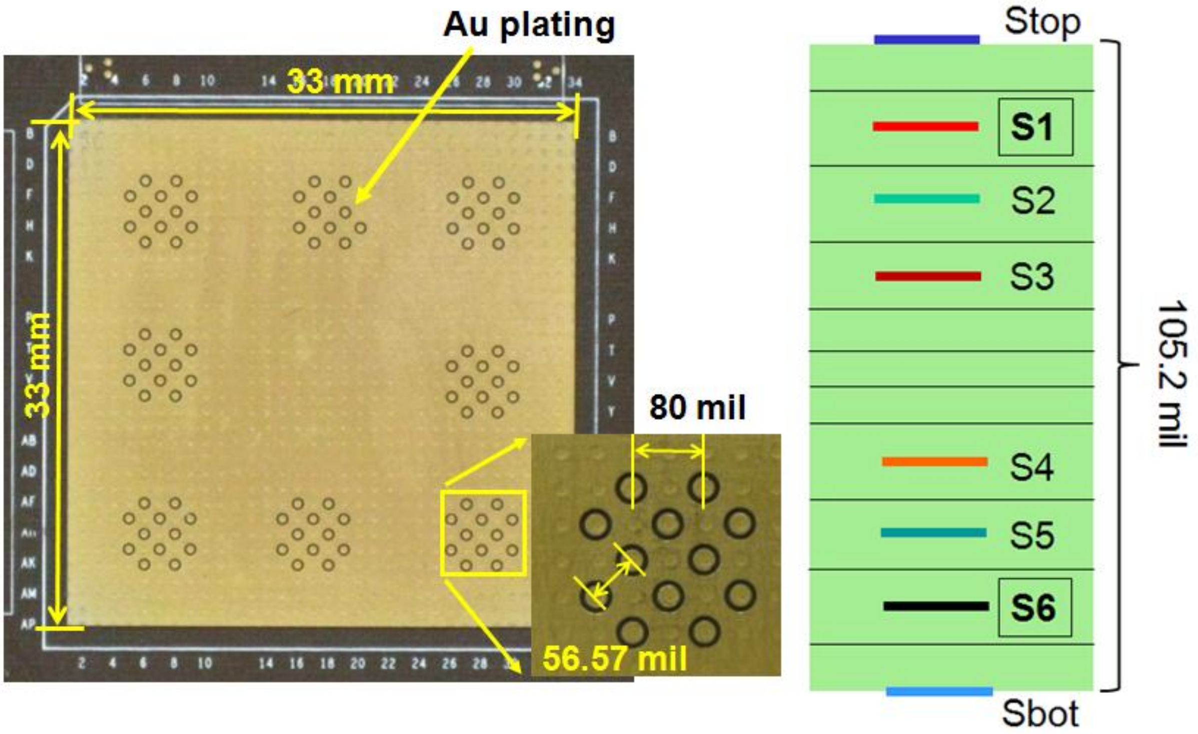


Figure 5.25 Via array test structure on a multilayer PCB with 8 test arrays for the probing fixtures. Signals are routed on layer 1 and layer 6 [13].

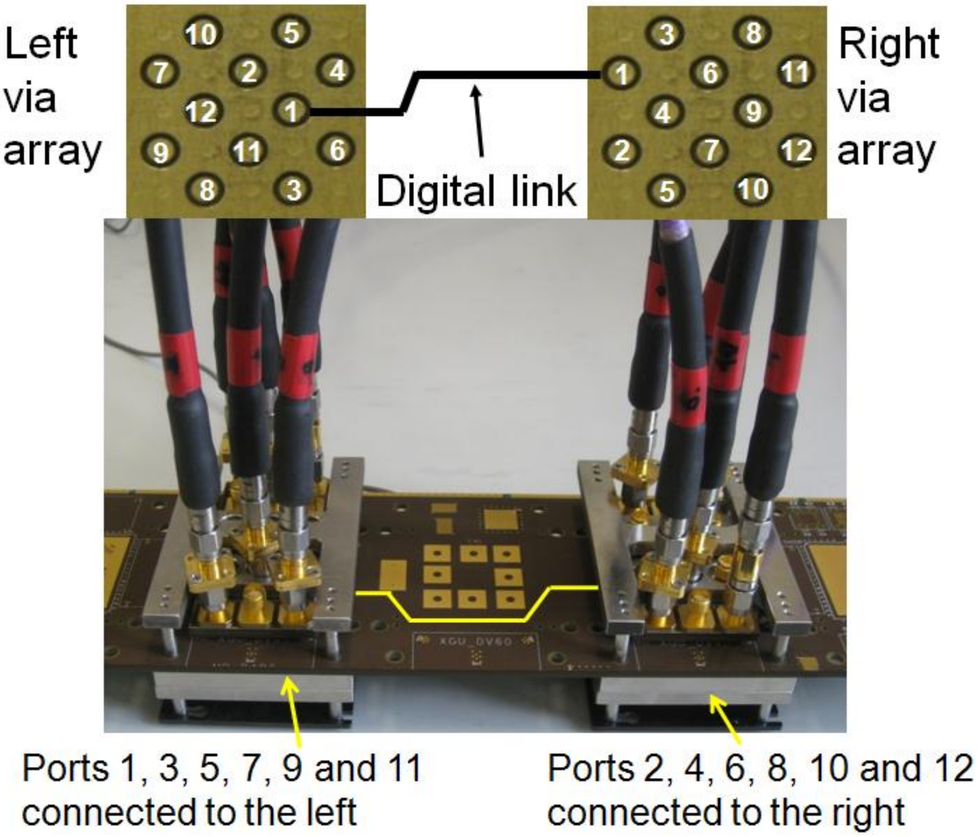


Figure 5.26 12-port measurement setup: Two interposers connected to dense via arrays routing long links in-between. Vias connected with the same link are labeled with identical numbers [13].

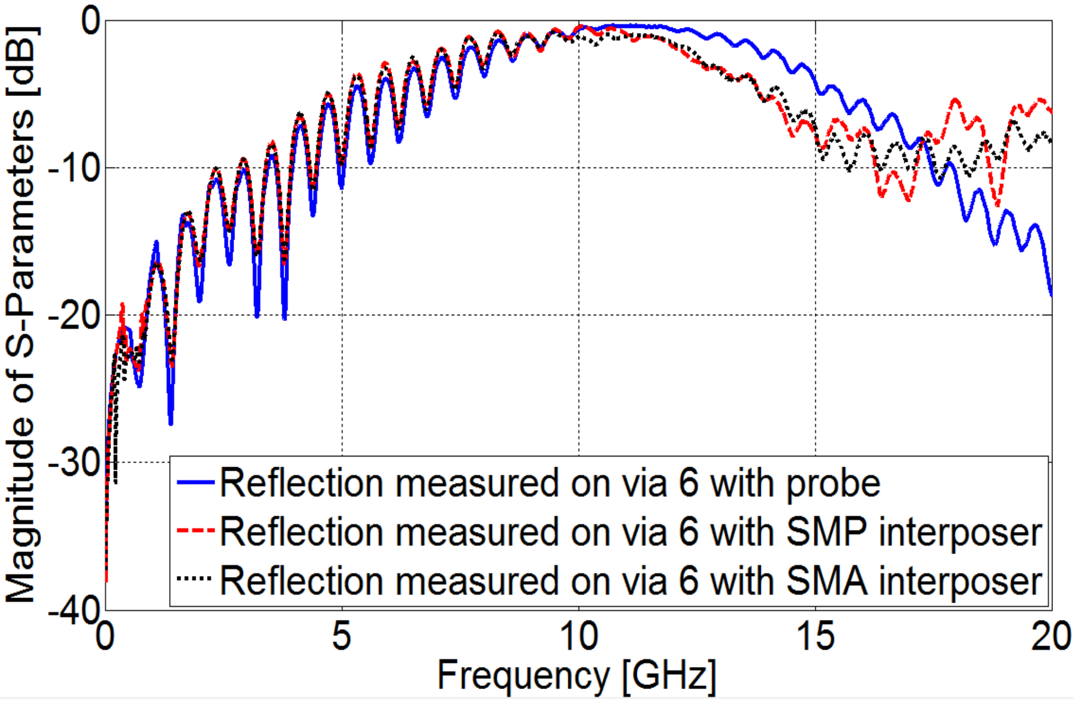


Figure 5.27 Reflections on via 6 in the left via array obtained by measurements with probe, SMP and SMA interposers. Good correlation is achieved up to 10 -15 GHz [13].

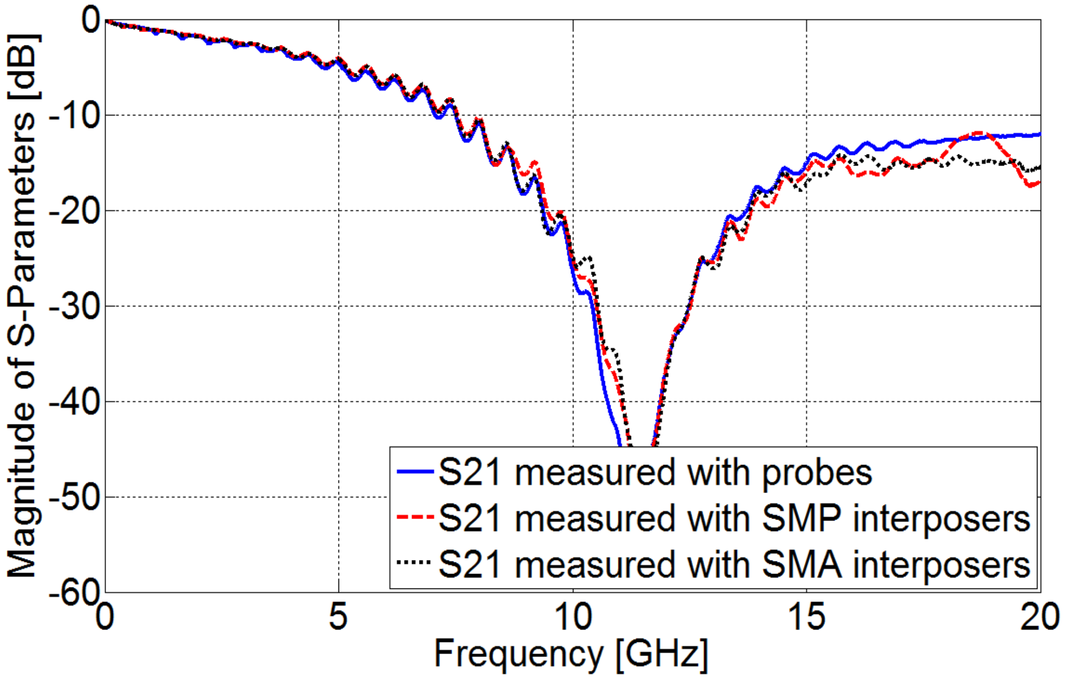


Figure 5.28 Transmission parameter of the link connecting via 6 in the left and right via arrays accordingly obtained by measurements with probes, SMP and SMA interposers. Good correlation is achieved up to 10 - 15 GHz [13].

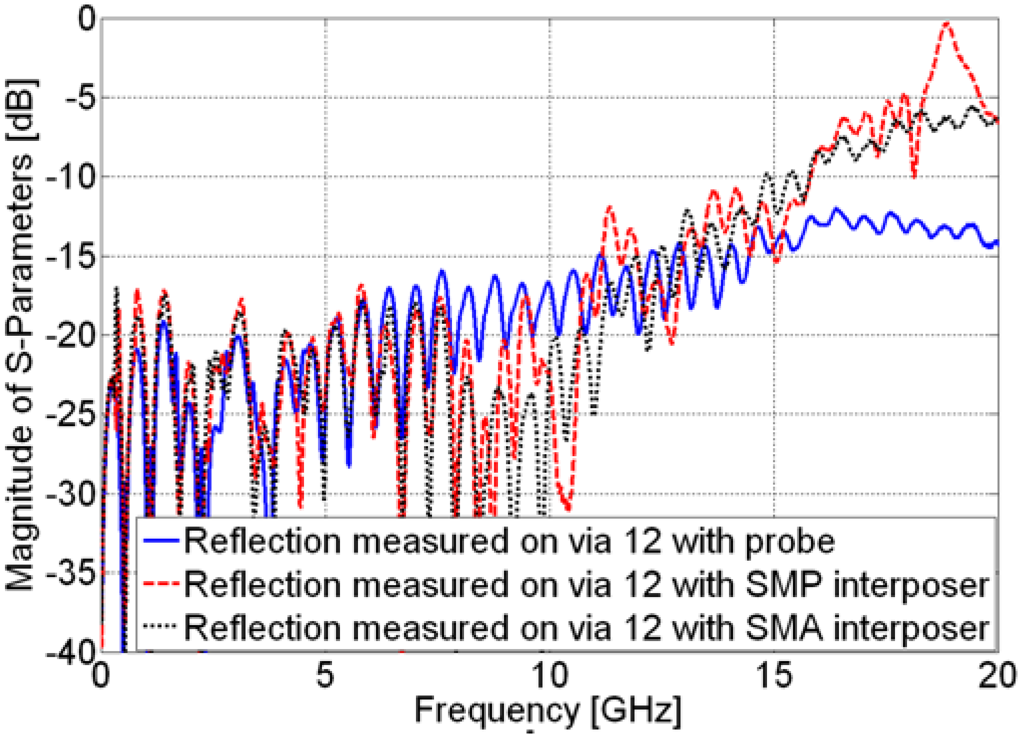


Figure 5.29 Reflections on via 12 in the left via array obtained by measurements with probes, SMP and SMA interposers. Good correlation is achieved up to 8 - 12 GHz [13], [133].

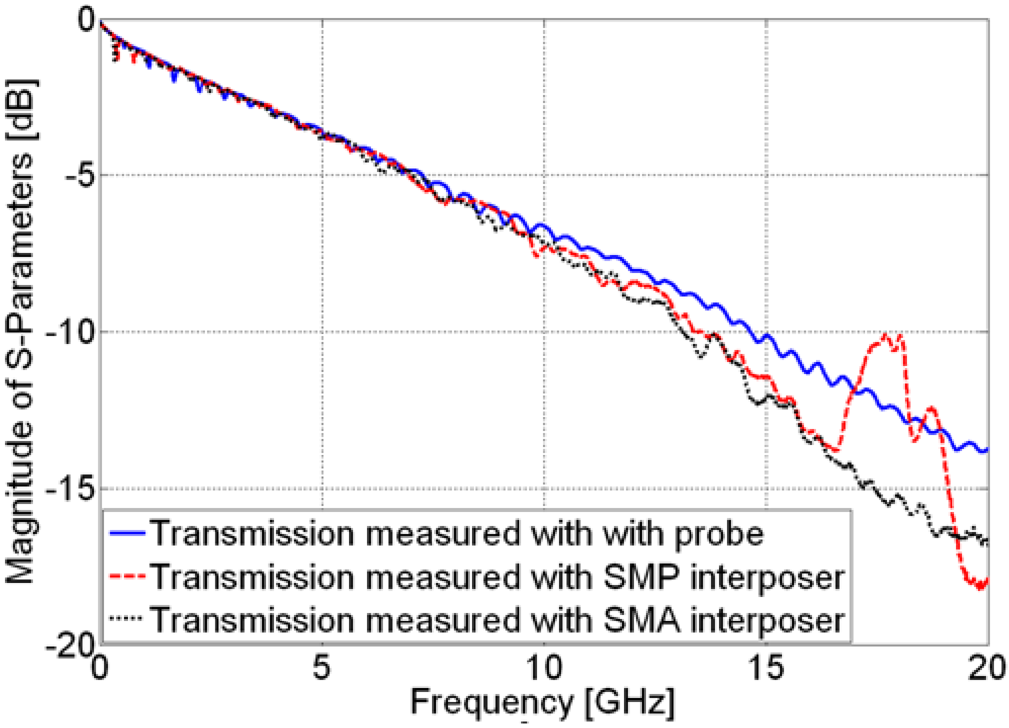


Figure 5.30 Transmission parameter of the link connecting via 12 in the left and right via arrays accordingly obtained by measurements with probes, SMP and SMA interposers. Good correlation is achieved up to 8 - 12 GHz [13], [133].

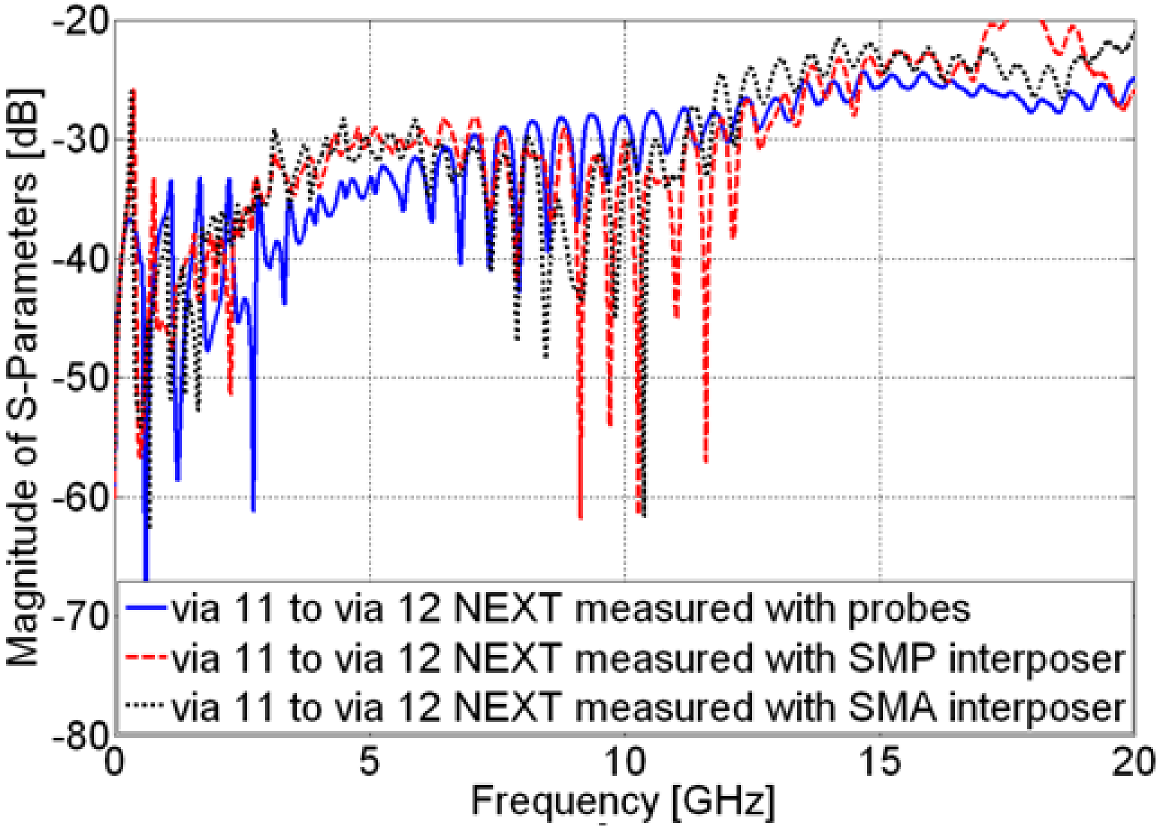


Figure 5.31 Comparison of near-end crosstalk (NEXT) of via 11 to via 12 in the via array at the beginning of the link obtained by probes, SMP and SMA interposers [13], [133].

Based on the shown results and taking into account the results from the crosstalk analyses in the previous Section the conclusion is that the interposers can be applied to measurement of coupled link structures with return loss larger than -16 dB (reflection at the quarter wave length resonance frequency), insertion loss less than -1 dB (at the quarter wave length resonance frequency), crosstalk of adjacent vias not less than -30 dB for the case of no interleaving ground via. The minimum measurable crosstalk can be even in the range of -40 dB if isolation ground vias are present between the adjacent signal vias.

Another test was performed where eye diagrams have been calculated from S-parameters measured with the probes and with two SMP interposers for the transmission in the link connecting the vias 5 in the access via arrays on the test board. A comparison of the results is shown in Figure 5.32. For the calculation a 256 bit pseudo random binary signal with a data rate of 10 Gbit/s and 20 ps rise time has been taken into account. The obtained results indicate that the designed interposers can be used for measurement of links with data rates of 10 Gbit/s which is applicable for measurements of the most common digital systems.

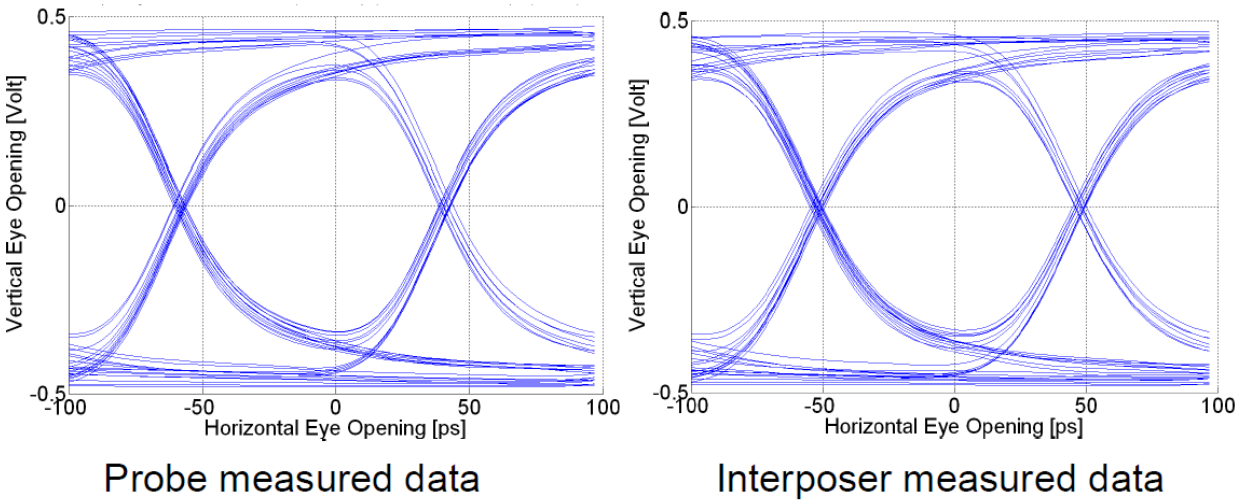


Figure 5.32 Eye diagrams calculated from S-parameters measured with probes and two SMP interposer for the transmission in the link connecting the vias 5 in the access via arrays on the test board. A 256 bit pseudo random binary signal with a data rate of 10 Gbit/s and 20 ps rise time has been taken as a basis for the calculation [13].

5.8. Modeling and Optimization

In this Section the extracted error parameters derived from the two-tier calibration are correlated to simulation data obtained by full-wave 3D models and refinements for optimization of the electrical performance are suggested (Figure 5.33) [113]. The 3D models used for the investigations were created from the PCB layout data using computer-aided design software (CAD, [129]). In order to reduce the computation time and memory requirements, the complexity of the initial interposer structure was reduced.

As illustrated in Figure 5.33 the interposer vias 5 and 6 were investigated using a reduced model which contained only the SMP launches of via 5 and via 6, the signal traces connecting the launches with the signal access vias in the launch via array, and the access via array by itself where most of the ground vias were removed. The LGA socket is included in the interposer model where the signal contact pins are connected to coaxial extensions (50 Ω) excited with waveguide ports on the bottom side (20 mil long, Figure 5.34).

In Figure 5.35 the model-to-hardware correlation of the extracted reflection from the connector side in via 5 is shown where adequate correlation in the frequency bandwidth up to 16 GHz can be seen. Considering the correlation of the transmission parameters depicted in Figure 5.36 one can see that the extracted transmission loss is larger than that obtained from the full-wave model.

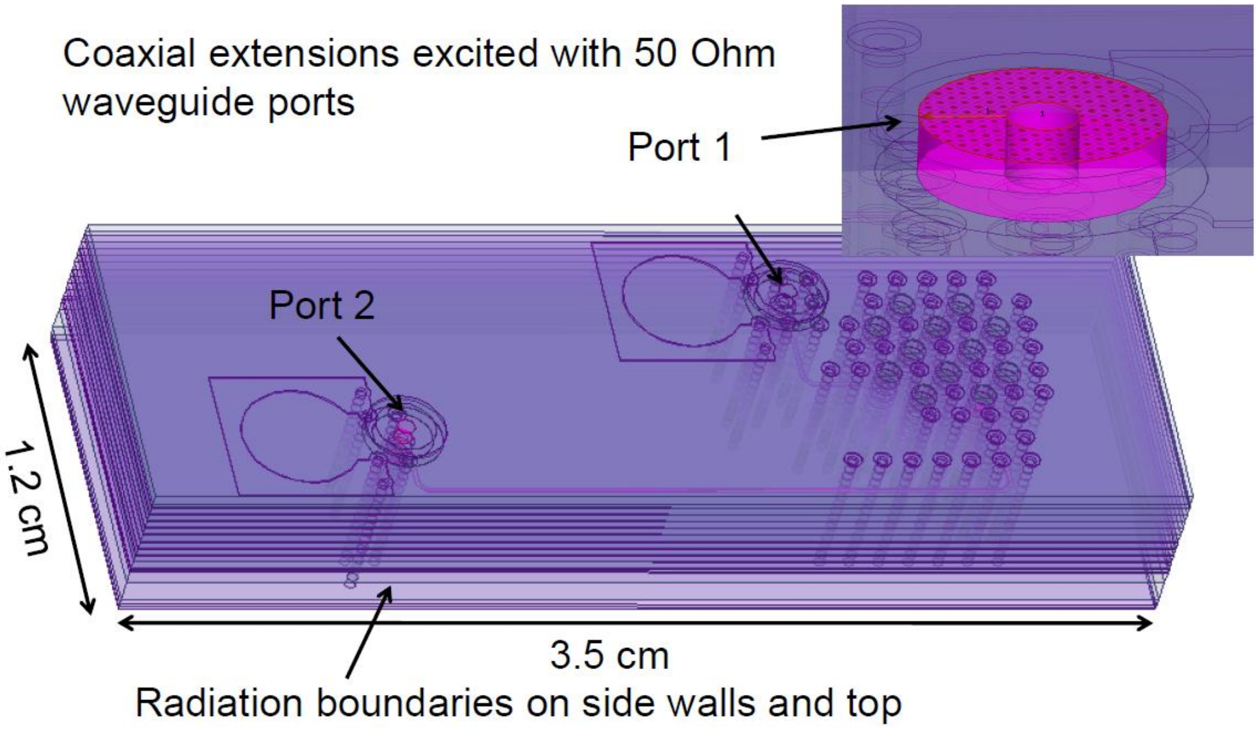


Figure 5.33 Reduced full-wave 3D model of via 5 and via 6 on the corner via array interposer placed on the LGA socket. (memory requirement approx. 7.20 GB, computational time approx. 2 days) [113].

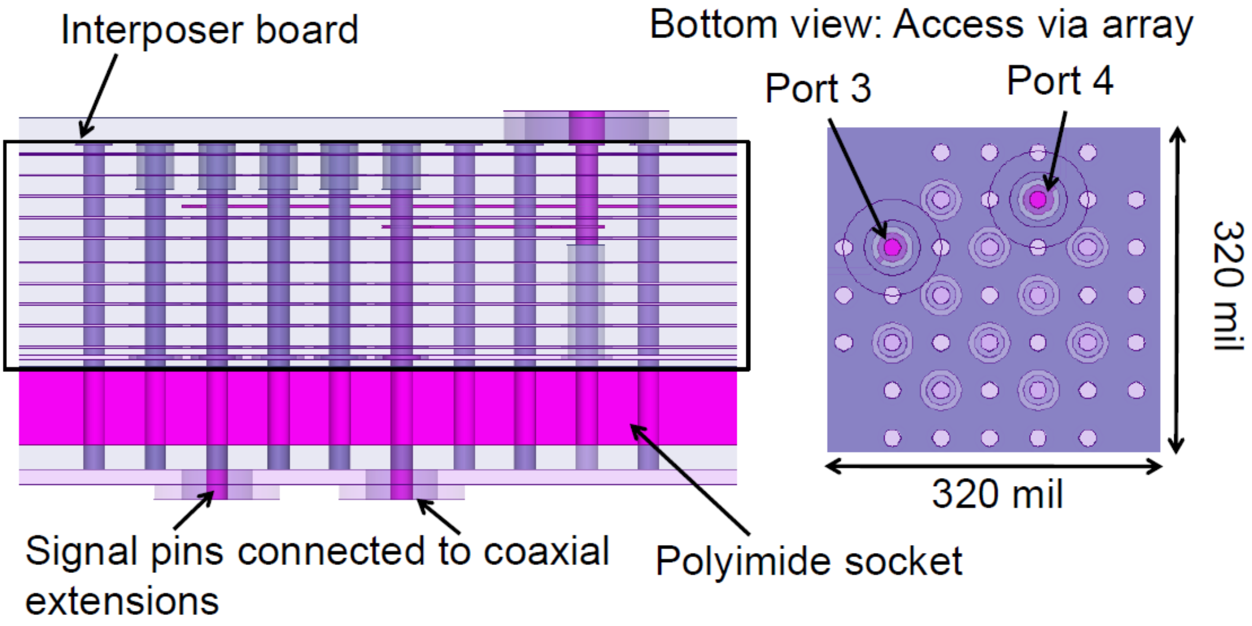


Figure 5.34 Side view and bottom view of the full-wave model placed on the LGA socket. The signal pins on the bottom are connected to coaxial extensions excited with 50 Ohm waveguide ports [113].

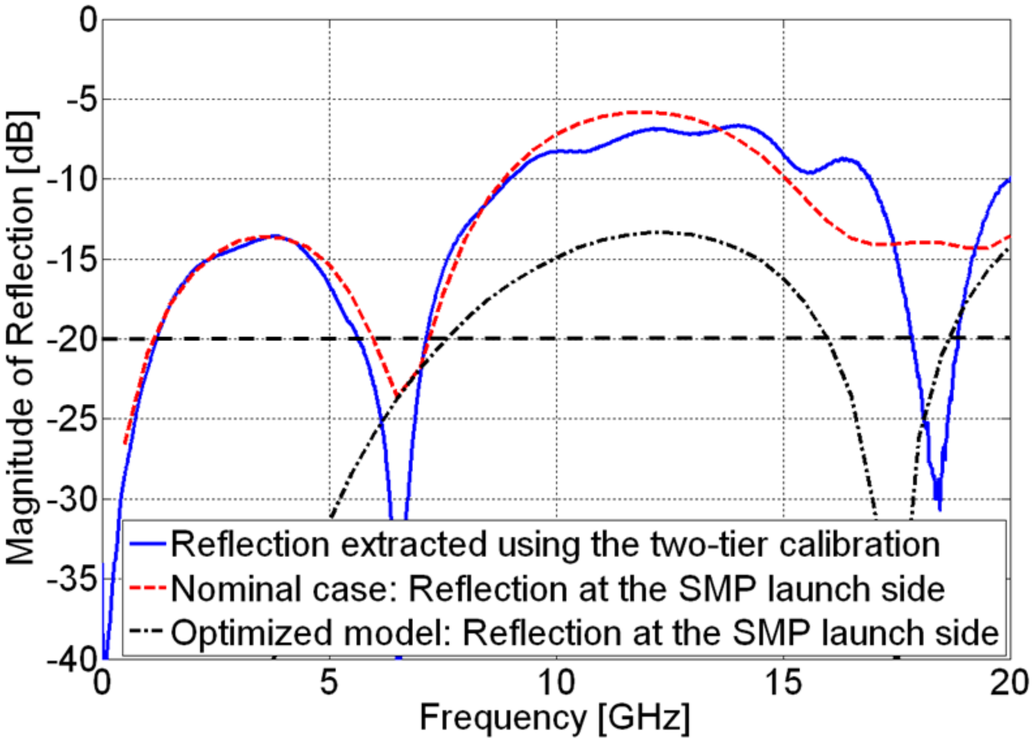


Figure 5.35 Comparison of the reflection at the SMP access via 5 on the implemented SMP interposer design and on the modified model. Increasing the antipad diameters improves the -20 dB limit by appr. 7 GHz.

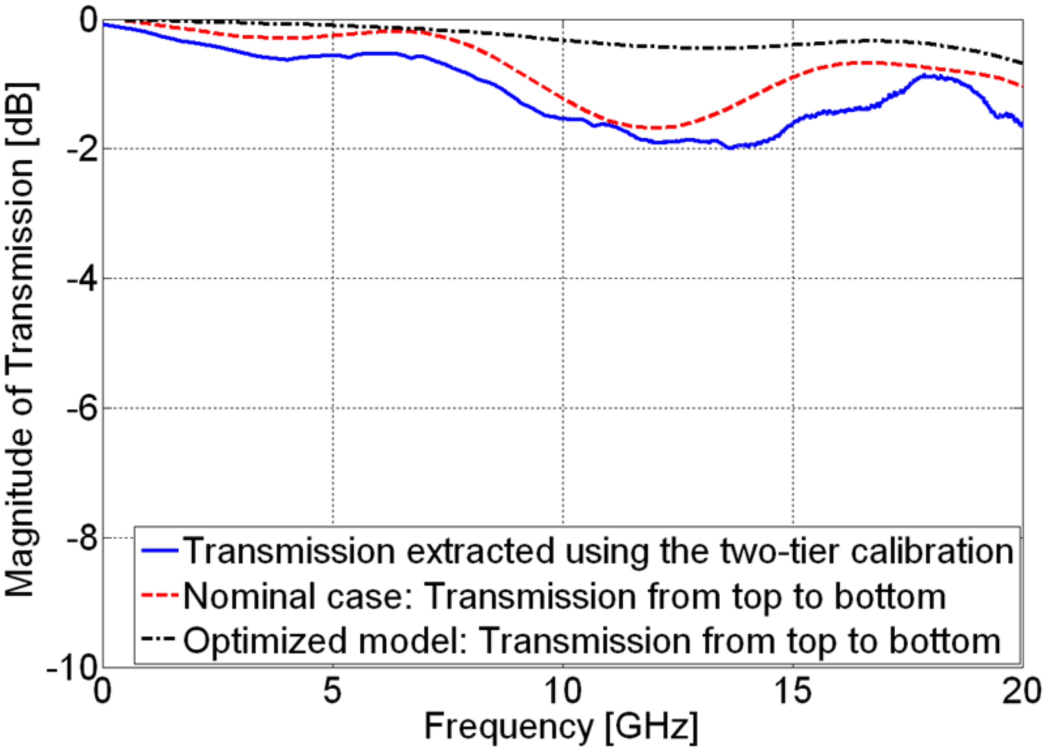


Figure 5.36 Comparison of the transmission in via 5 on the implemented SMP interposer design and on the modified model. Increasing the antipad diameters improves the transmission parameters in the entire bandwidth.

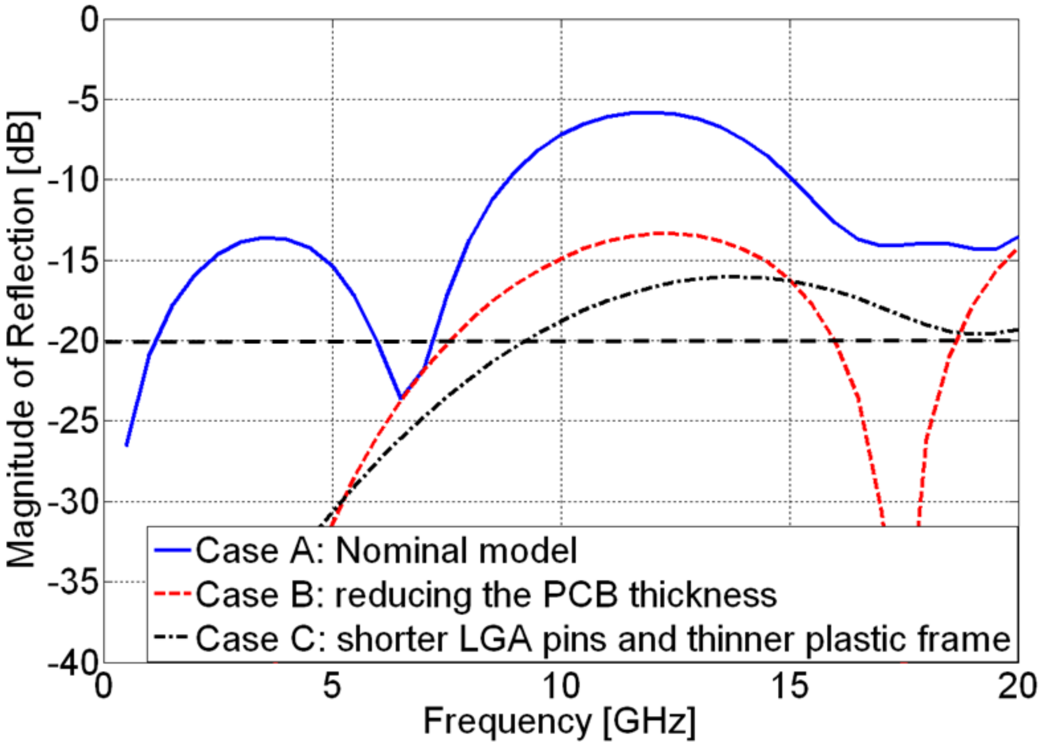


Figure 5.37 Comparison of the reflection at the SMP access via 5 on the implemented SMP interposer design and on the modified model.

In the next step, an attempt was made to reduce the capacitive discontinuities seen in the time domain analysis (Figure 5.17) where the antipad diameter of the connector access via and antipad diameter of the signal vias in the access launch via array were increased. In the nominal case (actual interposer design) the antipad diameter of the SMP signal via and the antipad diameter of the signal vias in the access via array is 33.8 mil. Three different antipad diameters are present in the optimized model: the diameter of the antipad in the upper layers of the SMP access via was increased to 64 mil where the antipad diameter in the signal layer was changed to 56 mil; the antipad diameter of the signal vias in the access via array was increased to 52 mil. Results from the comparison of the nominal case and the modified (optimized) model are depicted in Figure 5.35 and Figure 5.36. With the suggested modifications the electrical performance of the via 5 and via 6 was improved by 7 GHz in case of the reflection seen at the SMP launch side considering the -20 dB bandwidth limit (Figure 5.35). The transmission characteristics of the investigated vias are improved too where the transmission loss is reduced to approximately -0.8 dB (Figure 5.36).

Limitations imposed by the LGA socket (Figure 5.34) suggest the following potential improvements which were investigated with full wave modeling:

- shorter LGA contact pins and thinner plastic frame (Figure 5.37, case B),
- reducing the interposer PCB thickness (Figure 5.37, case C).

As illustrated in Figure 5.37 the -20 dB limit of the reflection on via 5 in the nominal case (case A) is extended by 6 GHz when the thickness of the interposer PCB is reduced from 138 mil to 79 mil where unused layers in the actual interposer design were not included to the full-wave model. Shortening the length of the LGA pins from 70 mil to 35 mil and the LGA plastic frame thickness from 55 mil to 32.5 mil extends the –20 dB bandwidth limit even by 8 GHz (case C). Further results have shown that due to the thinner interposer PCB, the shorter LGA pins and thinner plastic frame the coupling length of the signal vias in the access array can be reduced in order to decrease the crosstalk which appears in the interposer PCB. The results have shown that in case C the FEXT is reduced by -10 dB with respect to case A.

The initial idea for choosing thicker interposer PCB was caused by the expected mechanical instability when many measurement ports have to be attached to the interposer surface mounted connectors. In order to ensure good mechanical stability in multiport applications (e.g. connecting more than two measurement ports) thicker interposer PCB have to be used as in the actual design otherwise mechanical optimizations of the available clamping hardware are needed.

5.9. Summary

A novel multiport probing fixture for high frequency measurements of dense via array structures was developed in this thesis. Two basic designs and layouts of multiport interposers with SMP and SMA connector launches and access via arrays in the middle of the board edge were implemented. With help of additional mechanical and electrical tests the knowledge with regard to the force uniformity in the LGA contact pins, measurement reproducibility and limitations of the interposer application to digital link measurements was extended. The uniformity was found to be inferior in the corner via array position and is a significant impediment to accurate de-embedding of the interposer structure.

Comparing interposer based to probe based link measurement data an adequate correlation (reflection and transmission parameters) was obtained in case of links with stub access vias up to 10 GHz – 15 GHz and in case of links with shorter stub access vias the adequate correlation bandwidth is reduced to approx. 8 - 12 GHz. Poor correlation in terms of the near-end and far-end crosstalk was detected when the crosstalk of the link structure is in the range of the crosstalk in the interposer board.

Good model-to-hardware correlation was achieved considering the extracted error parameter of a via in the designed SMP interposer. Design modifications have been suggested which might extend the -20 dB limit of the reflection in the connector launch via by 7 GHz.

6. Conclusions and Outlook

This thesis has presented results from the design, application and analyses of probing and fixturing techniques for wideband multiport measurements in digital packaging. The electrical performance of the RPL and probing fixture signal launch techniques in comparison to the common coaxial surface mounted connector launch technique has been investigated in time and frequency domain measurements and with help of full-wave models. Beside the advantages with respect to the reduction of the needed spatial envelope for the measurement set up of the RPL and the probing fixture it was found that both suggested techniques represent an alternative to SMA signal launches for applications in digital packaging. Applying simple common calibration techniques and commercial and custom-made calibration standards, the RPL and the multiport interposer have been characterized and subsequently efficiently de-embedded from measurements of multilayer substrates. In summary, the scientific contributions presented in this thesis are:

- The crosstalk behavior of a high density via pin field in a connector footprint of a commercial connector embedded in a multilayer printed circuit board has been investigated in frequency domain applying surface mounted connector launch technique and a 12-port vector network analyzer (Section 3.2.1). Different via coupling scenarios were explored. The obtained results complemented and extended previous time domain investigations (Section 3.2.2).
- Multiport measurements in dense via arrays using single ended microprobes have been performed applying one and two-tier calibration techniques (Section 4). Custom-made calibration standards were developed which can be used for vertical measurements of dense via structures applying common desegmentation techniques (Section 4.2.1).
- The performance of the recessed probe launch has been explored with help of the TRL calibration algorithm. For this purposes multilayer TRL calibration standards were designed and used for the characterization of the designed recessed probe launch (Section 4.4.1). Based on the obtained results full-wave and lumped models were found which were used for sensitivity analysis, de-embedding and optimization of the designed recessed probe launch (Section 4.6). Furthermore, it was shown that the proposed signal launch can be applied for digital link

measurements with data rates up to 20 Gbit/s even without de-embedding (Section 4.7).

- The concept of a novel multiport probing fixture has been presented which allows the simultaneous connection of up to 12 measurement ports for measurements in dense via arrays on a 1 mm grid (Section 5.2). Applying simplified two-tier calibration procedure the effect of the probing fixture on measurements has been reduced and thus an alternative probing technique to the commercial single-ended microprobes and multipin probing cards/heads has been suggested (Section 5.3, Section 5.4, Section 5.7). The electrical performance study of the probing fixture let one to locate its weak points and with help of 3D full-wave electromagnetic models guidelines for its layout optimization were suggested (Section 5.5 and Section 5.8).

Based on the results obtained in this work, the different signal launch techniques can be compared to each other. The major criteria are shown in Table 6.1. The evaluation of the investigated signal launch techniques is considered with respect to the application in digital packaging and might slightly vary in other applications.

- **Bandwidth**: The criterion for the applicable bandwidth is considered from the perspective of signal integrity, when digital links have to be investigated as presented in Section 2.2. Usually in multilayer substrates to achieve adequate applicable bandwidth of coaxial surface mounted connectors (e.g. SMA, SMP) precise and careful connector launch design is required. Nevertheless the manufacturing tolerances often contribute themselves to the launch limitations. Considering the -20 dB limit, best performance was obtained by the RPL. Utilizing the suggested launch optimizations the bandwidth of the launch can be extended to 40 GHz and beyond (Section 4.6).
- **Mechanics**: The mechanics with respect to the stability of connection of measurement ports to the test devices is best in case of the SMA connector launch. The mechanical problem in case of the RPL and interposers is related to the tip placement accuracy. In case of the RPL, due to skating requirements and dimpling of the soft copper by the probe tips, it may be difficult to either ascertain the location of the probe tips or to reproducibly their position, especially when they are worn. Skating effects of the contact pins of the LGA array can occur if the LGA plastic frame is not properly fixed in the clamping hardware and the applied pressure is not sufficient.
- **Repeatability:** Measurements applying the SMA launch and RPL techniques showed better repeatability in comparison to those performed with the available interposer hardware (sensitive to behavior of clamping and LGA). With respect to the calibration repeatability the three launches have shown adequate results.

TABLE 6.1 EVALUATION OF THE INVESTIGATED SIGNAL LAUNCH TECHNIQUES

	SMA launch	RPL	Interposer
Applicable bandwidth	18 - 26 GHz	40 - 50 GHz	potentially 20 GHz
Mechanics	very good	good	need further optimization
Repeatability	very good	very good	adequate
Calibration substrates	custom-made (PCB, inexpensive)	commercial or custom-made	custom-made (expensive)
Calibration algorithm	common	common/ custom-made	common/ custom-made
Calibration effort	easy	difficult	easy
Costs in € per signal launch	10 - 50	500 - 1000	> 1000
Handling	common and easy to use	requires experience	easy to use

- **Calibration substrates:** Commercial calibration substrates are available in case of the SMA coaxial connector and the RF microprobes which can be purchased from the VNA and microprobe manufacturer. For complete calibration of the designed SMA launch, the RPL, and the interposer custom-made substrates are needed. In case of the interposer, the custom-made calibration substrates have to be additionally characterized in probe-based measurements (Section 5.3 and Section 5.4).
- **Calibration algorithm**: In case of the SMA and common microprobe launches, typically firmware available in the measurement equipment can be used. As presented in Section 5.4 additional Matlab calibration tools are required for the interposer calibration.
- **Calibration effort**: In contrast to the RPL technique the surface mounted connector and interposer calibration procedures are easier and less time consuming.
- **Costs**: The most expensive is the interposer launch technique due to the fact that it is custom-made and application specific. Which technique from the surface mounted connector and microprobe based is more expensive is not so clear. In

case of the hardware used at TET, the costs for the microprobes were more than those for the SMA launch technique (SMA adapters and cables do not become obsolete so fast).

- **Handling**: With respect to the needed experience for the application of the launches the interposer is handier than the other two. Indeed, microprobes demand the most experience and competence.

Further improvement of the recessed probe technique and the proposed multiport interposers is necessary in order to ensure applicability to digital systems which are driven at higher data rates e.g. 20 Gbit/s and beyond. Recommendations for future work encompass first of all the RPL and the multiport interposer probing techniques due to their advantages in contrast to the conventional coaxial connector probing techniques. In case of the recessed probe launch technique, besides the suggested layout modifications tests with improved probe designs can be beneficial for the consolidation of the obtained results. The sensitivity of the RPL with respect to the cavity size could not be investigated in detail. Initial tests at the Institute of Electromagnetic Theory, had indicated that with the help of a new milling machine (±10 µm milling precision) effects seen in models could be reconstructed. The application of the RPL for measurements in multilayer PCBs where multiport microprobes e.g. dual probes for differential measurements are used could be interesting.

In case of the multiport interposer, the suggested layout modifications will improve the applicable measurement bandwidth of the actual interposer designs. The application of calibration algorithms which include crosstalk error terms might extend the measurement bandwidth of the available interposer designs. An appropriate commercial calibration software called MMS4 (Multiport S-parameters Software, [136]) is newly available at the Institute. Additionally, the development of alternative signal launch techniques e.g. mounting of spring contacts (pogo pins) is expected to be crucial as contact repeatability will have to be improved in the next interposer design. In that regard mechanical simulations using FEM solvers can be helpful in identifying the weak points of the utilized mechanical clamping hardware.

A. Appendix

A.1 Signal Bandwidth in High Speed Interconnects

In general, the signal rise time T_r can be estimated from the data rate (DR) of the idealized waveform of a digital signal. Starting from the bit time T_b, the ratio between DR and a bit time corresponds to:

$$T_b = \frac{1}{DR}. \qquad (1.1)$$

The fundamental frequency is defined as

$$f_s = \frac{1}{T_{signal}} = \frac{1}{2 \cdot T_b}. \qquad (1.2)$$

Typically, T_r is approximately about $0.1 \cdot T_{signal}$ and the maximum frequency content of the digital signal corresponds to the ratio

$$F_{\max} \sim \frac{1}{T_r}. \qquad (1.3)$$

In other words, e.g. in case of signal data rate of 10 Gbit/s the fundamental frequency is 5 GHz, $T_r \approx 20ps$ and $F_{\max} = 50\,\mathrm{GHz}$. Considering the fact that most energy in digital pulses concentrates below the so-called knee frequency f_{knee} another rule of thumb for estimation of the maximum frequency content is [27], [137]:

$$F_{\max} = f_{knee} = \frac{0.5}{T_r}. \qquad (1.4)$$

Thus for DR of 10 Gbit/s the value of $F_{\max}$ is only 25 GHz.

A.2 The Short-Open-Load Calibration

The Short-Open-Load calibration algorithm is a fundamental calibration technique for one port VNAs. It is based on the reflectometer equation (Figure A.3.1) [43]:

$$S_{11meas} = M = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{DUT}}{1 - e_{11} \cdot \Gamma_{DUT}} \tag{2.1}$$

The computation of the error coefficients is related to the measurements of the three known standards Γ_{short}, Γ_{open} and Γ_{load} and their characteristic data (correction coefficients) which can be found in the data sheets provided by the calibration standards manufacturer.

Common definitions in case of coaxial terminations for the three standards can be described in S-parameter in relation to the correction coefficients as shown below [43].

Under consideration of the correction coefficients for the short standards a typical short termination is defined as an inductance with:

$$L_e(f) = L_0 + L_1 \cdot f + L_2 \cdot f^2 + L_3 \cdot f^3, \text{ and} \tag{2.2}$$

$$S_{11} = \Gamma_{short} = \frac{j2 \cdot \pi \cdot f \cdot L_e(f) - Z_0}{j2 \cdot \pi \cdot f \cdot L_e(f) + Z_0} \cdot e^{-\frac{j4\pi}{\lambda} \cdot l} . \tag{2.3}$$

Using the correction parameters of the open standard the open termination is defined as a capacitance with:

$$C_e(f) = C_0 + C_1 \cdot f + C_2 \cdot f^2 + C_3 \cdot f^3, \text{ and} \tag{2.4}$$

$$S_{11} = \Gamma_{open} = \frac{1 - j2 \cdot \pi \cdot f \cdot Z_0 \cdot C_e(f)}{1 + j2 \cdot \pi \cdot f \cdot Z_0 \cdot C_e(f)} \cdot e^{-\frac{j4\pi}{\lambda} \cdot l} . \tag{2.5}$$

The load termination is defined usually as 50 Ohm and so far approximately as:

$$S_{11} = \Gamma_{load} = 0 . \tag{2.6}$$

In case of calibration substrates for GSG microprobes used for the measurements applying the RPL technique the lumped models illustrated in Figure A.3.2. were used for the computation of the expected S-parameters of Γ_{short}, Γ_{open}, and Γ_{load}.

After measurement of the three terminations one can define three equations:

$$M_{open} = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{open}}{1 - e_{11} \cdot \Gamma_{open}}, \tag{2.2}$$

$$M_{short} = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{short}}{1 - e_{11} \cdot \Gamma_{short}}, \qquad \text{and} \tag{2.3}$$

$$M_{load} = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{load}}{1 - e_{11} \cdot \Gamma_{load}}. \tag{2.4}$$

With respect to all these equations the error coefficients can be computed for the system of three independent linear equations. If desired the term $e_{10} \cdot e_{01}$ can be split as shown in Section A.5 (eq. 4.39 - 4.54) or one can assume that $e_{01} = 1$ and then the equations can be simplified, too.

A.3 Two-tier Calibration

The two-tier calibration technique is a common measurement technique which is usually used for extraction of measurement fixtures (e.g. adapters, microprobes, probing fixtures, etc) from measurements [130], [131]. In [8] an application of the two-tier calibration method was presented where the error parameters (S-parameters) of microprobes and RPLs were extracted with help of this technique and later on applied to measurements on multilayer PCBs.

As shown in [8], the first tier (coaxial SOLT calibration) is usually performed for the removal of the measurement errors of the measurement set up (vector network analyzer and cables) and the second tier calibration is used for the extraction of two-port error parameters of microprobes and/or RPLs (Figure A.3.3). For the extraction of the error parameters of two RPLs using the TRL calibration algorithm a dedicated multilayer PCB is used which contains uniform recessed probe launch structures and 50 Ohm line standards allowing the calibration in the bandwidth between 3.8 GHz and 19 GHz. The extracted RPL error parameters are depicted in Figure A.3.4 and Figure A.3.5. It is important to note that the microprobes were calibrated on the microprobe vendor calibration substrate (CS-5, Al_2O_3, $\varepsilon_r = 9.8$). If the calibration tier for removing the effect of the microprobes is not desired, one can perform in the second tier the TRL calibration on the PCB calibration board and thus to extract the combined error parameters (probe + RPL) as shown in Figure A.3.6 and Figure A.3.7. For validation of this procedure, the separate error parameters of the utilized microprobes and their according RPLs were concatenated and correlated to the case with the combined error parameters (Figure 3.8, Figure A.3.9 and Figure A.3.10).

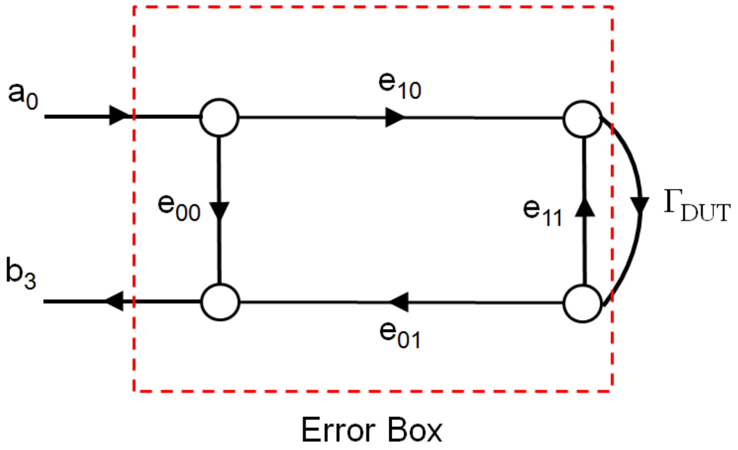


Figure A.3.1 Signal flow graph of the error terms of one port VNA measurement.

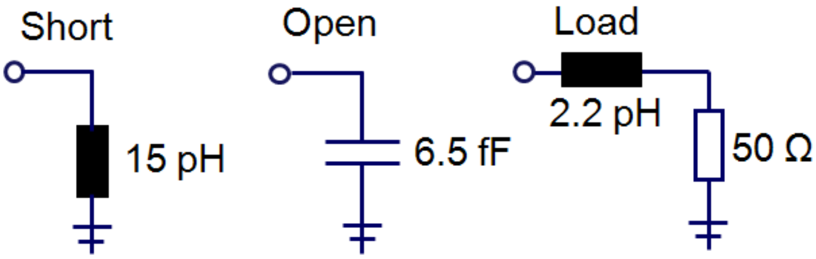


Figure A.3.2 Lumped models used for characterization of the calibration standards on the alumina substrate CS-5 ([24]) and computation of the expected S-parameters.

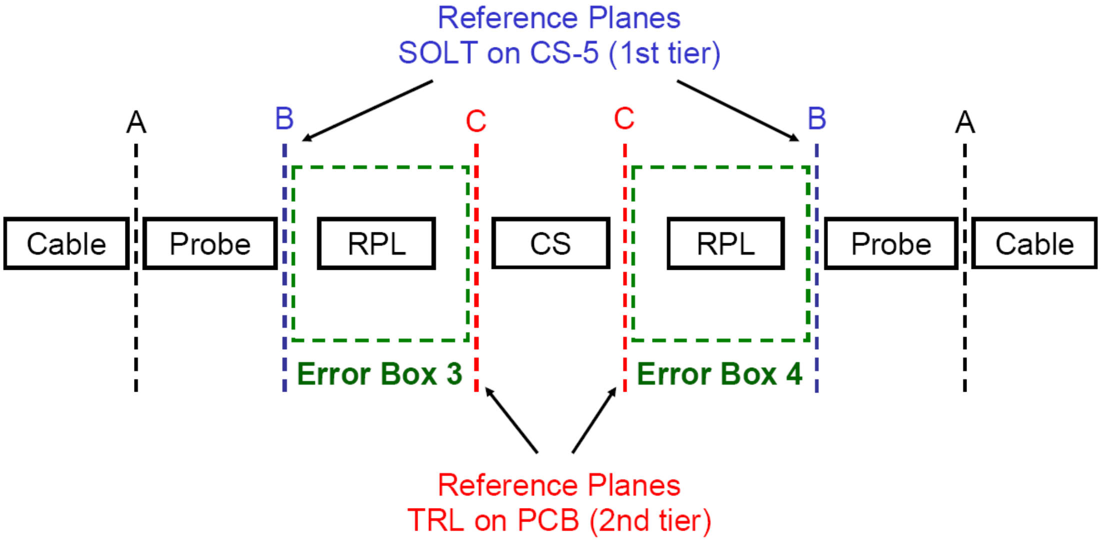


Figure A.3.3 Connectivity of the extracted error boxes of the two RPLs. The second tier was used for the extraction of error boxes due to differences between the first and second calibration [7].

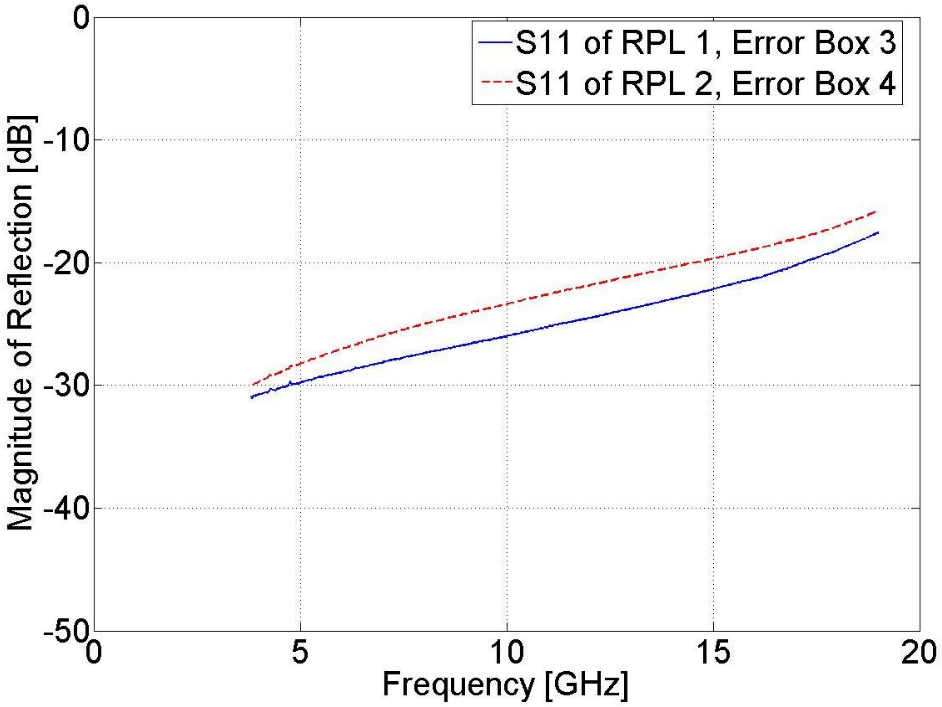


Figure A.3.4 Return loss of RPL extracted with 220 mil long line standard using 90 mil thru line standard [7].

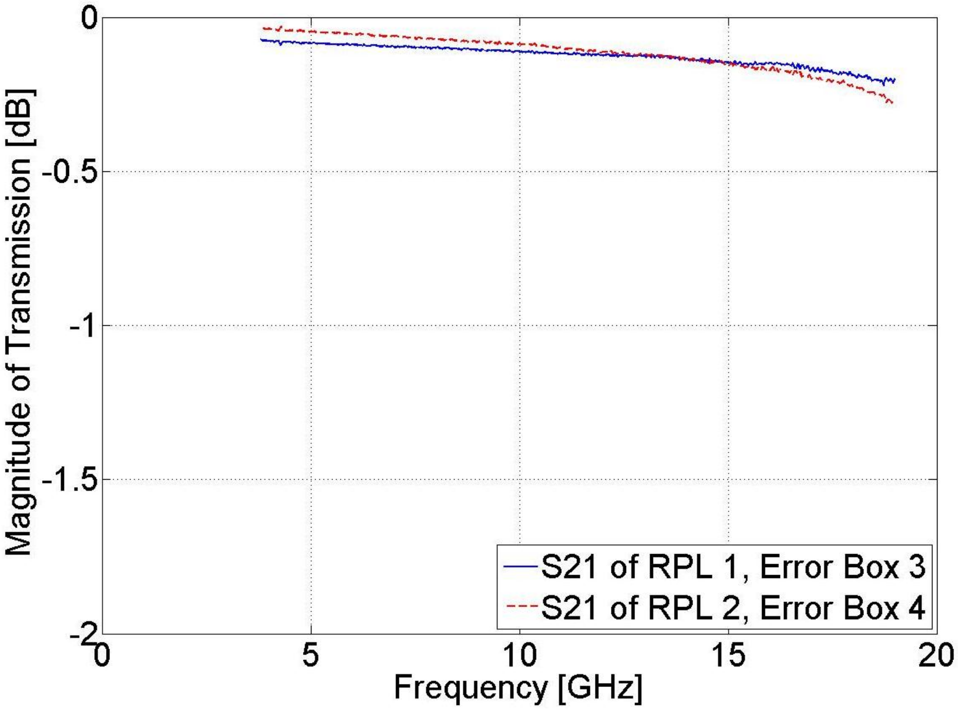


Figure A.3.5 Insertion loss of RPL extracted with 220 mil long line standard using 90 mil thru line standard [7].

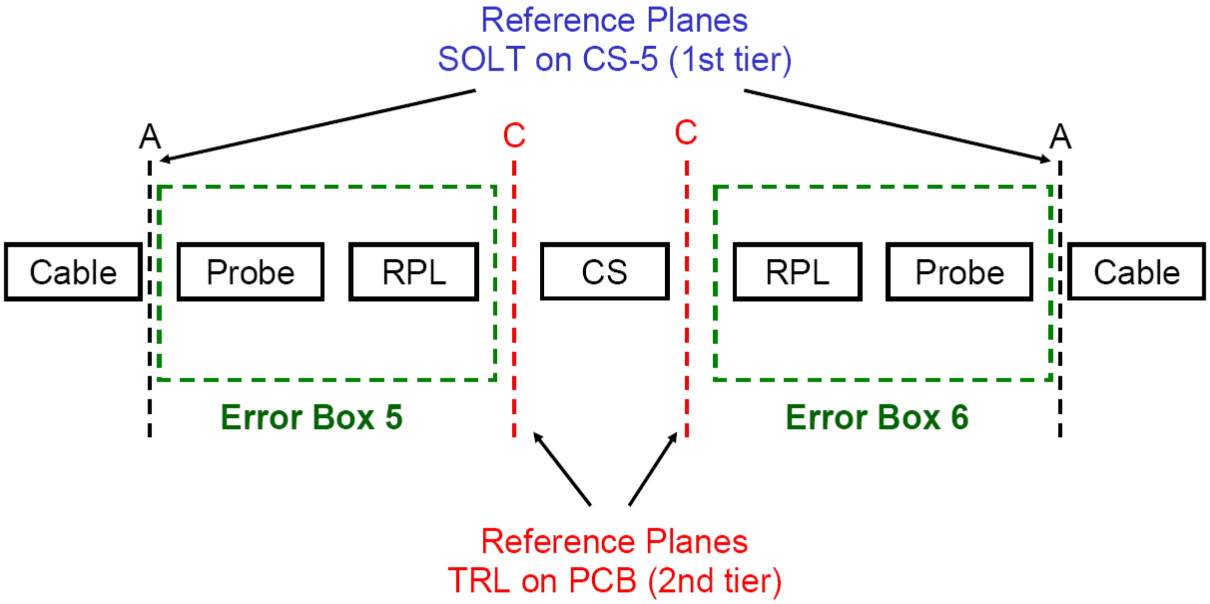


Figure A.3.6 Connectivity of the combined extracted error boxes of microprobes and RPLs. Here, the second tier consists of a TRL calibration performed on the PCB, whereas the first tier is the coaxial SOLT [7].

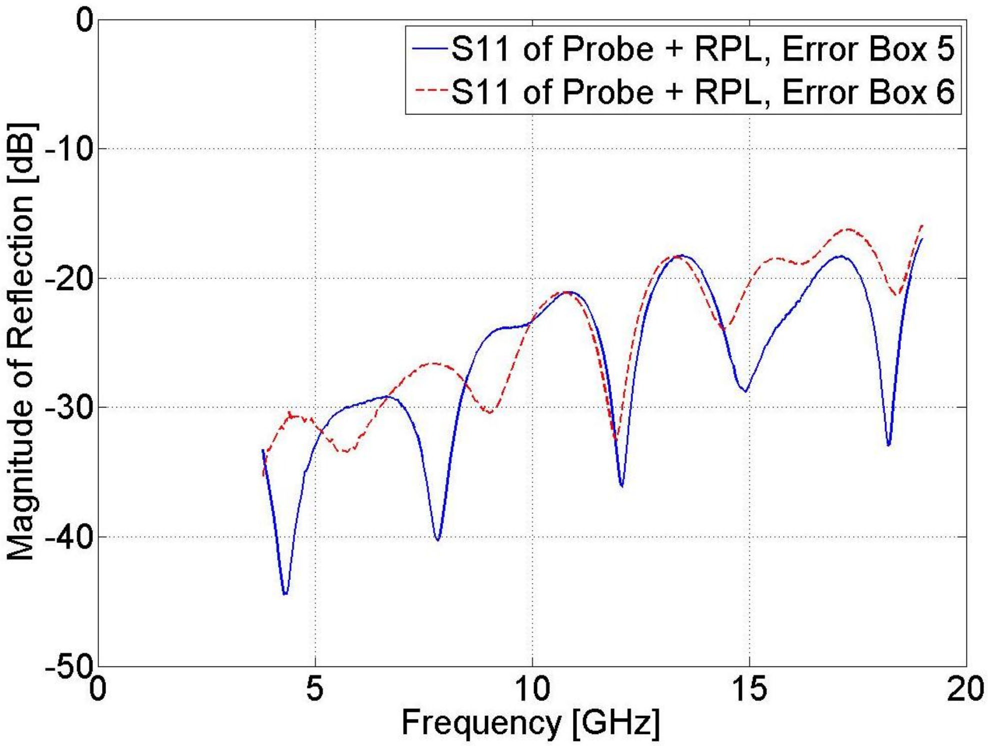


Figure A.3.7 Return loss of the combined error boxes for the microprobes and RPLs extracted from TRL calibration on PCB [7].

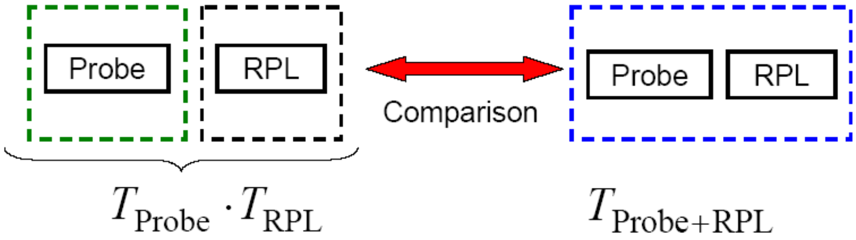


Figure A.3.8 Principle of comparison between cascaded error boxes and combined error box of microprobe and RPL [7].

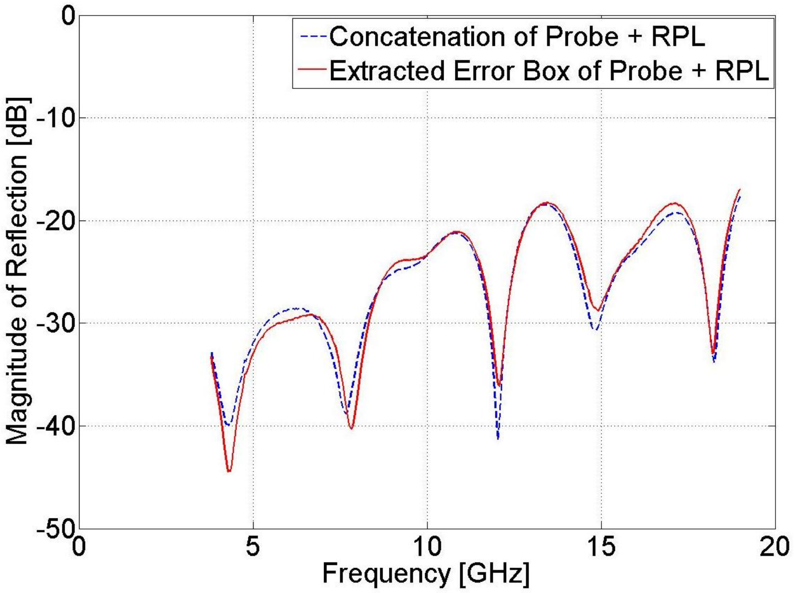


Figure A.3.9 Comparison of return loss in case of combined error box of microprobe and RPL and cascading of two separate error boxes for the microprobe and the RPL, respectively [7].

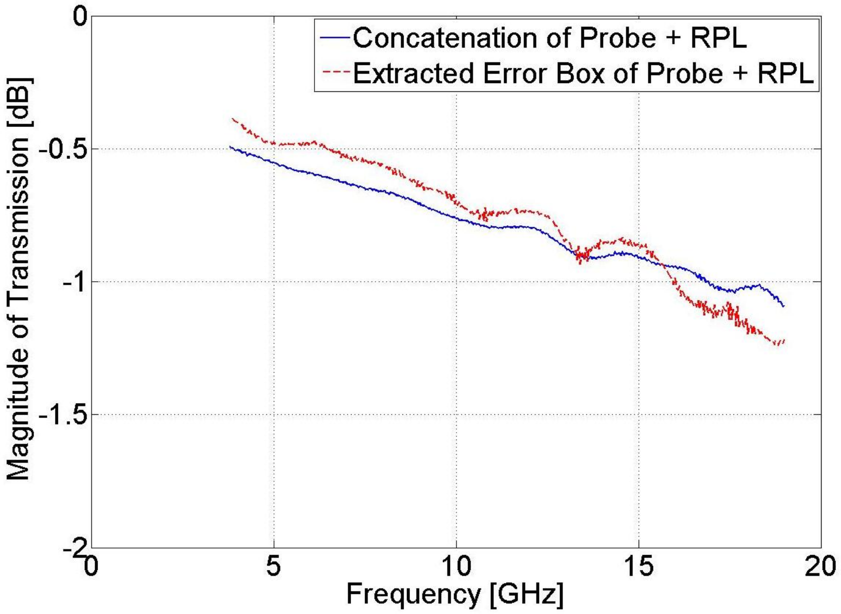


Figure A.3.10 Comparison of insertion loss of the two types of error boxes, the maximum difference is less than 0.2 dB [7].

This last comparison shows that the concatenated error boxes are comparable to the fully extracted error boxes which include the microprobes and the RPLs. Even though the error parameters of the microprobe and RPL have been computed from different calibration standards, close correlation in the return loss and transmission parameters can be observed. Obviously, the calibration procedures are applicable either in individual steps or in one combined step.

A.4 De-embedding Using Desegmentation

The desegmentation as known in network theory is a technique for “subtraction” of multiport networks where the characteristic of an unknown multiport component can be derived from the characteristics of other two known components. The general idea of this method is shown in Figure A.4.11 where the unknown α-network (DUT) can be extracted from the measured data (“$\alpha+\beta$”) when the S-parameters of the fixture used (β) are known. The desegmentation method extracts either the S-matrix or Z-matrix of an α-network from known S- or Z-matrices of γ- and β-networks where the γ-network has to be composed of the α- and β-networks.

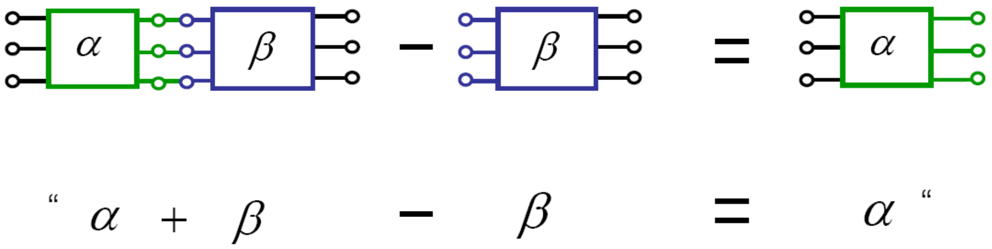


Figure A.4.11 General idea of the desegmentation method: When a known γ-network is composed of two other networks ($\alpha+\beta$) and one of them is known (β), by subtraction of the known networks the unknown αα-network can be obtained ($\alpha=\gamma-\beta$) [10].

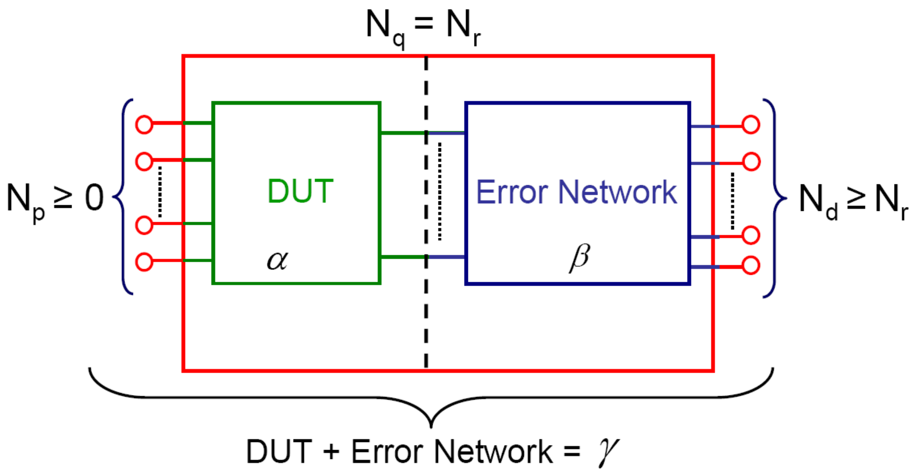


Figure A.4.12 Desegmentation applied to de-embedding: The γγ-network (embedded DUT) is composed of the αα- and ββ-networks (de-embedded DUT and error network, respectively). When the γγ- and ββ-networks are known, the αα-network can be extracted [10].

The desegmentation method is used for error network de-embedding from S-parameter measurements obtained by a vector network analyzer (Figure A.4.12). It is important to note that the numbers of ports (N_p, N_q, N_r, N_d) might be quite different from each other which increases the flexibility of the approach. Specifically, the number of ports of the error network can be smaller than the number of ports for the DUT. The outline of the method is given in the following with the restriction that the number of d-ports is equal to the number of q-ports (error network has as many input as output ports).

In general the definition of the S-matrices is expressed as:

$$S^{\gamma}: \qquad \begin{bmatrix} b_p \\ b_d \end{bmatrix} = \begin{bmatrix} S_{pp}^{\gamma} & S_{pd}^{\gamma} \\ S_{dp}^{\gamma} & S_{dd}^{\gamma} \end{bmatrix} \begin{bmatrix} a_p \\ a_d \end{bmatrix}, \tag{4.1}$$

$$S^{\beta}: \qquad \begin{bmatrix} b_r \\ b_d \end{bmatrix} = \begin{bmatrix} S_{rr}^{\beta} & S_{rd}^{\beta} \\ S_{dr}^{\beta} & S_{dd}^{\beta} \end{bmatrix} \begin{bmatrix} a_r \\ a_d \end{bmatrix}, \tag{4.2}$$

$$S^{\alpha}: \qquad \begin{bmatrix} b_p \\ b_d \end{bmatrix} = \begin{bmatrix} S_{pp}^{\alpha} & S_{pq}^{\alpha} \\ S_{qp}^{\alpha} & S_{qq}^{\alpha} \end{bmatrix} \begin{bmatrix} a_p \\ a_q \end{bmatrix}. \tag{4.3}$$

The submatrices in S^{α} are found as:

$$S_{qq}^{\alpha} = \left(NS_{rr}^{\beta} + I\right)^{-1} N, \tag{4.4}$$

$$S_{pq}^{\alpha} = S_{pd}^{\gamma}\left(S_{rd}^{\beta}\right)^{-1}\left(I - S_{rr}^{\beta}\left(NS_{rr}^{\beta} + I\right)^{-1} N\right)\left(S_{rd}^{\beta}\right)^{-1}\left(I - S_{rr}^{\beta}\left(NS_{rr}^{\beta} + I\right)^{-1} N\right), \tag{4.5}$$

$$S_{qp}^{\alpha} = \left(I - \left(NS_{rr}^{\beta} + I\right)^{-1} NS_{rr}^{\beta}\right)\left(\left(S_{dr}^{\beta}\right)^{t} S_{dr}^{\beta}\right)^{-1}\left(S_{dr}^{\beta}\right)^{t} S_{dp}^{\gamma}, \qquad \text{and} \tag{4.6}$$

$$S_{pp}^{\alpha} = S_{pp}^{\gamma} - S_{pq}^{\alpha} S_{rr}^{\beta}\left(I - \left(NS_{rr}^{\beta} + I\right)^{-1} NS_{rr}^{\beta}\right)^{-1} S_{qp}^{\alpha}, \tag{4.7}$$

where I is the identity matrix and:

$$N = \left(S_{dr}^{\beta}\right)^{-1}\left(S_{dd}^{\gamma} - S_{dd}^{\beta}\right)\left(S_{rd}^{\beta}\right)^{-1}. \tag{4.8}$$

Considering the case of a 2-port network as shown in Figure A.4.13, the elements of S^{α} are the following:

$$S_{11}^{\alpha}=\frac{S_{11}^{\gamma}\left(S_{21}^{\gamma}\right)^{-1}\left(S_{22}^{\gamma}S_{11}^{\beta}-S_{22}^{\beta}S_{11}^{\beta}+S_{21}^{\beta}S_{12}^{\beta}\right)-S_{12}^{\gamma}S_{11}^{\beta}}{S_{11}^{\beta}\left(S_{21}^{\gamma}\right)^{-1}\left(S_{22}^{\gamma}-S_{22}^{\beta}\right)+\left(S_{21}^{\gamma}\right)^{-1}S_{21}^{\beta}S_{12}^{\beta}}, \tag{4.9}$$

$$S_{12}^{\alpha}=\frac{S_{12}^{\gamma}S_{21}^{\beta}}{S_{11}^{\beta}\left(S_{22}^{\gamma}-S_{22}^{\beta}\right)+S_{21}^{\beta}S_{12}^{\beta}}, \tag{4.10}$$

$$S_{21}^{\alpha}=\frac{\left(S_{21}^{\beta}\right)^{-1}S_{21}^{\gamma}}{S_{22}^{\beta}\left(S_{21}^{\beta}\right)^{-1}\left(S_{12}^{\beta}\right)^{-1}\left(S_{22}^{\gamma}-S_{22}^{\beta}\right)+1}, \quad \text{and} \tag{4.11}$$

$$S_{22}^{\alpha}=\frac{\left(S_{21}^{\beta}\right)^{-1}\left(S_{22}^{\gamma}-S_{22}^{\beta}\right)\left(S_{12}^{\beta}\right)^{-1}}{S_{11}^{\beta}\left(S_{21}^{\beta}\right)^{-1}\left(S_{12}^{\beta}\right)^{-1}\left(S_{22}^{\gamma}-S_{22}^{\beta}\right)+1}. \tag{4.12}$$

The desegmentation method explained here can be used for de-embedding of multiport networks equivalent to the procedure when the T-matrices of networks are applied. In order to prove that for the case depicted in Figure A.4.13, the S-parameter matrices have to be first transformed to their equivalent T-parameter matrices using the generalized definition for an n-port network [48]. Using the well known definition:

$$T=\begin{bmatrix} S_{12}-S_{11}S_{21}^{-1}S_{22} & S_{11}S_{21}^{-1} \\ -S_{21}^{-1}S_{22} & S_{21}^{-1} \end{bmatrix}, \tag{4.13}$$

The T-matrix of the α-network with respect to Figure A.4.13 can then be extracted as follows:

$$T^{\alpha}=T^{\gamma}\left(T^{\beta}\right)^{-1}. \tag{4.14}$$

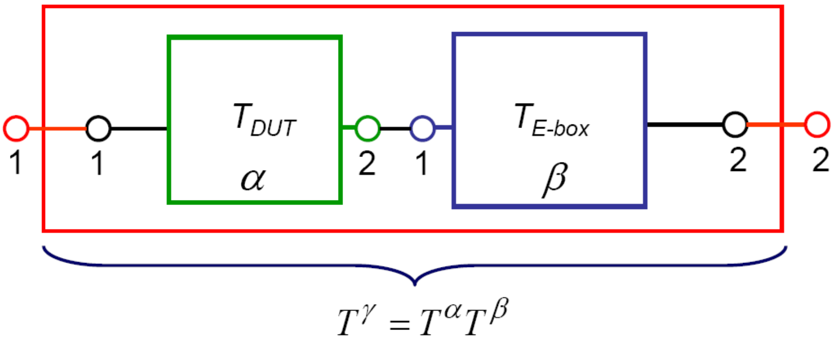


Figure A.4.13 T-matrix formulation for cascaded 2-port networks [10].

For the network shown in Figure A.4.13 the matrices T^{γ} and T^{β} are expressed as:

$$T^{\gamma} = \begin{bmatrix} S_{12}^{\gamma} - S_{11}^{\gamma}\left(S_{21}^{\gamma}\right)^{-1} S_{22}^{\gamma} & S_{11}^{\gamma}\left(S_{21}^{\gamma}\right)^{-1} \\ -\left(S_{21}^{\gamma}\right)^{-1} S_{22}^{\gamma} & \left(S_{21}^{\gamma}\right)^{-1} \end{bmatrix} \qquad \text{and} \tag{4.15}$$

$$T^{\beta} = \begin{bmatrix} S_{12}^{\beta} - S_{11}^{\beta}\left(S_{21}^{\beta}\right)^{-1} S_{22}^{\beta} & S_{11}^{\beta}\left(S_{21}^{\beta}\right)^{-1} \\ -\left(S_{21}^{\beta}\right)^{-1} S_{22}^{\beta} & \left(S_{21}^{\beta}\right)^{-1} \end{bmatrix}. \tag{4.16}$$

Inversion of T^{β} yields:

$$\left(T^{\beta}\right)^{-1} = \begin{bmatrix} \left(S_{12}^{\beta}\right)^{-1} & -S_{11}^{\beta}\left(S_{12}^{\beta}\right)^{-1} \\ S_{22}^{\beta}\left(S_{12}^{\beta}\right)^{-1} & \left(S_{12}^{\beta} - S_{11}^{\beta}\left(S_{21}^{\beta}\right)^{-1} S_{22}^{\beta}\right) S_{21}^{\beta}\left(S_{12}^{\beta}\right)^{-1} \end{bmatrix}. \tag{4.17}$$

Inserting (4.15) and (4.17) into (4.14) yields:

$$T_{11}^{\alpha} = \left(S_{12}^{\gamma} + S_{11}^{\gamma}\left(S_{21}^{\gamma}\right)^{-1}\left(S_{22}^{\beta} - S_{22}^{\gamma}\right)\right)\left(S_{12}^{\beta}\right)^{-1}, \tag{4.18}$$

$$T_{12}^{\alpha} = \left(-S_{11}^{\beta} S_{12}^{\gamma} + S_{11}^{\gamma}\left(S_{21}^{\gamma}\right)^{-1}\left(S_{22}^{\gamma} S_{11}^{\beta} + S_{21}^{\beta} S_{12}^{\beta} - S_{22}^{\beta} S_{11}^{\beta}\right)\right)\left(S_{12}^{\beta}\right)^{-1}, \tag{4.19}$$

$$T_{21}^{\alpha} = \left(\left(S_{21}^{\gamma}\right)^{-1}\left(S_{22}^{\beta} - S_{22}^{\gamma}\right)\right)\left(S_{12}^{\beta}\right)^{-1}, \text{ and} \tag{4.20}$$

$$T_{22}^{\alpha} = \left(\left(S_{21}^{\gamma}\right)^{-1} S_{11}^{\beta}\left(S_{22}^{\gamma} - S_{22}^{\beta}\right) + \left(S_{21}^{\gamma}\right)^{-1} S_{12}^{\beta} S_{21}^{\beta}\right)\left(S_{12}^{\beta}\right)^{-1}. \tag{4.21}$$

Using the T- to S-parameter transformation by the well known relations:

$$S = \begin{bmatrix} T_{12}T_{22}^{-1} & T_{11} - T_{12}T_{22}^{-1}T_{21} \\ T_{22}^{-1} & -T_{22}^{-1}T_{21} \end{bmatrix}, \tag{4.22}$$

and considering the port definitions in Figure A.4.13 the unknown S^{α} can be expressed as:

$$S^{\alpha} = \begin{bmatrix} T_{12}^{\alpha}\left(T_{22}^{\alpha}\right)^{-1} & T_{11}^{\alpha} - T_{12}^{\alpha}\left(T_{22}^{\alpha}\right)^{-1}T_{21}^{\alpha} \\ \left(T_{22}^{\alpha}\right)^{-1} & -\left(T_{22}^{\alpha}\right)^{-1}T_{21}^{\alpha} \end{bmatrix}. \tag{4.23}$$

Inserting (4.18) – (4.21) into (4.23) yields exactly (4.9) – (4.12). So after the T- to S-parameter transformation the same expressions for the de-embedded DUT as in the desegmentation method are obtained.

The main advantage of the de-embedding by desegmentation technique is that it does not require any S- to T-parameters conversion and - if desired - allows stepwise extraction of the embedded error networks. It is important to note that in this approach all matrices have to be of the same size, i.e. the error network has to have the same number of ports as the embedded DUT. In multiport set ups (number of ports between 4 and 12) this can be cumbersome, especially when some ports need to be de-embedded and others not.

A.5 The Thru-Reflect-Line Calibration

The matrix relations below were mainly explained in [47], [110] and were implemented in the Matlab tool called “ebx” used for the error box extractions in this thesis.

The measured S-parameters of the three standards - thru, line and reflect - can be described in T-matrix form with the following relations:

$$T_{Thru} = T_t = T_x \cdot T_y \quad \text{and} \tag{5.1}$$

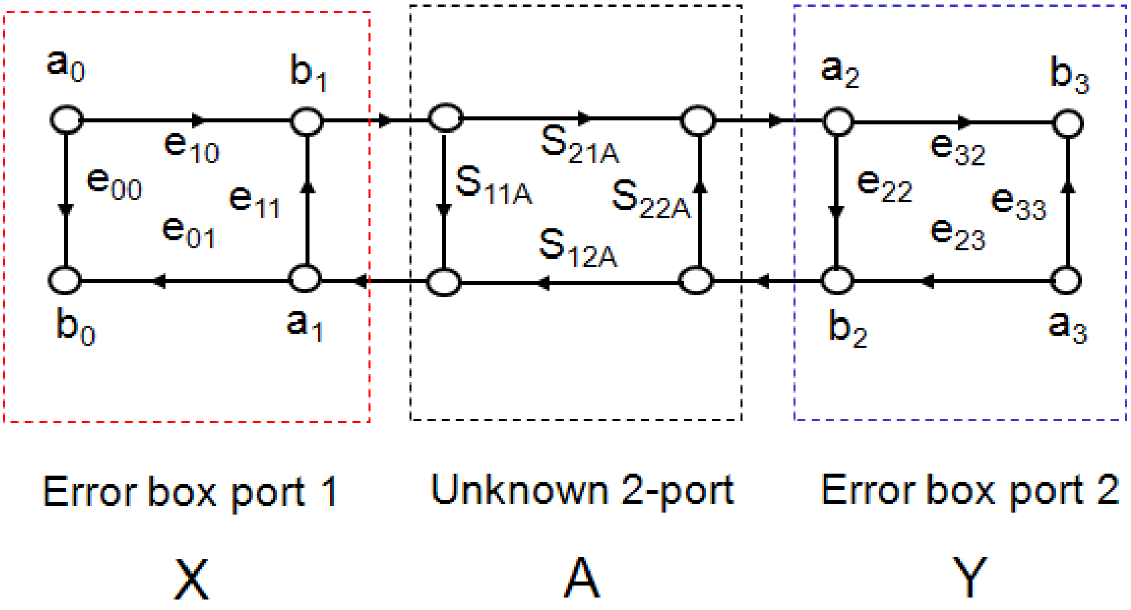


Figure A.5.14 Signal flow graph of the 2-port Thru-Reflect-Line calibration.

$$T_{Line} = T_d = T_x \cdot T_l \cdot T_y . \tag{5.2}$$

Applying the following matrix relations for the computation of T_x leads to

$$T_y = T_x^{-1} \cdot T_t , \tag{5.3}$$

$$T_d = T_x \cdot T_l \cdot T_x^{-1} \cdot T_t \quad , \tag{5.4}$$

$$T_d \cdot T_t^{-1} = T_x \cdot T_l \cdot T_x^{-1} \cdot T_t \cdot T_t^{-1} , \tag{5.5}$$

$$T_d \cdot T_t^{-1} \cdot T_x = T_x \cdot T_l \cdot T_x^{-1} \cdot T_x , \tag{5.6}$$

$$T_d \cdot T_t^{-1} \cdot T_x = T_x \cdot T_l . \tag{5.7}$$

Considering the signal flow graph in Figure A.5.14 the submatrices are

$$T_X = \frac{1}{e_{10}} \begin{pmatrix} e_{10}e_{01} - e_{00}e_{11} & e_{00} \\ -e_{11} & 1 \end{pmatrix} , \tag{5.8}$$

$$T_Y = \frac{1}{e_{32}} \begin{pmatrix} e_{32}e_{23} - e_{22}e_{33} & e_{22} \\ -e_{33} & 1 \end{pmatrix} , \quad \text{and} \tag{5.9}$$

$$T_M = \frac{1}{S_{21M}} \begin{pmatrix} S_{21M} S_{12M} - S_{11M} S_{22M} & S_{11M} \\ -S_{22M} & 1 \end{pmatrix} . \tag{5.10}$$

Let us assume that the T-matrices of the thru and line standards behave like

$$T_{Thru} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \qquad \text{and} \tag{5.11}$$

$$T_{Line} = \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{\gamma l} \end{pmatrix} . \tag{5.12}$$

In general, $T_{12} = T_{21} = 0$ means that the lines are matched. Then,

$$T_{ml} \cdot T_{mt}^{-1} \cdot T_X = T_X \cdot T_l \quad , \tag{5.13}$$

$$M \cdot T_X = T_X \cdot T_l \quad , \qquad \text{with} \tag{5.14}$$

$$\begin{pmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{pmatrix} \cdot \begin{pmatrix} x_{11} & x_{12} \\ x_{21} & x_{22} \end{pmatrix} = \begin{pmatrix} x_{11} & x_{12} \\ x_{21} & x_{22} \end{pmatrix} \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{\gamma l} \end{pmatrix} . \tag{5.15}$$

This leads to

$$m_{11} \cdot x_{11} + m_{12} \cdot x_{21} = x_{11} \cdot e^{-\gamma l} \tag{5.16}$$

$$m_{21} \cdot x_{11} + m_{22} \cdot x_{12} = x_{21} \cdot e^{-\gamma l} \tag{5.17}$$

$$m_{11} \cdot x_{12} + m_{12} \cdot x_{22} = x_{12} \cdot e^{\gamma l} \tag{5.18}$$

$$m_{21} \cdot x_{12} + m_{22} \cdot x_{22} = x_{22} \cdot e^{\gamma l} . \tag{5.19}$$

Dividing Eq. (5.16) by (5.17) and Eq. (5.18) by (5.19) yields

$$m_{21} \cdot \left(\frac{x_{11}}{x_{21}} \right)^2 + \left(m_{22} - m_{11} \right) \cdot \left(\frac{x_{11}}{x_{21}} \right) - m_{12} = 0 \qquad \text{and} \tag{5.20}$$

$$m_{21} \cdot \left(\frac{x_{12}}{x_{22}} \right)^2 + \left(m_{22} - m_{11} \right) \cdot \left(\frac{x_{12}}{x_{22}} \right) - m_{12} = 0 . \tag{5.21}$$

Note: The solutions for the quadratic equations are the same and for typical reflectometer a > b holds. This gives

$$\frac{x_{11}}{x_{21}} = a = e_{00} - \frac{(e_{10}e_{01})}{e_{11}} \qquad \text{and} \tag{5.22}$$

$$\frac{x_{12}}{x_{22}} = \underline{\underline{b = e_{00}}} \qquad \text{, will} \tag{5.23}$$

$$\frac{(e_{10}e_{01})}{e_{11}} = a - b\,. \tag{5.24}$$

The same can be applied to T_Y:

$$T_Y \cdot N = T_l \cdot T_Y \qquad \text{and} \tag{5.25}$$

$$N = T_{mt}^{-1} \cdot T_{ml} \qquad \text{, will} \tag{5.26}$$

$$\begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \cdot \begin{pmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{\gamma l} \end{pmatrix} \tag{5.27}$$

This again leads to

$$y_{11} \cdot n_{11} + y_{12} \cdot n_{21} = y_{11} \cdot e^{-\gamma l} \tag{5.28}$$

$$y_{21} \cdot n_{11} + y_{22} \cdot n_{21} = y_{21} \cdot e^{-\gamma l} \tag{5.29}$$

$$y_{11} \cdot n_{12} + y_{12} \cdot n_{22} = y_{12} \cdot e^{\gamma l} \tag{5.30}$$

$$y_{21} \cdot n_{12} + y_{22} \cdot n_{22} = y_{22} \cdot e^{\gamma l}\,. \tag{5.31}$$

Dividing Eq. (4.28) by (4.29) and Eq. (4.30) by (4.31) leads to

$$n_{12} \cdot \left(\frac{y_{11}}{y_{12}}\right)^2 + (n_{22} - n_{11}) \cdot \left(\frac{e_{00}}{e_{10}}\right) - n_{21} = 0\,, \tag{5.32}$$

$$n_{12} \cdot \left(\frac{y_{21}}{y_{22}}\right)^2 + (n_{22} - n_{11}) \cdot \left(\frac{y_{21}}{y_{11}}\right) - n_{21} = 0\,. \tag{5.33}$$

Here, again: The solutions for the quadratic equations are the same and for typical reflectometer c > d holds. Similar relations result from this:

$$\frac{y_{11}}{y_{12}} = c = \frac{(e_{23}e_{32})}{e_{22}} - e_{33}, \tag{5.34}$$

$$\frac{y_{21}}{y_{22}} = \underline{\underline{d = -e_{33}}}\,, \qquad \text{and} \tag{5.35}$$

$$\frac{(e_{23}e_{32})}{e_{22}} = c - d\,. \tag{5.36}$$

In the next step, the reflection standard Γ on port 1 and port 2 respectively is used for computing of e_{11} and e_{22}

$$\Gamma_{mx} = e_{00} + \frac{(e_{10}e_{01}) \cdot \Gamma_{\text{standard}}}{1\text{-}e_{11} \cdot \Gamma_{\text{standard}}}, \qquad \text{hence} \tag{5.37}$$

$$\Gamma_{\text{standard}} = \frac{1}{e_{11}} \cdot \frac{b - \Gamma_{mx}}{a - \Gamma_{mx}}\,. \tag{5.38}$$

Similarly

$$\Gamma_{my} = e_{33} + \frac{(e_{23}e_{32}) \cdot \Gamma_{\text{standard}}}{1\text{-}e_{22} \cdot \Gamma_{\text{standard}}}, \qquad \text{and} \tag{5.39}$$

$$\Gamma_{\text{standard}} = \frac{1}{e_{22}} \cdot \frac{d - \Gamma_{my}}{c - \Gamma_{my}}\,. \tag{5.40}$$

This leads to

$$\frac{1}{e_{22}} = \frac{1}{e_{11}} \cdot \left(\frac{b - \Gamma_{mx}}{a - \Gamma_{mx}}\right) \cdot \left(\frac{c + \Gamma_{my}}{d + \Gamma_{my}}\right). \tag{5.41}$$

Note that during the thru connection e_{22} is measured!

$$\Gamma_{ml} = e_{00} + \frac{(e_{10}e_{01}) \cdot e_{22}}{1\text{-}e_{11} \cdot e_{22}}, \qquad \text{consequently} \tag{5.42}$$

$$e_{11} = \frac{1}{e_{22}} \cdot \frac{b - \Gamma_{ml}}{a - \Gamma_{ml}}\,. \tag{5.43}$$

Using e_{22} from Eq. (A.4.42) gives

$$\underline{\underline{e_{11} = \sqrt{\left(\frac{b - \Gamma_{mx}}{a - \Gamma_{mx}}\right) \cdot \left(\frac{c + \Gamma_{my}}{d + \Gamma_{my}}\right) \cdot \left(\frac{b - \Gamma_{ml}}{a - \Gamma_{ml}}\right)}}}\,. \tag{5.44}$$

Here, it is clear that the sign of e_{11} depends on the high reflection standard. In case of an open standard it is expected that the extracted $\mathrm{Im}\{e_{11}\}<0$ if not, then e_{11} is computed using $e_{11}=|e_{11}|\cdot e^{\arg(e_{11})+\pi}$ (a phase of 180° is added to the extracted phase of the e_{11} at the correspondent frequency step).

Next e_{22} can be computed using

$$\underline{\underline{e_{22}=\frac{1}{e_{11}}\cdot\left(\frac{b-\Gamma_{ml}}{a-\Gamma_{ml}}\right)}}. \tag{5.45}$$

The missing coefficients are obtained by

$$e_{10}e_{01}=e_{11}\cdot(b-a) \qquad \text{and} \tag{5.46}$$

$$e_{23}e_{32}=e_{22}\cdot(c-d). \tag{5.47}$$

Let us assume that the network is reciprocal. Then the error matrix becomes

$$E=\begin{pmatrix} e_{00} & e_{10}e_{01} \\ 1 & e_{11} \end{pmatrix}. \tag{5.48}$$

Using the relation

$$\Delta e-e_{00}e_{11}=e_{10}e_{01}. \tag{5.49}$$

Thus,

$$|e_{10}|=|\ \sqrt{(\Delta e-e_{00}e_{11})}\ |, \tag{5.50}$$

$$e_{10}^2=(\Delta e-e_{00}e_{11}). \tag{5.51}$$

The phase of e_{10} is obtained by

$$\arg\{e_{10}\}=\frac{\arg(\Delta e-e_{00}e_{11})}{2} \tag{5.52}$$

The matrix can then be written as

$$E=\begin{pmatrix} e_{00} & e_{01} \\ e_{10} & e_{11} \end{pmatrix} \tag{5.53}$$

The same procedure can be used for the computation of e_{32}.

A.6 Crosstalk in Backplane Connector Footprint

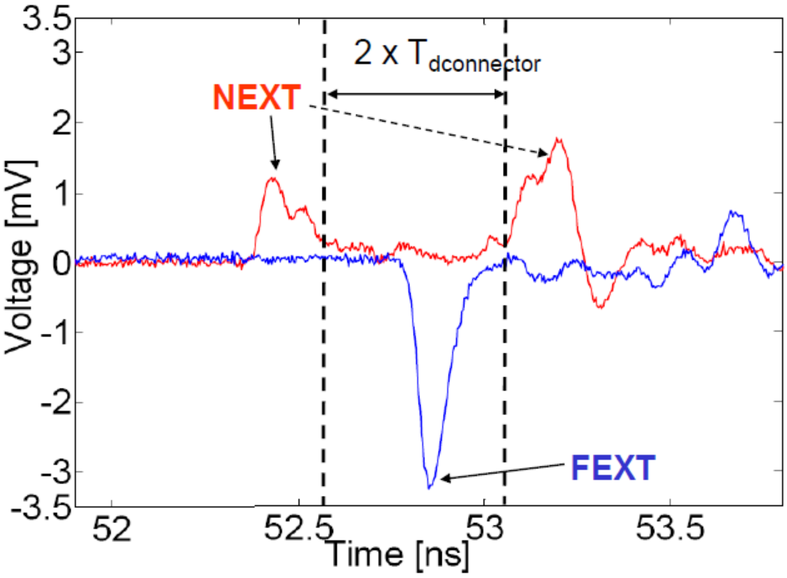


Figure A.6.15 Time domain plot of the near-end and far-end crosstalk behavior in the connector footprint. Obviously, the crosstalk is induced in the connector footprints: two peaks separated by the double delay time of the connector. The FEXT is mainly inductive [11].

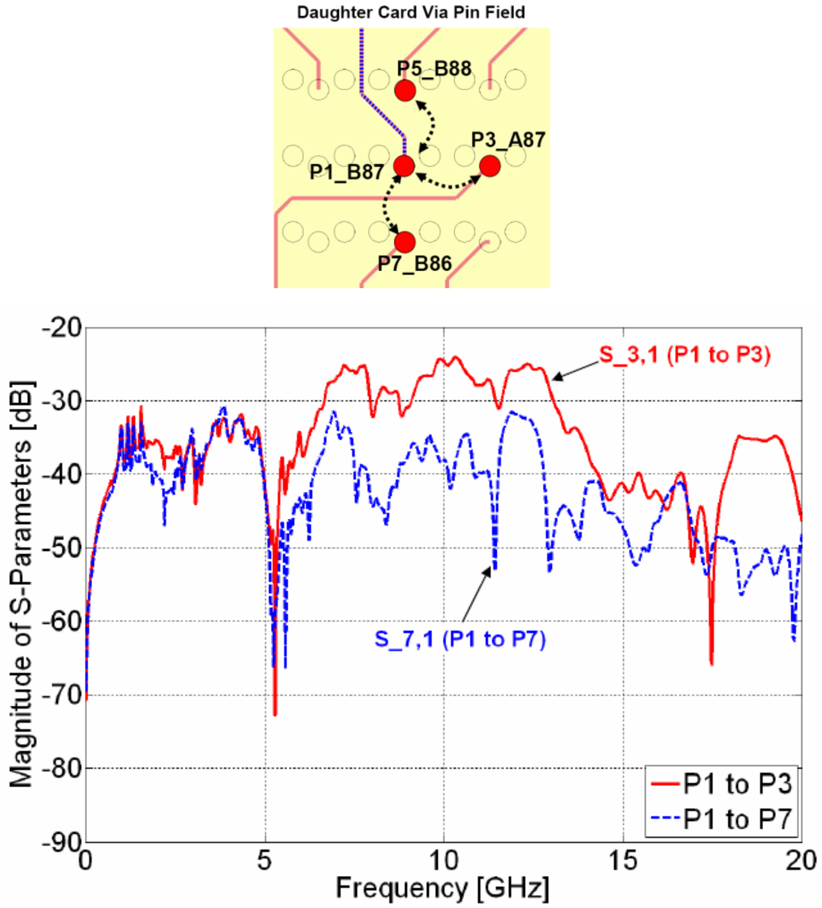


Figure A.6.16 Daughter card near-end crosstalk depending on the orientation to the aggressor via [11].

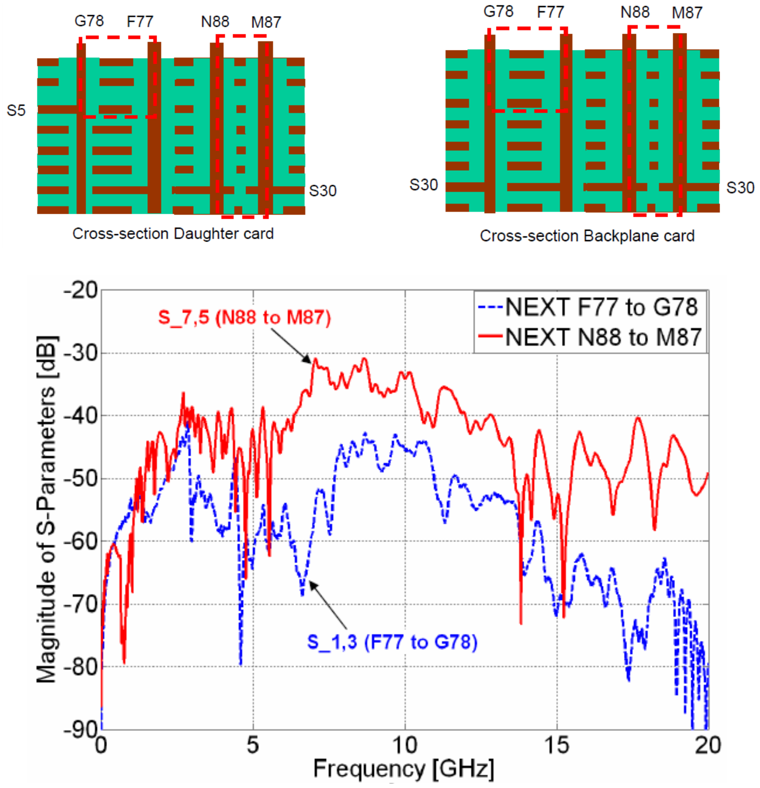


Figure A.6.17 Daughter card near-end crosstalk dependency on the common coupled via length [11].

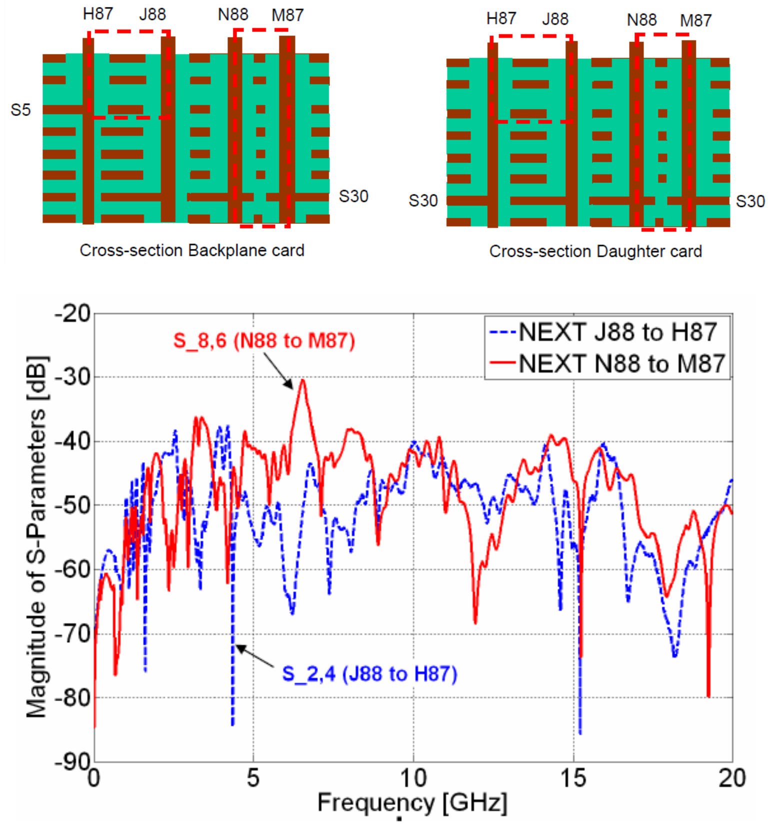


Figure A.6.18 Backplane card near-end crosstalk dependency on the common coupled via length [11].

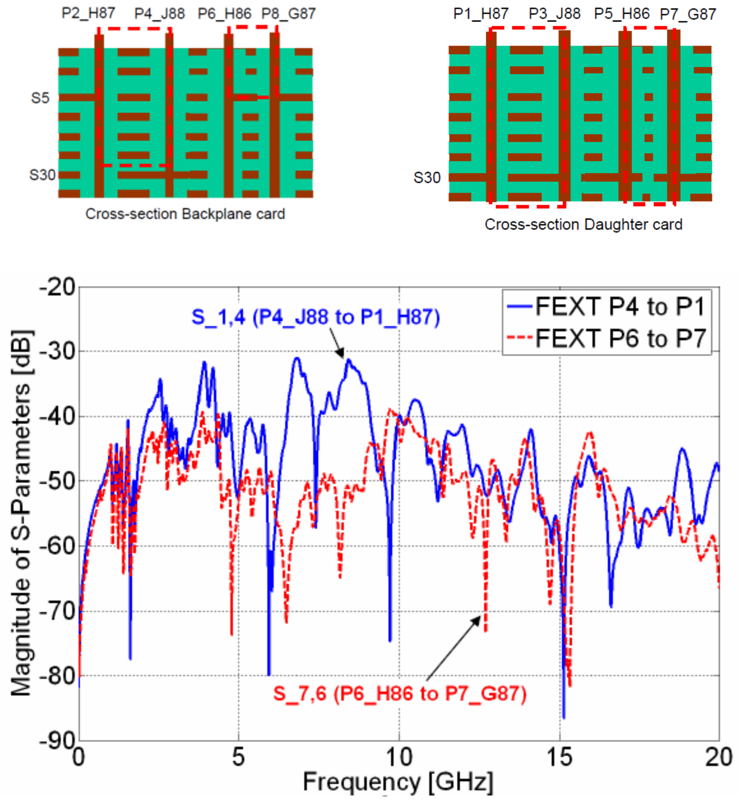


Figure A.6.19 Far-end crosstalk induced by a shorter stub via compared to far-end crosstalk induced by longer stub via [11].

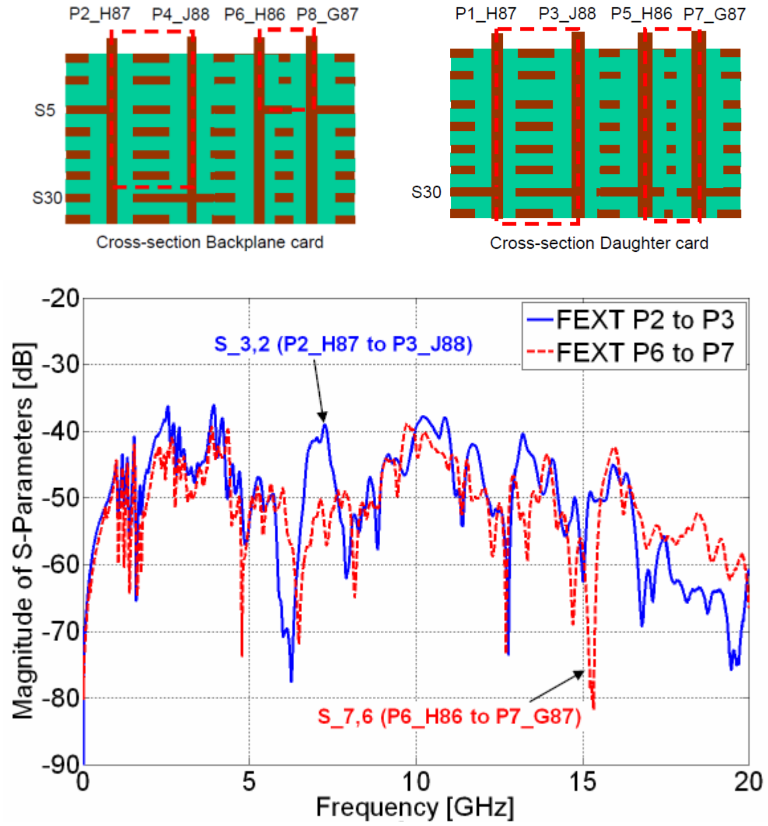


Figure A.6.20 Far-end crosstalk induced by a longer stub via compared to far-end crosstalk induced by another longer stub via [11].

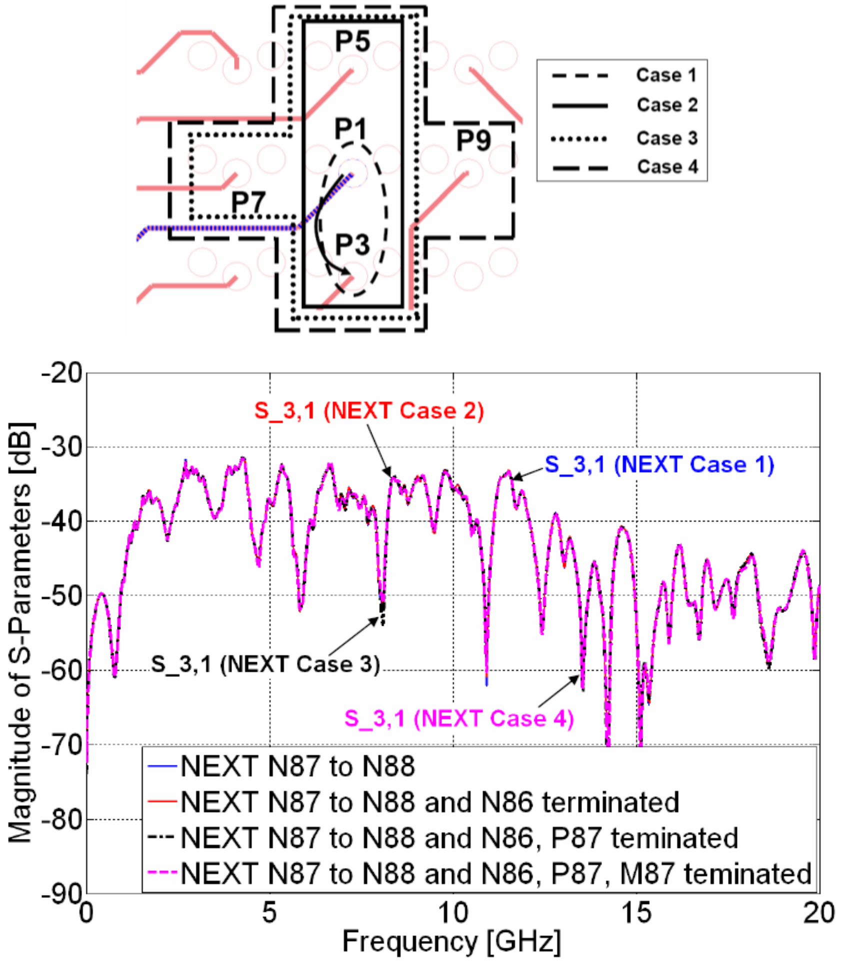


Figure A.6.21 Daughter card near-end crosstalk dependency on the termination of the adjacent vias (no dependency observable) [11].

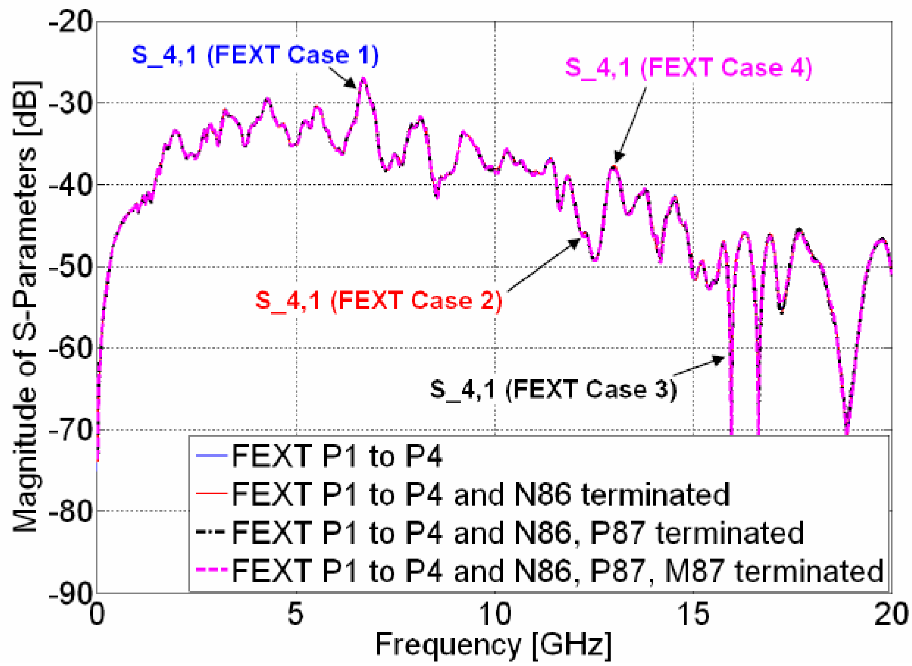


Figure A.6.22 Far-end crosstalk dependency on the termination of the adjacent vias (no dependency observable) [11].

A.7 Microprobe Based Measurements

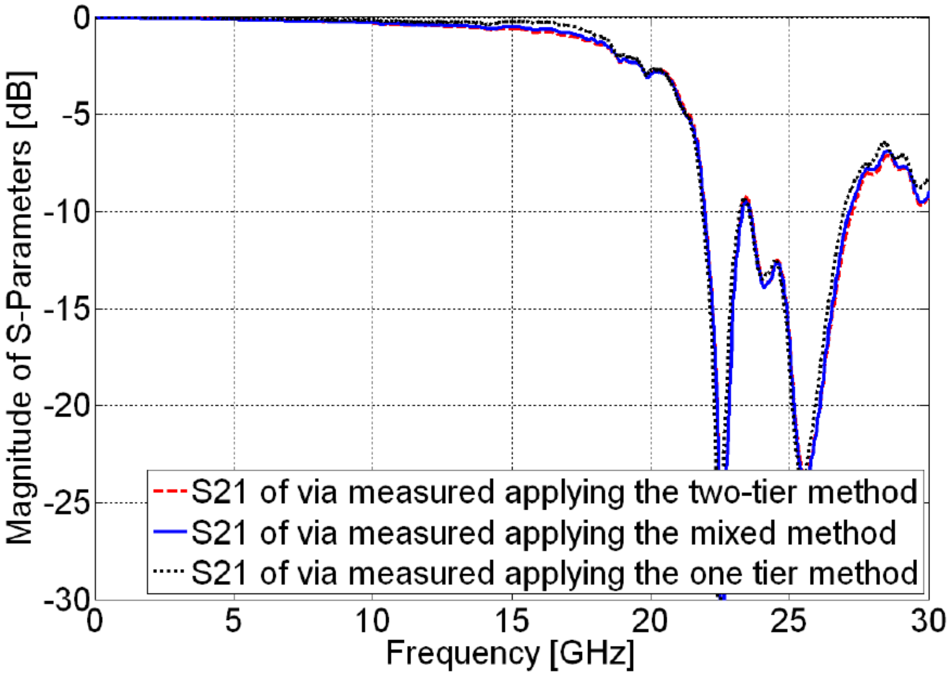


Figure A.7.23 Comparison of the measured transmission through one via in the via array obtained by applying the different methods: one tier SOLT, two-tier and mixed methods.

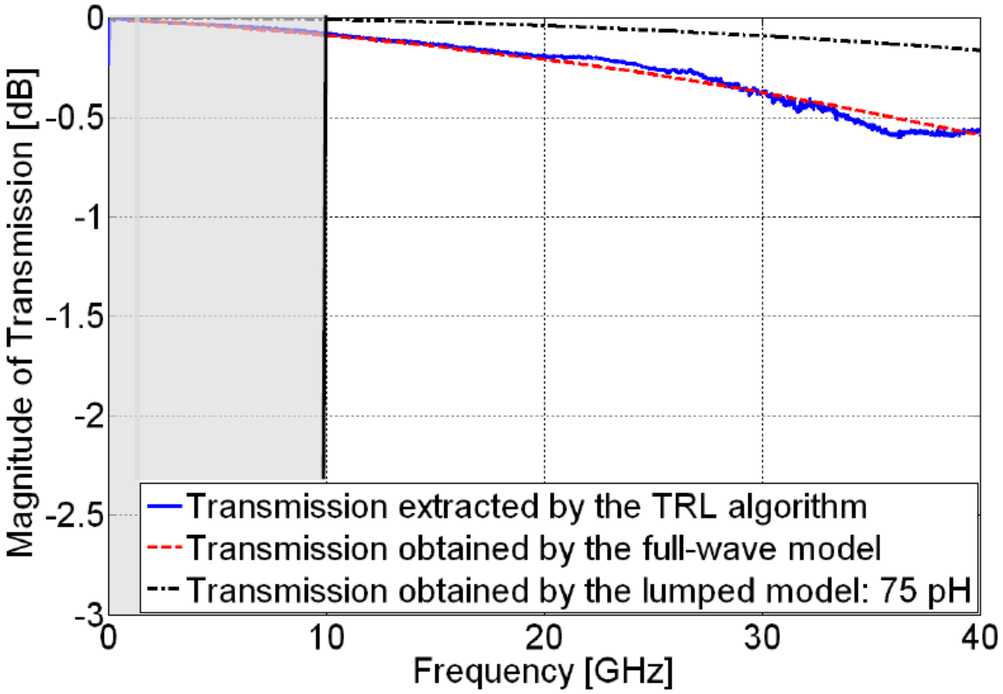


Figure A.7.24 The extracted transmission parameters of the measured RPL correlate well in the frequency range between 10 GHz and 40 GHz. In the band below 10 GHz the TRL algorithm is not reliable [14].

A.8 Interposer Based Measurements

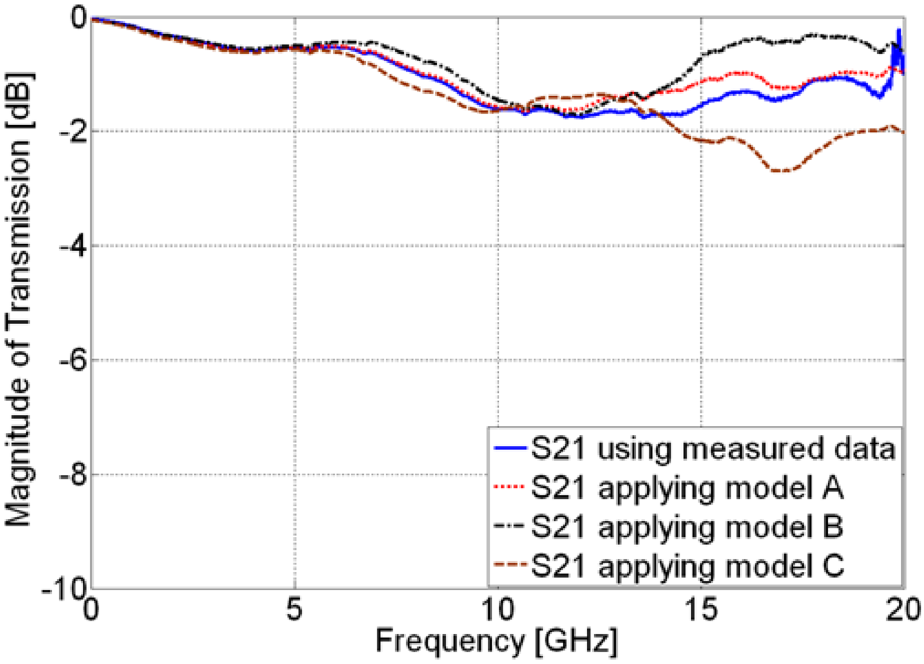


Figure A.8.25 Comparison of the transmission parameters in via 5 obtained after calibration with the measured "expected" S-parameters and the generated S-parameters from the lumped models A, B and C. The best correlation is obtained for model A.

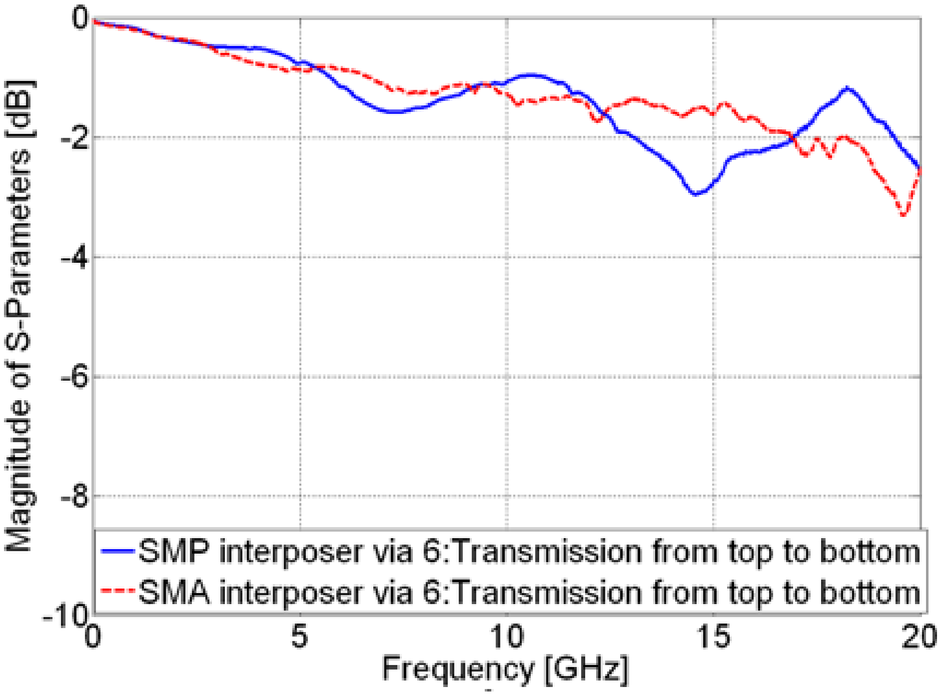


Figure A.8.26 Comparison of the transmission parameters in via 6 extracted by the two-tier calibration procedure. In general, the SMA interposer induces less insertion loss [13].

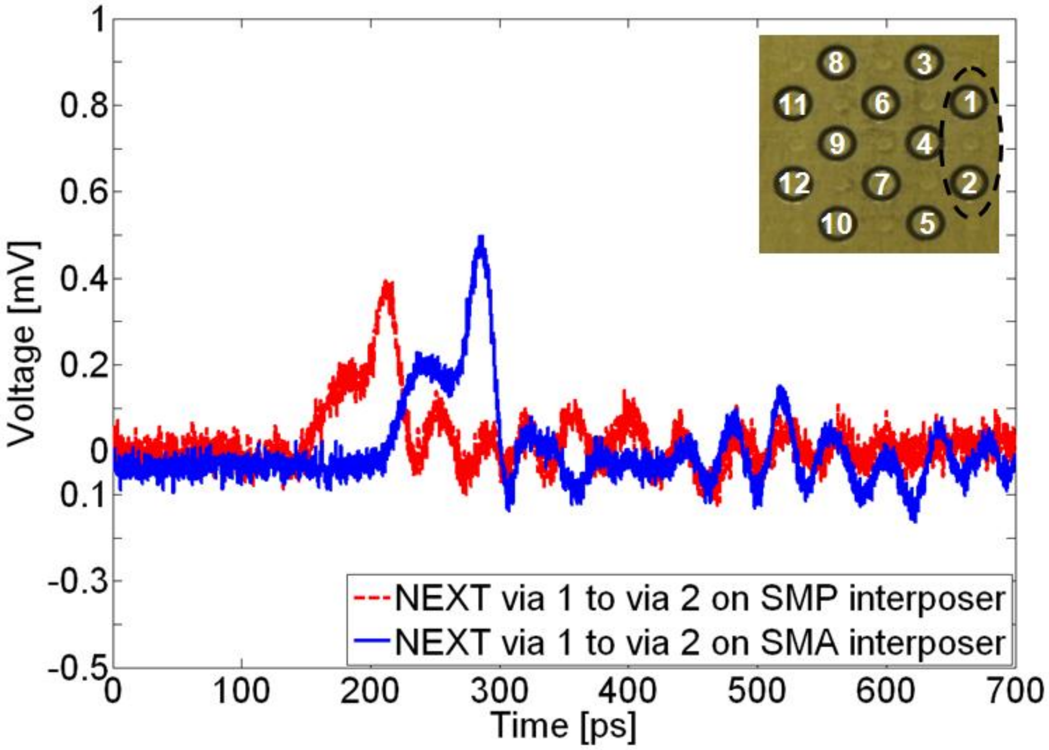


Figure A.8.27 Time domain near-end crosstalk due to rising edge between via 1 and via 2 of access vias isolated with one ground via in-between obtained by digital sampling oscilloscope with "load" terminated interposers [13].

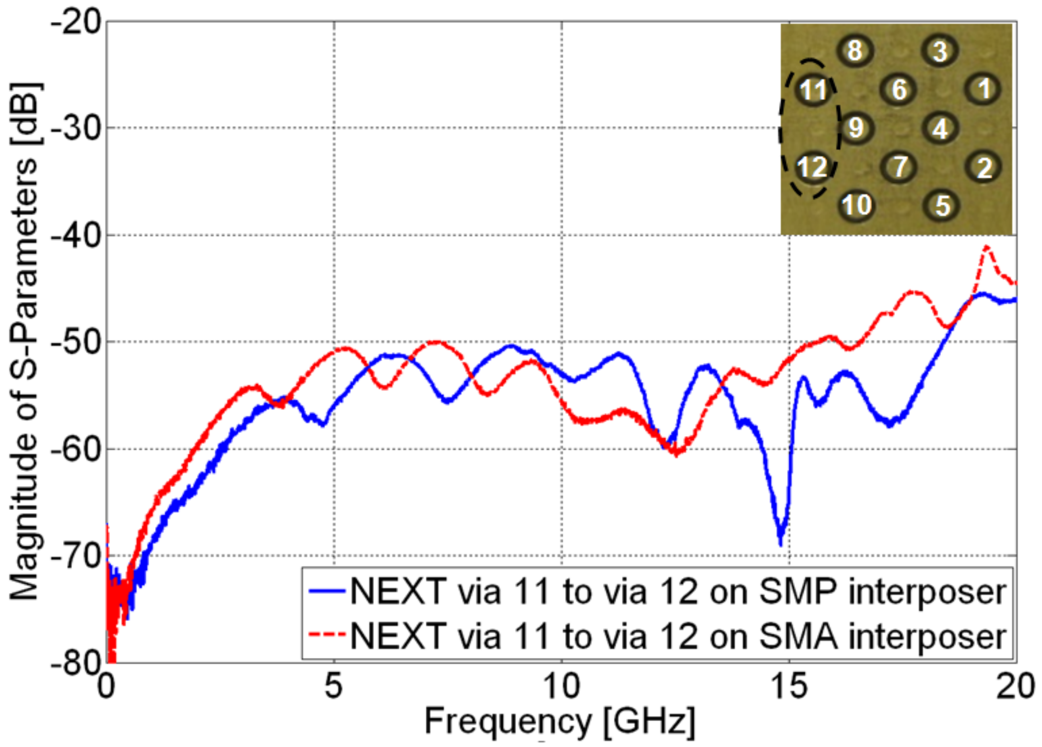


Figure A.8.28 NEXT of via 11 to via 12 with intervening ground via in the via arrays of the middle via array SMP and SMA interposers. In both cases the crosstalk is below-40 dB [13].

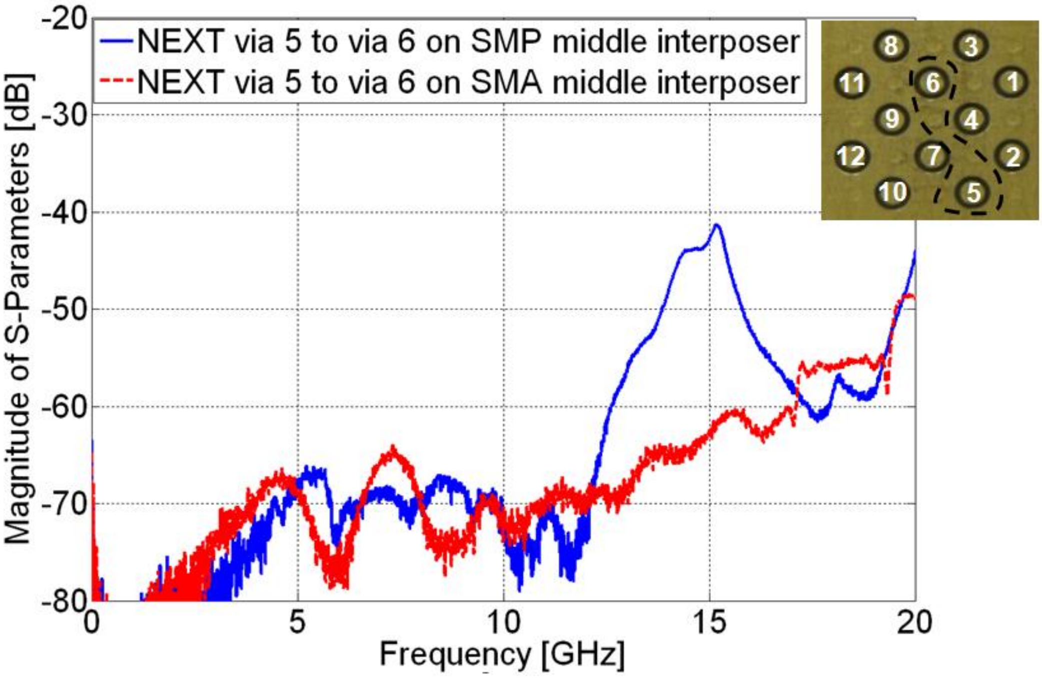


Figure A.8.29 NEXT of via 5 to via 6 in case of the SMP and SMA middle via array interposers. In general the crosstalk is in the range of -50 dB where in case of the SMP interposer it increases to approximately -40 dB at 15 GHz [13].

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