Development of a highly integrated and radiation-tolerant software-defined radio platform for multi-band radio applications in space systems

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Abstract

Software-defined radios (SDR) for space systems have become of great interest in the past decades due to their flexible reconfiguration capabilities on digital processing. Due to the rapid development of new technologies according to Moor's-law, cognitive radio systems have become much more powerful and even capable of realizing multi-band operation purposes with specific radio frequency integrated circuit (RFIC) devices which have been mainly developed for mobile services such as 4G or beyond. Using these technologies in space application would be of great benefit since radio systems are then much smaller and more feasible for operating multiple applications in different frequency bands by simple software-related reconfiguration. Obviously, such technologies are not designed for the harsh environment in space, specifically for radiation.

The presented thesis describes the development of a highly integrated, radiation-tolerant SDR system for multi-band radio applications in space systems. Due to the required state-of-the-art technologies, the avoidance of commercial of-the-shelf (COTS) electronic devices is not feasible but on the other hand probably not mandatory. To ensure a reliable system that is capable of withstanding the constant radiation that will be present in space and the resulting effects on a system, a design methodology is investigated that will guide the development process specifically by means of a selection of electronic devices and their desired qualification level. In terms of new technologies that are mandatory for achieving the multi-band purposes on a highly integrated design, some of these have not been constructed with a radiation environment in mind and should therefore be selected carefully. If radiation test data are available they need to be verified and if no data are available, radiation tests are required. Specifically, the RFIC devices are of great importance for the proposed SDR design and needed to be investigated in detail to ascertain whether their use could be allowed. Such results and specifically the test methodology of such complex and integrated devices are presented as a central part of this thesis.

Even if critical system components have already been independently investigated and described by a third party (e.g. researchers, institutes or manufacturers) in terms of their behavior under radiation, a characterization at the system level is crucial, on one hand to verify the radiation tolerance of the whole system, and on the other hand to

assess the strategic mechanisms for protection from radiation effects, autonomous from radiation-based results on component level, that the system should respond to. Results from these system tests, as well as their preparation and execution, form the concluding part of this present work.

Kurzfassung

Softwareseitig beschreibbare Radiosysteme, sogenannten Software-defined radios (SDR), in Raumfahrtsystemen sind in den letzten Jahrzehnten aufgrund ihrer flexiblen Konfigurationseigenschaften für die digitale Verarbeitung von großem Interesse geworden und haben zunehmend an Bedeutung gewonnen. Die rasante Entwicklung neuer Technologien hat flexible Funksysteme deutlich leistungsfähiger gemacht. Sie sind nach neuestem Stand in der Lage, Mehrbandbetriebszwecke durch integrierte Hochfrequenzschaltung (RFIC) zu realisieren. Diese sind überwiegend für mobile Dienste wie 4G bzw. 5G oder militärische Radarapplikationen entwickelt worden. Die Verwendung solcher Technologien für Weltraumanwendungen hat diverse Vorteile: Funksysteme werde deutlich kleiner und darüber hinaus können mehrere Anwendungen durch einfache Neukonfigurierung in unterschiedlichen Frequenzbändern in einem einzelnen System betrieben werden. Selbstredend sind diese Technologien nicht für die extremen Umweltbedingungen im Weltraum ausgelegt, insbesondere für die hohe Strahlungsbelastung.

Die vorliegende Dissertation beschreibt den Entwurf eines hoch integrierten, strahlungstoleranten SDR für die Nutzung von Mehrkanalfunkanwendungen in Raumfahrsystemen. Aufgrund der notwendigen neuen Technologien, unter anderem des RFIC, ist die Nutzung von rein kommerzieller Elektronik nicht vermeidbar. Anders gesagt: Es stellt sich die Frage, ob und in welchem Maße eine Verwendung von kommerzieller Elektronik, auch bezeichnet als commercial off-the-shelf (COTS), zulässig ist und welchen Einfluss diese auf die Zuverlässigkeit des Gesamtsystems hat. Um dieser Frage nachzugehen, wurde im Rahmen dieser Dissertation eine neuartige Bewertungsmethodik entworfen, um COTS-Komponenten zu evaluieren. Dabei bezieht sich das Bewertungsverfahren primär auf die Strahlungseinflüsse von Funktionsblöcken des zu entwickelnden SDR-Systems und beschreibt einen einzigartigen Entscheidungsprozess für die Auswahl geeigneter Komponenten. Dabei werden mitunter kritische Systemkomponenten, dessen Verwendung nur durch kommerzielle, nicht raumfahrtqualifizierte Elektronik möglich ist, speziell auf verfügbare Daten zu Strahlungstests und/oder bereits existierender Anwendung in Raumfahrtmissionen analysiert und bewertet. Sofern keine valide Daten verfügbar sind, sind eigene Strahlungstests anzuwenden. Dabei trägt ein wesentlicher

Teil dieser Dissertation zur Charakterisierung des ausgewählten RFIC für das SDR-System bei. Durch den hohe Integrationsgrad und Komplexität des RFICs wurden neue Testmethoden entworfen um eine detaillierte Auswertung des Verhaltens unter Strahlungseinflüssen und die letztendliche Bewertung des Einsatzes im System zu gewährleisten. Die essenziellen Methodikentwürfe, Testprozeduren und Ergebnisse zum ausgewählten RFIC sind in der vorliegenden Arbeit beschrieben.

Selbst wenn kritische Systemkomponenten und ihr Verhaltens unter Strahlung bereits durch Dritte, oder wie in der vorliegenden Arbeit eigenständig untersucht und beschrieben wurden, ist eine Charakterisierung auf Systemebene von entscheidener Bedeutung. Sie ist ausschlaggebend um einerseits die Strahlungstoleranz des Gesamtsystems zu verifizieren, als auch die implementierten strategischen Mechanismen zum Schutz von Strahlungseffekten zu bewerten, welche das System autonom auf strahlungsbasiere Ereignisse reagieren lassen sollen. Die Ausführungen, sowohl zur Vorbereitung als auch zur Durchführung der Systemtests, sowie die Diskussion der Ergebnisse bilden den abschließenden Teil dieser Dissertation.

Contents

List of Abbreviations

ADC analog-to-digital converter

ADS-B automatic dependent surveillance broadcast

AGC automatic gain control

AIS automatic identification system

ASIC application-specific integrated circuit

BBP baseband processor

BJT bipolar junction transistor

BPU baseband processing unit

BRAM block RAM

CCSDS consultative committee for space data systems

CERN European organization for nuclear research

CHARM CERN high energy accelerator mixed-field facility

CME coronal mass ejection

CMOS complementary metal-oxide semiconductor

CN criticality number

COTS commercial of-the-shelf

CPU central processing unit

CPS CERN proton synchrotron

CRAM configuration logic bits

CSPBGA chip-scale package ball grid array

CVS current and voltage sensing

DAC digital-to-analog converter

DAQ data acquisition

DD displacement damage

DDR double data rate

DF destructive failure

DN detection number

DPA destructive physical analysis

DSP digital signal processors

DUT devices under test

EEE electrical, electronic, and electromechanical

ECC error correction codes

ECSS European cooperation for space standardization

ENSM enable state machine

EP enhanced product

ESA European space agency

ESP emission of solar protons

FF flip-flops

FFT fast-fourier transformation

FIB focused ion beam

FLUKA FLUktuierende KAskade

FMECA failure mode, effects and criticality analysis

FPGA field programmable gate arrays

FSBL first-stage boot loader

GaAs gallium arsenide

GaN gallium nitride

GCR galactic cosmic ray

GEO geostationary orbit

GNSS global navigation satellite system

GPP general purpose processors

GPS global positioning system

GSDR generic software-defined radio

HIF heavy-ion facility

HW hardware

IEEE institute of electrical and electronic engineers

IF intermediate frequency

IMD inter-modulation distortion

ISS international space station

ITU international telecommunication union

JPL jet propulsion laboratory

JTAG joint test action group

KVI kernfysisch versneller instituut

LEO low Earth orbit

LET linear energy transfer

LDO low-dropout

LO local oscillator

LOL local-oscillator leakage

LUT look-up tables

LVDS low-voltage differential signaling

MBU multi-bit upset

MIMO multiple input multiple output

MOS metal-oxide semiconductor

MOSFET metal-oxide-semiconductor field-effect transistor

MOQ minimum orders of quantity

MRAM Magnetoresistive random-access memory

NASA national aeronautics and space administration

OBC on-board computer

OCM on-chip memory

OCXO oven controlled crystal oscillator

OS operating system

PEM plastic encapsulated microcircuit

PCB printed circuit board

PL programmable logic

PN probability number

POL point-of-load

PS programmable system

PSU power supply unit

RadHard radiation-hardened

RAM random access memory

RHA Radiation hardness assurance

RF radio frequency

RFIC radio frequency integrated circuit

RSSI received signal strength indicator

SAA south Atlantic anomaly

SBR software-based radio

SC software conditioning

SDR software-defined radio

SDRAM synchronous dynamic random-access memory

SEE single event effect

SEECA single event effect criticality analysis

SEB single event burnout

SEFI single event functional interrupt

SEGR single event gate-rupture

SEL single event latchup

SET single event transient

SEU single event upset

SHE single event hard error

SiC silicon carbide

SN severity number

SPC statistical process control

SPI serial peripheral interface

SoC system-on-chip

SOI silicon-on-insulator

SR software radio

SRAM synchronous random-access memory

SSBL second-stage boot loader

SUT system under test

SW Software

TSMC Taiwan semiconductor manufacturing company

TCXO temperature controlled crystal oscillator

TID total ionizing dose

TTC telemetry, tracking and control

UART universal asynchronous receiver-transmitter

UCL cyclotron resource centre of the catholic university of Louvain

UHF ultra high frequency

USB universal serial bus

UWB ultra wideband

VCXO voltage controlled crystal oscillator

VHF very high frequency

WLAN wireless local area network

Chapter 1

Introduction

This PhD thesis presents the design and development of a highly integrated and radiation-tolerant software-defined radio (SDR) platform for multi-band radio frequency (RF) applications on spacecraft. Even though SDRs are commonly known and used for space flight missions, they are either limited in performance and very expensive due to their use of space-qualified and radiation-hardened (RadHard) components or they are cheap and not strictly reliable since they are made of commercial of-the-shelf (COTS) devices without assurance of survivability under radiation conditions that are ever-presented and dominating in space. The SDR platform approach presented here outlines a novel device selection process to ensure a reliable use under the extreme environmental conditions in space, including part-level radiation test investigations on complex radio frequency integrated circuit (RFIC) devices that have never been tested before, and finally a full system-level verification under radiation conditions.

1.1 Motivation

Using new technologies that are generally made for non-space applications can also be highly beneficial for systems in space. In the manner of radio systems, new RFIC devices were released initially for mobile services allowing fast reconfigurations in many functions, from sampling rates up to the selection of different frequency bands. Looking back to classic commercial radio systems in space mission, these were usually developed for a single purpose and as a result a specific hardware was designed, manufactured and finally integrated into the spacecraft. Later modifications were then only possible if the radio systems integrated a digital signal processing unit that allows programmable reconfiguration such as is known for SDR systems. Using such new RFIC technologies would allow the operations of multiple applications on a single radio platform and could massively reduce the spacecraft size, integration handling and finally the overall costs.

Nevertheless, one has to ensure that those devices that are obviously not designed for space applications will reliably work under the harsh environmental conditions in space, especially with respect to radiation. It is not specifically said that COTS devices will immediately fail under radiation conditions, but one has to carefully consider risk assessment and the expected environmental situation. This point of view is applicable for any kind of functionality and is not limited to the desired used of the game-changing RFIC technology. Thus, it is essential from the system-level viewpoint to develop a strategy on how to use COTS devices in a system, since such guidelines are not available and could narrow the gap between expectation and performance, as mentioned above.

1.2 State-of-the-art and problem definition

Radio systems in space missions are usually designed according to specific requirements, independently if they are used for satellite communication or as Earth's observation payloads as part of a science mission. Mostly, quality assurance requires the use of space-qualified devices to improve system reliability, especially if the radio system is used as a spacecraft essential unit, e.g. the communication subsystem. Thus, the use of COTS parts in commercial space missions is often avoided or even prohibited and can lead to prohibitively high mission costs and a huge technology and performance gap between ground-related and space flight state-of-the-art radio systems.

Over the past decades, more and more universities have been pushing forward into the space market by developing tiny satellites also known as *CubeSats*. Such satellites and their contributory subsystems are mainly financially driven with a low-cost and high risk acceptance approach. Using this resulting COTS-devices-only design approach on the other hand allows systems to be generally more efficient and powerful compared to commercial spacecraft systems. However, the rates for potential loss of missions and failure tolerance are very high and statistics have shown that less then 20 % of those CubeSat missions have been completely successful [1]. One reason is that devices were not carefully chosen and quality assurance and testing were not applied. In fact, not all mission failures are related to malfunctions in COTS devices but ultimately it is difficult to determine specific hardware failures on device-level once it is in space.

The use of COTS devices in space missions has always been a sensitive topic till now and has resulted in the above-mentioned classification of space missions: (1) classic commercial space mission with high requirements on reliability and low risk acceptance, and (2) low-budget driven CubeSat mission with high risk acceptance and failure tolerances (discussed in more detail in chapter 3). Nevertheless, COTS devices have become more and more important and also of interest for commercial space flight industries, such as

SpaceX that is planning to launch satellite constellation with tens of thousand of satellites into orbit for commercial services like a high-speed global internet [2]. Indeed, the use of COTS parts is in this example absolutely mandatory since space-qualified devices are far too expensive to be profitable and are not available in such high quantities and short lead-times. This race to space or commercialization of the space sector (also announced as *NewSpace* era) redefines the classic commercial space category [3, 4]. Even if the space industry is now moving towards the use of COTS electronics in their space missions, commercial operators will still keep their selection methodology a secret. It is therefore up to each system designers and quality assurance engineers to decide for themselves which level of quality for electrical, electronic, and electromechanical (EEE) components should be used and currently there is no published guidance approach that supports the decision of selecting between space-qualified or COTS devices.

Radiation testing at certain point will be unavoidable, especially if new technologies are required to be used that are not available RadHard and which have not been previously investigated. Radiation test procedures that are available were typically developed for the qualification on non-complex EEE parts. With decreased featuring-sizes and increased complexity of single devices (e.g. field programmable gate arrays (FPGA) or RFIC), radiation testing becomes more and more challenging and test methods need to be developed for individual hardware components. Another point that has not been covered in the past is full system-level radiation testing but could be a mandatory step in the system verification process, especially if COTS devices are used and radiation effects mitigation strategies are applied and need to be verified.

1.3 Objectives and thesis structure

The primary objective of this PhD thesis is the design and verification of a highly integrated and radiation-tolerant SDR platform for multi-band RF operations. In order to understand the basic mechanism of radiation effects in electronic systems and devices, the fundamentals are therefore presented in chapter 2. Chapter 3 introduces the principles and ideas of SDRs and describes the state-of-the-art of reconfigurable radios for space flight missions with their limitations and disadvantages as already mentioned in section 1.2. The desired and to be developed SDR platform should provide a good trade-off between radiation tolerance, reliability, costs and performance. To realize the intended integrated solution for multi-band RF purposes, key technologies are required to be used as COTS parts since no space-qualified alternatives are available. These circumstances, and in particular the trade-off between costs and reliability, necessitate a valid selection methodology for COTS devices to decide whether the desired COTS electronic parts are acceptable to be used, if additional characterization (up-screening) is mandatory or if space-qualified devices are to be recommended once they are available.

This novel design approach is presented in chapter 4. Since the essential components of the SDR system are intended to be used as COTS parts, radiation effects on such devices are required to be evaluated prior to their acceptance for use. Radiation effects on system-critical COTS devices are presented in chapter 5. Especially the mandatory RFIC technology has been found to be the bottleneck devices in the SDR system design and this has never before been tested under radiation conditions before. A test methodology for this complex and highly integrated device needs to be developed and is presented with the results of certain radiation test campaigns in section 5.2. Finally, the developed and manufactured SDR system, consisting of a hybrid design approach (section 4.2) of COTS devices followed the presented novel design selection procedure (section 4.2.1), and RadHard devices need to be verified on system-level. The final system design and full system-level verification process is described and discussed in chapter 6, including the test methodology to verify the system's robustness and survivability and the overall performance with implemented radiation effects mitigation strategies to enhance system reliability under different radiation conditions. The results of the presented work are finally concluded in chapter 7.

Chapter 2

Basics of radiation effects in space

According to [5], 45 % of spacecraft anomalies are related to radiation effects in space. An earlier study, published in 1994 [6] also linked 9 % to 21 % of spacecraft malfunctions to the radiation environment, whereas 19 % to 53 % of detected anomalies were unexplained and could also be related to the harsh conditions in space. Thus, radiation effects are the major concern in the development process presented in this thesis and the later evaluation under radiation conditions. This chapter therefore gives a brief introduction to the fundamental mechanisms of radiation effects in electronics and their sources in space are presented.

2.1 Space radiation environment

Years before humans sent satellites into space, the evidence of radiation presence had been observed in the aurora borealis by ionization of air or in the deformations of ionized tails from comets by solar winds, even if their sources were not clearly understood at first. In 1958, the presence of high energy particles around Earth was discovered in the so called Van Allen belts, which are further discussed in section 2.1.3 on trapped particles. Since then it has become clear that for missions in space, an extremely disruptive and challenging environment needs to be considered which degrades electronic systems, can damage on-board equipment and generates biological hazards during manned space flight missions. Different types of radiation can occur which are usually absorbed or diminished by the Earth atmosphere and that just could impact on the ground with a negligible flux (except neutrons). These types vary extremely in their energy and nature, their distribution and sometimes their origins. The following sections 2.1.1-2.1.3 discuss the sources of radiation, specifically for near-Earth space radiation environment.

2.1.1 Solar radiation

The Sun is seen as source and modulator of space radiation and the latter's intensity depends on the Sun's activity which has been discovered to be cyclic [7]. This quasi-periodic cycle is approximately 11 years long while the solar maximum usually appears for seven years and the minimum duration is about four years long. Solar particle events are known to be large and the flux of trapped electrons seems to be higher during the declining phase of the solar maximum, while trapped proton fluxes are maximized during the solar minimum [8, 9]. The radiation environment of the solar system is affected by the Sun in three ways:

- **Solar wind**
  The solar wind is a constant flow of low energy electrons, protons and alpha particles. These particles are usually trapped or deflected by the Earth's magnetic field and are mostly not critical for spacecraft electronics compared with other radiation sources. The solar wind also has a modulating effect on the galactic cosmic ray (GCR) which is discussed in more detail in section 2.1.2.

- **Solar flares**
  Solar flares are randomly occurring events that depend on solar activity and are events that lead to magnetic disruption in the solar photosphere. They are lasting for hours and mostly eject high numbers of electrons but also throw out energetic protons, alpha particles and heavy-ions [10].

- **Coronal mass ejection**
  A coronal mass ejection (CME) ejects large amounts of plasma that could last for days and which contains huge quantities of high energy protons and smaller amounts of heavy-ions compared to solar flares [10]. CMEs are responsible for many disturbances in interplanetary space missions and could also affect electronics in near-Earth missions if particles are sufficiently high energetic to pass through the Earth's magnetic field and the spacecraft's structure. Missions with higher inclinations ($\geq 60°$) are usually more affected due to Earth's more attenuated magnetic field at these altitudes (Figure 2.4).

Solar flares and CMEs are solar particle events that can occur simultaneously and which depend on solar activity. The total flux of solar particles thereby can be three times higher in magnitude compared to those which are produced by GCRs as explained by [11].

2.1.2 Galactic cosmic rays

GCRs originate outside of our solar system and consist of extremely highly energetic ionized particles that are probably accelerated by shock waves from supernova explosions propagating through the interstellar medium. GCRs appear in isotropic direction and are randomized over time. Their composition consists of 87 % hydrons (protons), 12 % alpha particles (helium) and 1 % heavier-ions and electrons [12]. The energy varies between 10s MeV up to 10^{11} GeV and travels at a small fraction of the speed of light (50 to 1200 km/s). Figure 2.1 illustrates the behavior of GCR influence on our solar system.

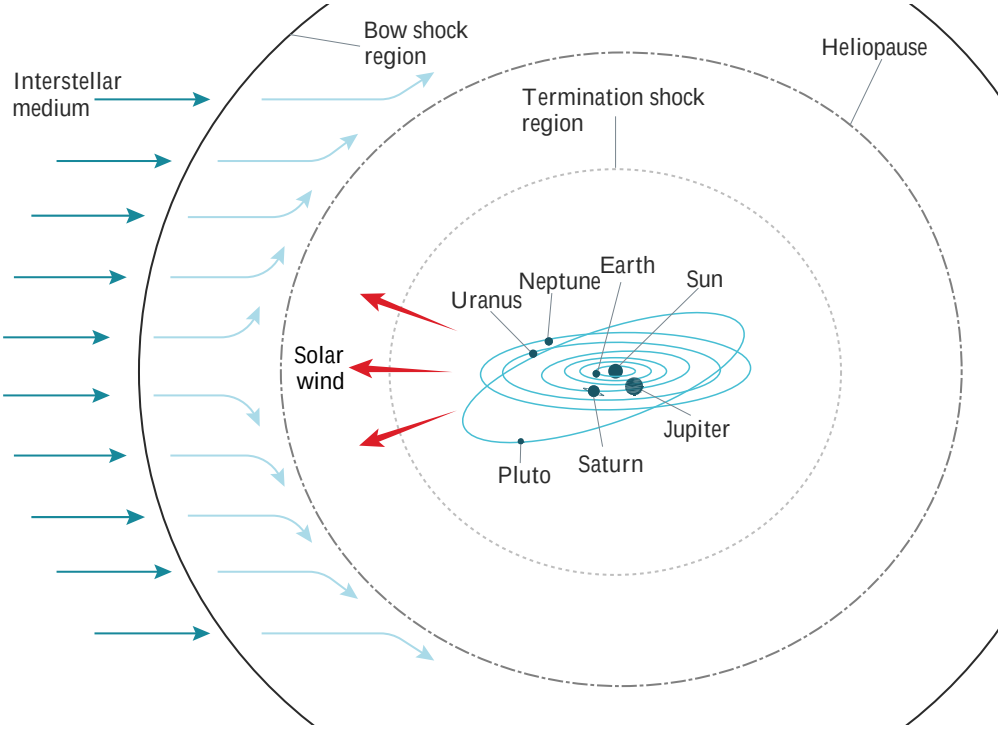


FIGURE 2.1: Illustration of the solar system with the heliosphere, interaction of solar wind and the GCRs, according to [13].

Solar particles are emitted radially from the sun and slow down to subsonic velocity at the *termination shock* region. The *heliopause* is the outer region of the interplanetary magnetic field and protects the solar system against the incident GCR particle flux. At this point, the solar wind and the interstellar medium pressure are in balance. At the *bow shock* region, the interstellar medium's becomes subsonic such as for the termination shock region for the solar wind velocity. Lower energetic particles ($\leq$50 MeV) are not able to enter the heliosphere (the inner part of the heliopause). For higher energetic particles (>1 GeV), the flux decreases with the energy, as set out in [14]. The GCR flux depends on the solar activity and the resulting solar wind. Thus, the maximum GCR flux is achieved during solar minimum and vice versa, as portrayed in Figure 2.3. Only protons and heavy-ions lighter than iron (Fe) are considered in this plot since the relative abundance of ions decreases significantly after iron, as shown in Figure 2.2. The main

direct ionization contribution to GCRs are the following ions of the elements hydrogen (H), helium (He), carbon (C), oxygen (O), neon (Ne), magnesium (Mg), silicon (Si) and iron (Fe) [15].

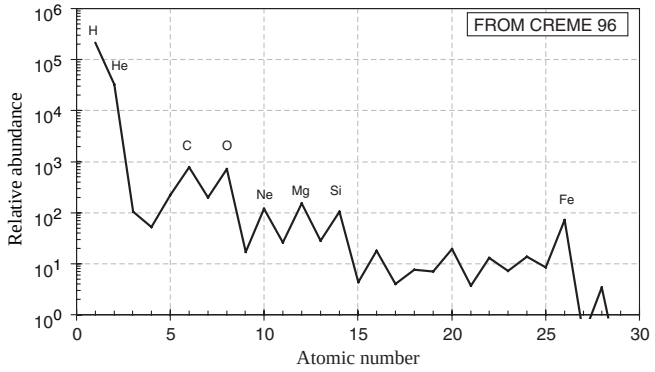


FIGURE 2.2: Abundances of GCR elements from hydrogen (H) to iron (Fe), according to [12].

The integral linear energy transfer (LET) spectra include all elements from protons to heavier-ions and can be converted from the energy spectra as illustrated in Figure 2.3. The LET describes the energy loss in a sensitive volume (e.g. silicon (Si)) of ionized particles per unit path length ($MeV \cdot cm^{-2} \cdot mg^{-1}$) and is important for single event effect (SEE) analysis which is presented in more detail in section 2.2.

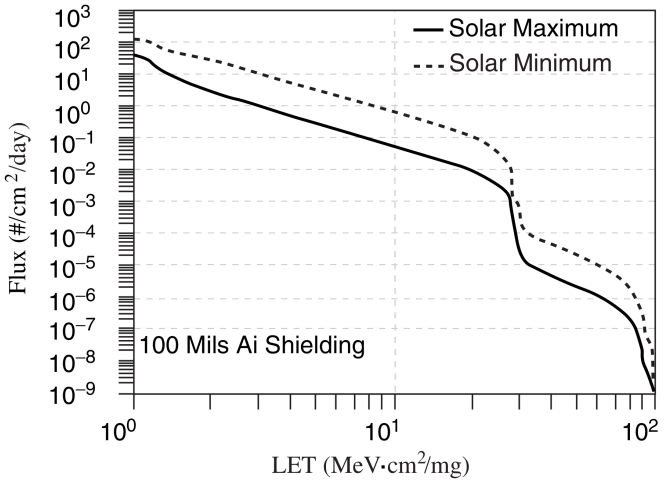


FIGURE 2.3: The integral LET spectra for the GCR during solar minimum and maximum [12].

Highly energetic GCR particles are able to pass the radiation belts and reach the Earth's magnetic field where they could affect the electronics in LEO space missions. However, the flux of these particles remains very low compared to GEO satellite missions where fluxes can reach a few particles per cm^2 per day and are potentially higher at the polar regions or at the south Atlantic anomaly (SAA), see the following section 2.1.3.

2.1.3 Trapped particles

Due to the Earth's magnetic field, solar and GCR particles are trapped and progressively enable the formation of the near-Earth radiation fields, known as *radiation belts*. These radiation belts are formally known as *Van Allen belts*, discovered in 1958. They consist of two regions, the inner and outer belts as presented in Figure 2.4, whereby the inner belt is mainly composed of electrons (up to 5 MeV) and protons (100s of MeV). Electrons ($\leq$7 MeV) dominate the outer belt [6, 16].

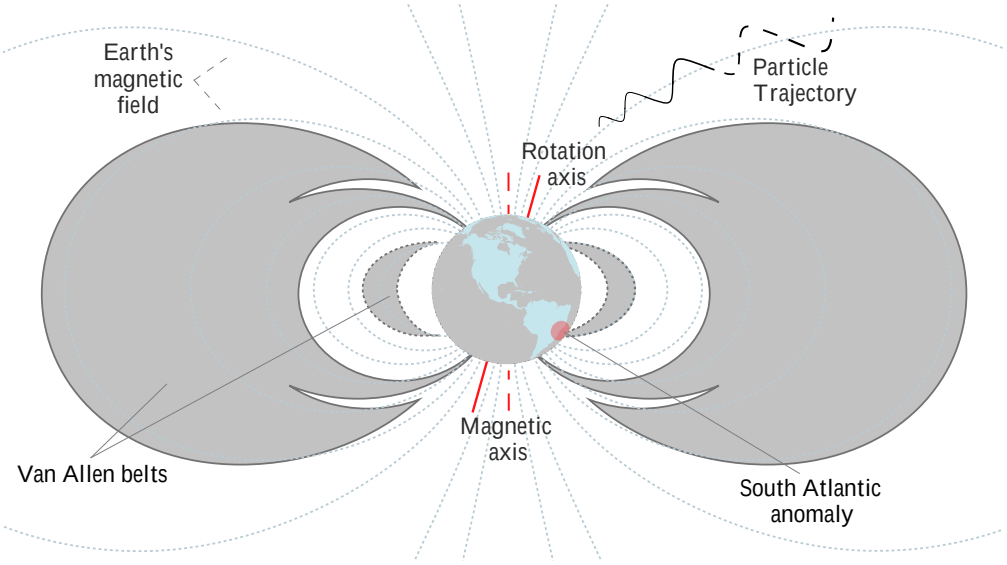
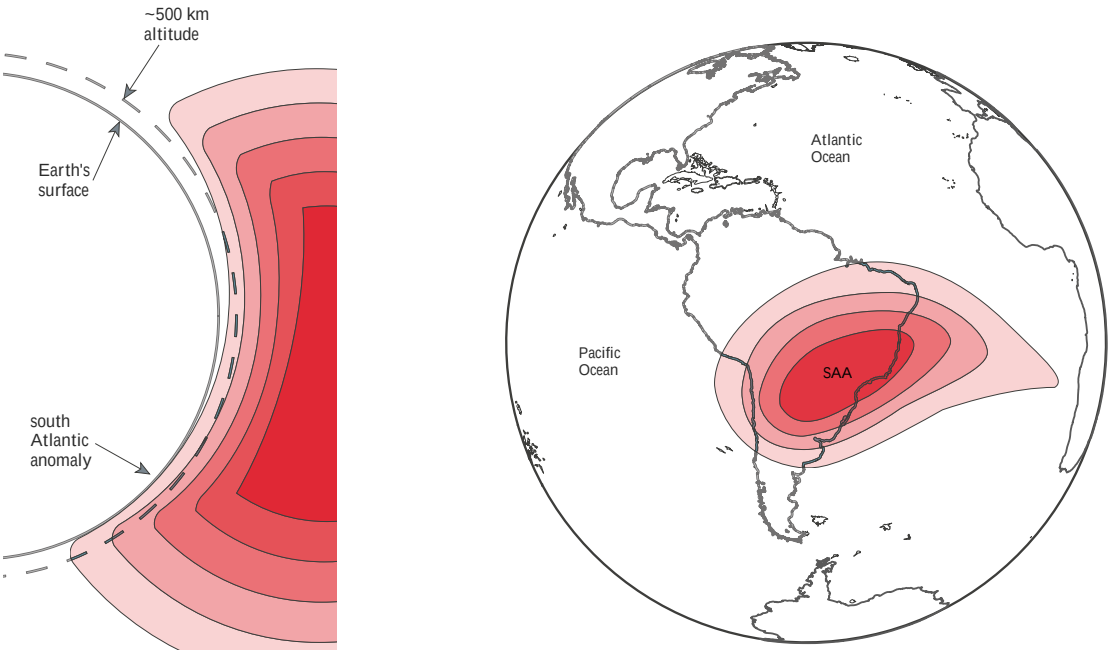


FIGURE 2.4: Illustration of the Earth's magnetic field and the Van Allen radiation belts, according to [13].

The inner belt ranges from 1.200 km to 6.000 km and the outer belt approximately from 13.000 km to 60.000 km above the Earth's surface (as seen from the Earth's equator). The inner Van Allen belt consists of a proton and electron belt, whereas the outer (electron) belt has a high concentration of only electrons. The omnidirectional proton and electron flux in the Van Allen belts is about 10^7 to 10^9 particles per $cm^{-2}{\cdot}day^{-1}$ (depending on the altitude and inclination) with proton energies above 30 MeV and 1 MeV for electrons, respectively [10, 17]. For the outer electron belt, the maximum electron flux occurs with $\approx 10^9$ particles per cm^2 per day above 1 MeV [17].

Because the Earth's magnetic field is tilted about 11° from its rotational axis (bold line in Figure 2.4), the radiation belts do not align symmetrically with the Earth's surfaces. The asymmetric behavior of the Earth's magnetic field results into a localized altitude drop of the inner Van Allen belt (200 km to 800 km instead of 1.200 km) which is called the *south Atlantic anomaly* (SAA). An illustration of the SAA is presented in Figure 2.5 showing a local drop of inner belt over the south Atlantic ocean and South America in a cross-section (a) and global (b) view.



(a) SAA cross-section view

(b) SAA global view

FIGURE 2.5: Illustration of the SAA in (a) cross-section view and (b) global view, according to [13].

The particle flux within the SAA is much lower compared to the center of the radiation belts. However, for low altitudes, the SAA is the only region on Earth where higher proton and electron fluxes can be expected which can be critical for LEO missions. This could be critical also for man-rated missions such as on the international space station (ISS) which frequently/regularly passes over the SAA.

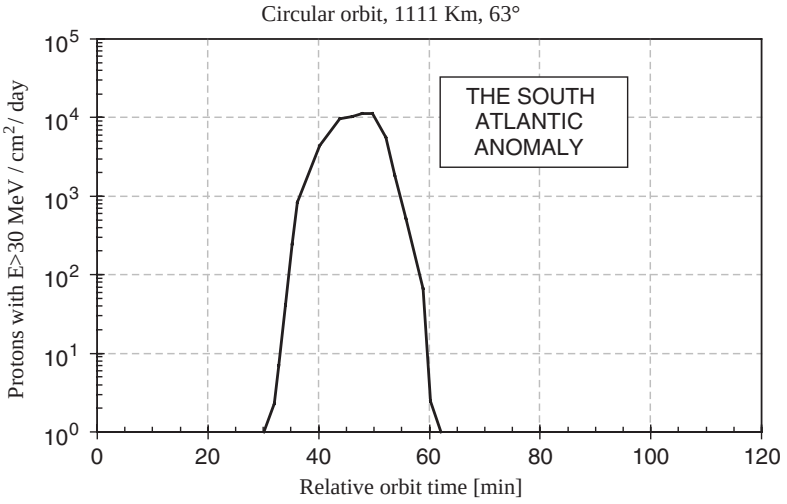


FIGURE 2.6: Trapped proton flux vs. relative orbit time of the circular orbit mission, showing the effect of the SAA [10, 18].

The highest radiation dose the ISS is exposed to occurs when it flies through the SAA. As an example, Figure 2.6 shows the proton flux of a circular orbit (1.111 km altitude

and 63° inclination) over a time span of two hours. A high peak can be observed at 40 to 50 minutes, reaching a fluence of 10^4 particles per cm^2.

2.2 Radiation effects in electronics

Radiation effects in electronics or semiconductors impact in two fundamental ways:

- **Cumulative effects**
  Cumulative effects or dose effects are characterized by drifts in the parametric of the electronics that accumulate over time due to long-term exposure to radiation. Those effects include total ionizing dose (TID) effects presented in section 2.2.2 and displacement damage (DD) discussed in section 2.2.3.

- **Single event effects**
  SEEs are radiation effects in electronics that are caused by the passage of single particles through the semiconductor. SEEs are instantaneous disruptions that occur randomly, leading the electronic devices to fail in a non-destructive or destructive way. Those types of events and their mechanisms are discussed in section 2.2.4.

Figure 2.7 shows a diagram of the radiation environment and its interaction type causing radiation effects. The radiation sources have already been discussed previously in the section 2.1.

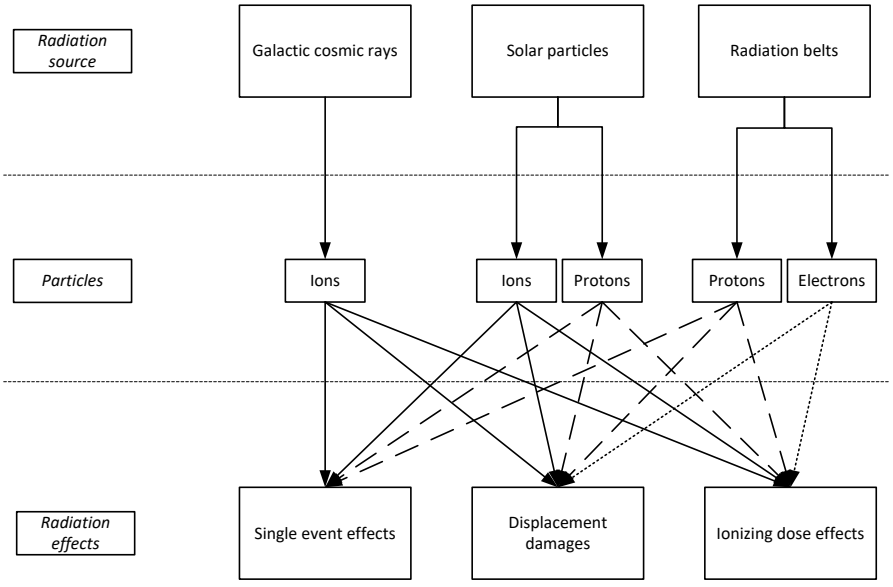


FIGURE 2.7: Radiation sources and types of interaction causing radiation effects in electronics.

Three main types of particles that cause radiation effects are considered: electrons, protons and heavy-ions. Since electrons are mainly responsible for surface charging and usually do not affect the electronics inside a spacecraft, radiation effects from electrons will not be within the scope of this thesis. For radiation effects, interactions with matter represent the fundamental mechanism, and these are outlined in the following section 2.2.1.

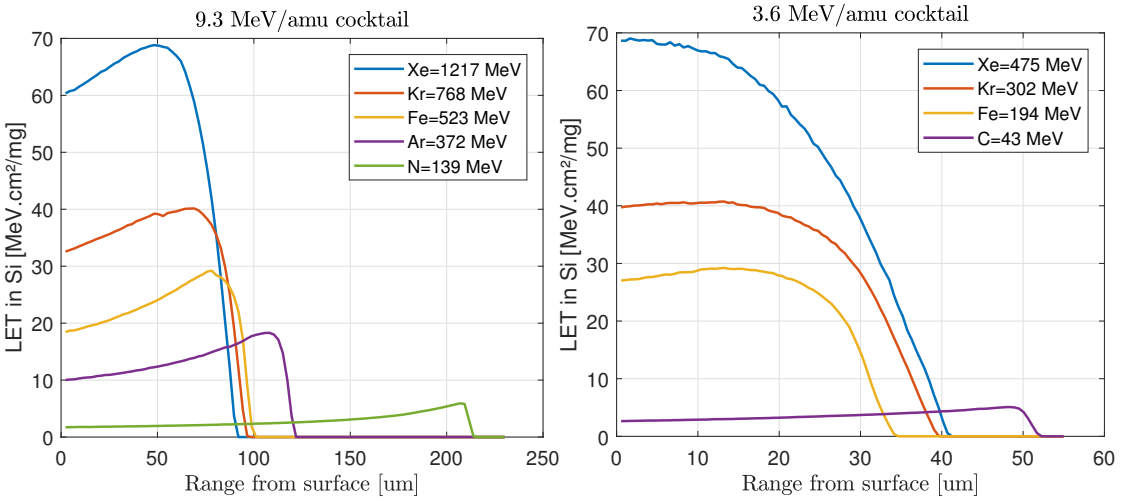
2.2.1 Particle interaction with matter

Incident charged particles such as protons, ions or electrons pass through matter and lose their energy by a succession of different electromagnetic interactions with the electrons around the nuclei or by direct interaction with the atomic nuclei. These interactions depend on the type of particle, its energy and the composition of the matter itself. Particle-matter interactions are categorized into two groups in terms of radiation effects in electronics and are described in the following subsections. For the present work, charged particles such as protons and heavy-ions are of most interest. Thus, the particle interaction with matter focusing on both of these types. However, non-charged particles such as photons (e.g. γ-rays) or neutrons are also capable of causing radiation effects. In probabilistic photon interactions, energy is transferred to electrons of the atomic shells and these release additional energy via a secondary interaction that is mostly an ionization process. The types of interaction of photons with matter take place commonly via photo-electric effects, Compton scattering or pair productions [19]. Neutrons are potentially able to generate SEEs through indirect ionization (section 2.2.1.2). However, neutrons primarily occur in the terrestrial environment, from sea level up to the atmosphere (20 km) and are not common in space applications. For space applications, charged particle interactions with matter are more dominant and of interest. These will now be discussed in more detail.

2.2.1.1 Particle interaction causing direct ionization

Due to its charge, the incident particle (mainly heavy-ion) interacts with the atom. In the course of successive interactions, the charged particle progressively loses its energy via a transfer process to the atoms. The energy state of the atom is thus raised to a higher level and leads to an excitation or ionization of the electrons of the nuclei. An increased number of electrons (and associated positive ions) for electronic materials becomes available for conduction. Direct ionization happens through incident particles in matter creating a high density of electron-hole pairs until the ion has lost all its energy and stops. The energy loss makes two types of contribution: (1) the electronic contribution where the incident particle interacts with the surrounding electrons of the

nuclei via inelastic processes, and (2) nuclear contribution (see section 2.2.1.2) in which the incident particle directly interacts with the nuclei during an elastic or inelastic process. The energy per unit length being transferred to the material is known as the LET whereby the stopping power describes the energy loss per unit length. The LET progressively increases for high-energetic particles reaching a peak of ionization, so-called *Bragg peak*. Beyond this point, the energy loss in electron ionization stops and begins to decrease, as being illustrated in Figure 2.8.



(a) High energy cocktail (b) Low energy cocktail

FIGURE 2.8: LET and range silicon of various ions on high (a) and low (b) energy cocktails (University of Jyväskylä), according to [20].

Direct ionization as discussed previously is usually applicable for heavy charged particles, in particular heavy-ions. For low energy protons, the electronic LET is higher than for high proton energies enabling those particles to produce direct ionization and thus causing SEEs [21]. This phenomenon mainly affects modern, integrated semiconductor technologies ($\leq$65 nm).

2.2.1.2 Nuclear interaction causing indirect ionization

For nuclear interaction, radiation interacts directly with the atomic nuclei. If the incident radiation has sufficient energy to pass the Coulomb barrier, it will overcome the electronic reaction and approach the nucleus close enough to interact directly with the nuclei. Only protons with their unitary charge and sufficiently high energies ($\geq$2.8 MeV, according to [21]) to break the Coulomb barrier can interact with the nucleus and cause a nuclear interaction. The nuclear interaction leads to ion recoils and fragmentation, thus generating one or more secondary ions. The charge, energy and angle of secondary ions depend on the properties of incoming protons. Secondary ions are able to deposit a critical charge (LET) in the sensitive volume causing SEEs. A further effect is DD

when the incident proton has enough energy that it displaces the whole atom from its position in the crystalline lattice structure (see section 2.2.3). The probability of nuclear interactions is much lower than the electromagnetic type of interaction but has a more dramatic impact. As discussed in section 2.2.1.1, heavy-ions mainly interact with matter by direct ionization. Nevertheless, high energy ions are able to pass through the Coulomb barrier and also interact with the nucleus causing DD and creating ion recoils with a high LET [21].

2.2.2 Total ionizing dose

TID refers to the dose that is deposited onto the electronics through ionization effects and which leads to lasting parametric shifts that accumulate over time. The main driver for TID effects is the generation, transport and trapping of holes in the insulation in metal-oxide semiconductor (MOS) and bipolar devices at or close to the silicon-oxide interface. The most common insulator in MOS and bipolar technologies is silicon dioxide (SiO_2), which is also used to form the gates of MOS transistors. For complementary metal-oxide semiconductor (CMOS) devices, a loss of performance or functionality is possible due to isolation leakage if sufficiently high doses have been absorbed. For bipolar devices, TID effects typically lead to a reduction in current gain.

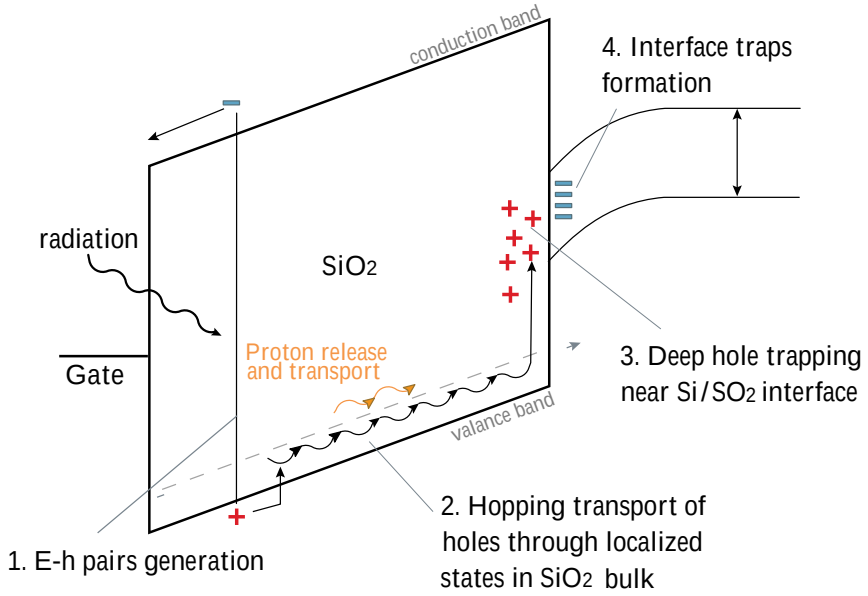


FIGURE 2.9: Band diagram of a MOS device supplied with positive gate voltage illustrating the effect of ionizing radiation on carrier generation, hopping and trapping, according to [22].

Figure 2.9 shows the band diagram (or vertical cut) of the MOS stack used in CMOS and bipolar junction transistor (BJT) devices with the energy shown on the vertical axis and the physical distance on the horizontal axis. It illustrates the mechanism of TID in the transistor's oxide. Incoming radiation ionizes electrons in the valance band and

pushes them up to the conduction band, leaving holes (*1. E-h pair generation*). Since the mobility in oxides for electrons is relatively high with respect to holes, electrons and holes cannot be created equally. Since electrons can be removed easily from the conduction band with the applied positive gate-voltage, leaving the holes in the valance band to move slowly by a hopping mechanism towards the interface (*2. Hopping transport of holes through localized states in the SiO_2 bulk*). When these holes get near the interface, they become trapped in the oxide forming deep hole traps and generating a positive charge close to the silicon (*3. deep hole trapping near the interface*). This positive charge affects the localized field and thus the device characteristics. During the hopping mechanism of the holes, protons are released due to hydrogen that is left in the semiconductor process. The protons get pushed in the same direction as the holes, but move directly to the silicon interfaces, creating defects at the silicon surface which is more problematic for bipolar devices than for newer CMOS technologies (*4. Interface trap formation*).

2.2.3 Displacement damage

Besides TID, DD represents the second type of cumulative radiation effect. Compared to TID, DDs are volumetric effects in that the silicon changes the electrical properties of the bulk accumulates over time. DD primarily occurs due to nuclear interaction when the incident particle imparts its energy fully to the atom (nucleus). As seen in Figure 2.10, if the particle energy supplied to the nucleus can overcome the binding energy in the crystalline lattice structure, it can be displaced from its initial position to various end locations. The dislocation produces a localized vacancy and mobile interstitial defect.

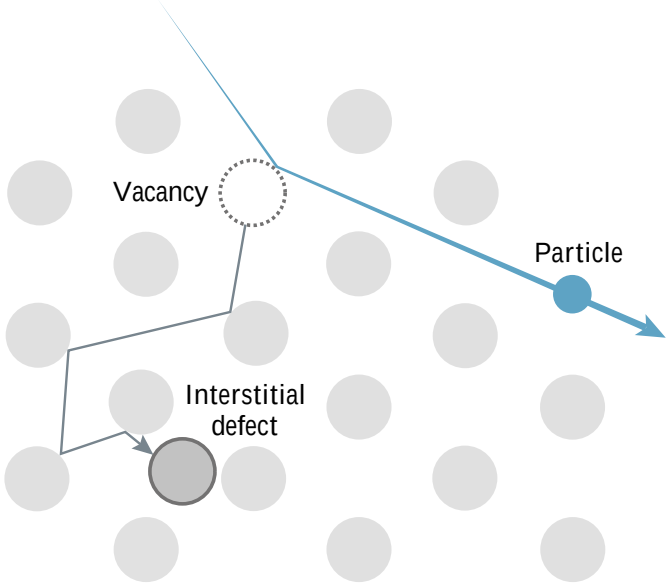
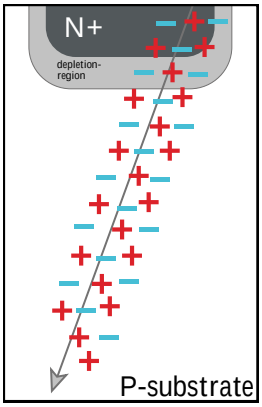


FIGURE 2.10: Illustration of DD in the crystalline lattice structure, according to [13].

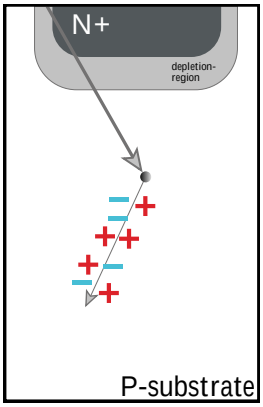
Both defects can create traps in the silicon band gap that cumulatively lead to changes in the device's operation such as increased leakage current or a decrease in overall performance (e.g. gain factor). BJTs are potentially affected by DD and typically show reduction in the current-gain. MOS circuits are quite robust against DD effects. For higher DD doses, metal-oxide-semiconductor field-effect transistor (MOSFET) devices' drive strength and switching speed may be affected [13, 23].

2.2.4 Single event effects

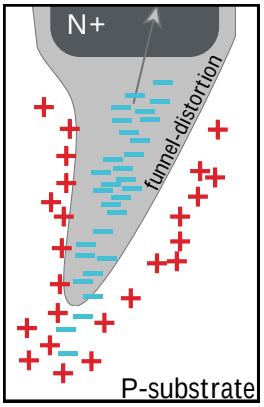
The basic mechanism of an SEE (also termed a single event transient (SET) as an archetype) can be depicted according to Figure 2.11, which shows the charge collection phases on a reversed-bias p/n-junction [13, 24, 25].



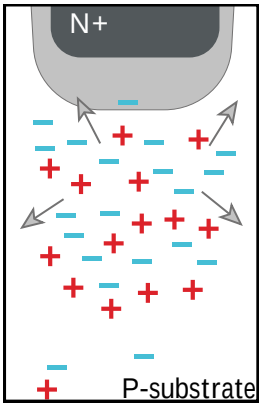
(a) Onset event of an ion particle



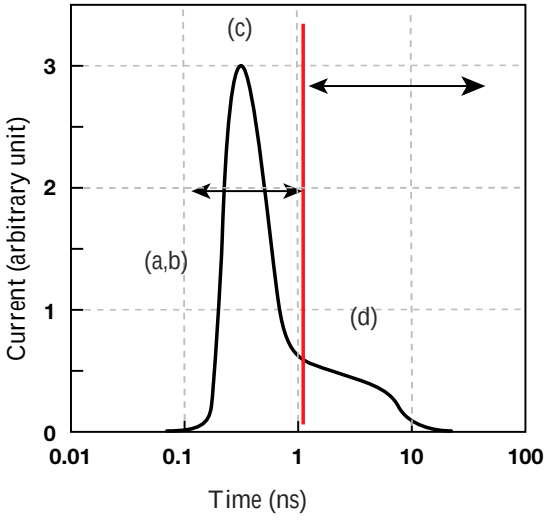
(b) Onset event of a proton particle



(c) Prompt charge collection



(d) Diffusion charge collection



(e) Transient charge vs. time

FIGURE 2.11: Phases of charge collection in a reversed-biased p/n-junction and the resulting current transient caused by the passage of a high energy ion, according to [24–26].

An SEE occurs when an energetic particle (ion, proton) strikes an electronic device down to its semiconductor substrate and traverses through the depletion region. The charged ion leaves a high density of ionized excess electron-hole-pairs (direct ionization) on its track (Figure 2.11 (a)). For protons (Figure 2.11 (b)), SEEs are mainly generated through indirect ionization due to heavy-ion recoils (secondary ions) that are generated by nuclear interaction. The incident particle and the secondary products produce a dense distribution of electron-hole-pairs along its trajectory. Carriers are rapidly collected by the high electric field near the depletion region and compensates for the charge stored in the junction. The charge distribution induces a temporary funnel-shaped potential distortion, leads to a enhanced charge-collection and extends the depletion region deeper into the substrate (Figure 2.11 (c)). This phase is called *prompt-charge-collection* and lasts a few nanoseconds until the funnel collapses and *diffusion-charge-collection* dominates (Figure 2.11 (d)) the charge collection process. The diffusion-charge-collection takes a couple of 10s to 100s of nanoseconds until all excess carrier have been collected, recombined or diffused away from the junction region. The charge collection process follows a transient pulse shape (current at the junction) as illustrated in Figure 2.11 (e). The time and current of this pulse depend on the type and energy of the incident charged particle and its material properties. For most modern microelectronics, in particular digital circuits based on CMOS, the further away from the junction that the event occurs, the smaller the amount of charge collected and the less likely it is that this event will cause an SEE [13].

SEEs come in two categories: *non-destructive* SEEs causing a temporary failure and *destructive* SEEs leading to a permanent damage and persistent loss of the device's functionality. Both SEE categories are presented in more detail in the following sections (2.2.4.1 and 2.2.4.2).

2.2.4.1 Non-destructive SEEs

Non-destructive SEEs occur in different types depending on the device functionality and technology. The common non-destructive SEEs are presented below:

- **SEU**
  A single event upset (SEU) occurs at the sensitive area of a logic cell and can cause a change in its logical state. Memory devices, registers or sequential logic are typically affected by SEUs.
- **MBU**
  Depending on the deposited charge (or energy) and the technology size, multiple logic cells can be upset by a single particle. This type of SEE is called a multi-bit upset (MBU) event and also occurs in memory or logic devices.

- **SEFI**
  A single event functional interrupt (SEFI) refers to the temporary loss of functionality or interruption of the nominal operation. SEFIs typically occur in complex and integrated circuits consisting of state machines or logic controllers. SEFIs are typically able to recover, e.g. by a power-cycle or reset of the device.

- **SET**
  An SET is a transient impulse with a certain period and amplitude that could propagate towards other analog or digital (combinatorial logic) circuits causing further failures. SETs are expected from power devices, converters, photonic devices and analog/mixed signal circuits.

2.2.4.2 Destructive SEEs

Destructive SEEs cause permanent damage to and non-recoverable loss of functionality of the device. Destructive SEEs also depend on the technology and the most common types are presented as follows:

- **SHE**
  A single event hard error (SHE) is a non-recoverable change in the logic state of a device, often associated with stuck-bit. The mechanism is similar to an SEU but could lead to a total loss of operation and is hence declared as destructive event.

- **SEL**
  A single event latchup (SEL) is a rapid increase in the current and is generated when the energized particle triggers on a pair of the parasitic transistors and thus results in a self-maintained short-circuit condition. SELs are common for CMOS technologies and could lead to thermal destruction. They can however be mitigated, typically by a reset or power-cycle.

- **SEB**
  A single event burnout (SEB) affects mainly power MOSFETs and may cause a device's destruction due to high current states and Joule effects as the result of a particle strike that enables a parasitic transistor. SEBs are destructive conditions and can be protected by external circuits [27].

- **SEGR**
  A single event gate-rupture (SEGR) is caused by particle strikes generating a damaging ionization column between the gate oxide and the drain of a MOSFET. The permanent damage in the gate insulator (SiO_2) layer typically results in a leakage current and destroys the device's ability to control and regulate the current flow.

2.2.4.3 Types of SEE in correlation to technology and environmental conditions

The response to non-destructive or destructive SEEs depends on multiple factors, including the technology being used and the environmental conditions. Specifically, destructive events such as SELs have proven to be more critical when the temperature is increased. An overview of responses to SEEs in correlation to characteristics of and trends in the device technology (e.g. feature size or cell density) and environmental behavior is presented in Table 2.1.

TABLE 2.1: SEE types and their correlation to environmental conditions and technology trends, according to [28].

	Non-Destructive				**Destructive**			
Trend	SEU	MBU	SEFI	SET	SHE	SEL	SEB	SEGR
Feature size ↓	↑			↑	↑		↑	
Cell density ↑	↑	↑						
Voltage ↓	↑	↑					↑	
Current ↑							↑	
Temperature ↑						↑	↓	
Temperature ↓						↓	↑	
Speed ↑	↑				↑			
Pulse width ↑				↑				

Some of the most common electronics and their susceptibility to SEEs are presented in the following list, according to [28, 29]:

- **Logic elements**
  Logic devices or elements such as NOR, AND or NAND, inverters and comparators are mainly susceptible to SETs and changes in the logic states (flip), known as SEUs. For comparators, SELs needs to be considered, for instance when they are built on CMOS technology.

- **Linear and analog devices**
  Linear and analog devices are commonly known for functions like voltage regulators or amplifiers and contain different technologies such as bipolar transistors (BJT) and/or MOSFETs. Amplifiers, e.g. operational amplifiers are sensitive to SETs whereby power amplifiers mainly are based on MOSFET technologies and thus are susceptible to SEBs. Voltage regulators are built of transistors, diodes and resistors, complementary to operational amplifiers. They are also used as power devices as described below.

- **Power devices**
  Common power devices include regulators and switches, such as step-down converter, low-drop out (LDO) regulators etc. They are sensitive to SETs as described for linear and analog devices and SELs.

- **Power MOSFET**
  MOSFET are classified in n-channels and p-channel technologies. While p-channel MOSFET are practically immune to SEBs, n-channel technologies are sensitive to SEBs and SEGRs due to their parasitic NPN transistor structures [30].

- **Memories**
  Memories are categorized into non-volatile and volatile devices. For volatile memories, common technologies like SRAM are being used for random access memories. SRAMs as seen as a storage element, basically consist of a flip-flop or latch built of bipolar transistors, an inverter and logic elements. Non-volatile memories, such as flash devices, are based on logic elements like NAND or NOR gates. Fully built-in memories also consist of state-controllers and other complex circuits. Thus, they are susceptible to a broad range of SEEs as summarized in Table 2.2.

- **Converters**
  Converters are mostly known for ADCs or DACs that contain at least a comparator element which makes them sensitive to SEL. If other technologies are integrated, like clocked gate elements or registers, SEUs and SETs needs to be considered as well. Besides ADCs/DACs, AC-DC converters also belongs to the converter family. Such devices use BJTs and MOSFETs and are sensitive to SEL, SET, SEB and SEGR.

- **Complex integrated circuits**
  Examples for complex integrated circuits are FPGAs or ASICs. Commonly known FPGAs are hardware logic devices that use logic gates and memory elements. They are typically manufactured on SRAM, flash or anti-fuse technology. Thus, the SEE sensitivity varies from SELs to SEUs. ASICs are specifically designed integrated circuits that can contain memory blocks and microprocessors making them susceptible to SEUs, SETs, SEFIs and SELs for CMOS technologies.

The susceptibility for different SEE types to the previous discussed electronic components and different technologies such as bipolar, CMOS, BiCMOS or silicon-on-insulator (SOI) are summarized in Table 2.2 on the following page.

This overview can specifically be important for further investigations into the device selection process (section 4.2.1) in terms of choosing between high-reliability products and low-cost COTS alternatives for development of the system design.

TABLE 2.2: SEEs and their applicability to electronic components and technologies, according to [28, 29].

Type	**Non-Destructive**				**Destructive**			
Devices	SEU	MBU	SEFI	SET	SHE	SEL	SEB	SEGR
Memories	✓	✓	✓	✓	✓			
Logic (latch)	✓	✓			✓			
Logic (combi)			✓	✓		✓		
State controllers			✓					
Analog/Mixed circuits				✓			✓	
DSPs, FPGAs and ASICs	✓	✓	✓		✓	✓		
Power MOSFETs							✓	✓
Power devices				✓		✓		
Converters	✓			✓		✓	✓	✓
Technologies								
CMOS, BiCMOS or SOI	✓	✓	✓	✓	✓	✓		
Power MOS							✓	✓
Bipolar	✓			✓				

2.3 Error rate determination for space applications

In order to determine the behavior of electronic devices and systems that are affected by radiation, it is important to know the properties of the radiation environment and the devices' or systems' sensitivity. Radiation conditions depend on the target orbit as mentioned in section 2.1 and can be predicted by simulation tools and computer-based models. The following sections outline the basic terms and procedures used for understanding the process of error rate determinations, based on radiation test results.

2.3.1 Radiation environment models

There are several models available that predict the (integral) particle flux and dose for GCR, solar and trapped particles. Common models are AP8 (protons) and AE8 (electrons) for trapped particles, GCRs ISO 15390 or CREME96 for GCR and emission of solar protons (ESP) or jet propulsion laboratory (JPL) (NASA) for solar particles

[31]. The calculation of dose-effects (TID) is usually done with dose depth or by 3D-Monte Carlo analysis. Software (SW) tools like SHIELDOSE-2 calculate electron and proton doses for aluminum planar and spherical shields. The input for such analysis is the electron and proton flux. Tools that can be used to simulate the environmental radiation conditions and predict error rates are OMERE [32] or SPENVIS [33].

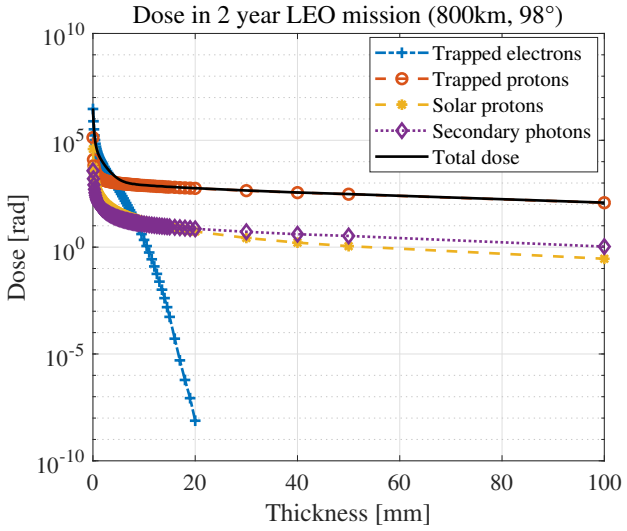
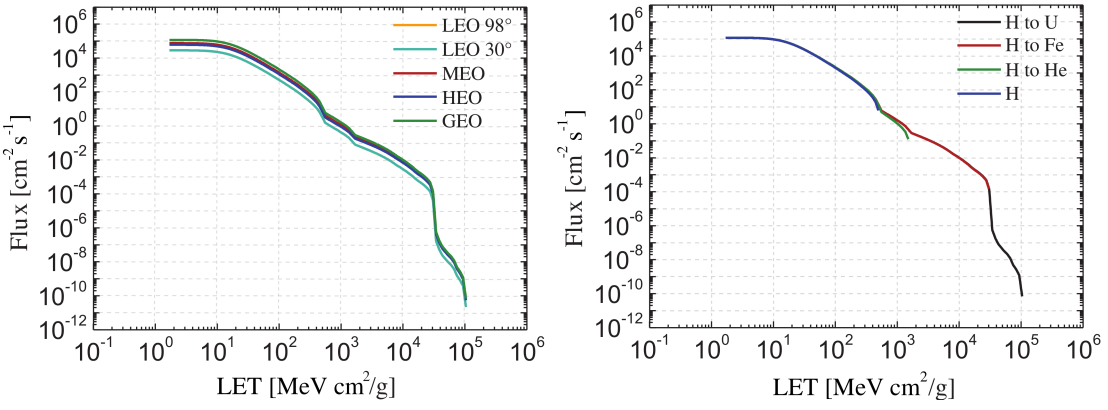


FIGURE 2.12: Calculated dose for a two years LEO mission (800 km altitude, 98°) vs. aluminum shielding thickness, using OMERE [32]

Figure 2.12 shows the particle distribution for a two-year LEO mission with respect to aluminum shielding. The integral flux, or integral LET spectrum, for different types of orbit (LEO to GEO) is presented in Figure 2.13 (a). The kink in the integral flux (the so-called *iron knee*) is based on the different particle elements in the spectrum as illustrated in Figure 2.13 (b).



(a) Integral flux for different orbits

(b) Element contribution for integral flux

FIGURE 2.13: Integral flux / integral LET spectrum for different orbits and missions (a) and the element contribution (b), simulated using OMERE [32] and according to [34]

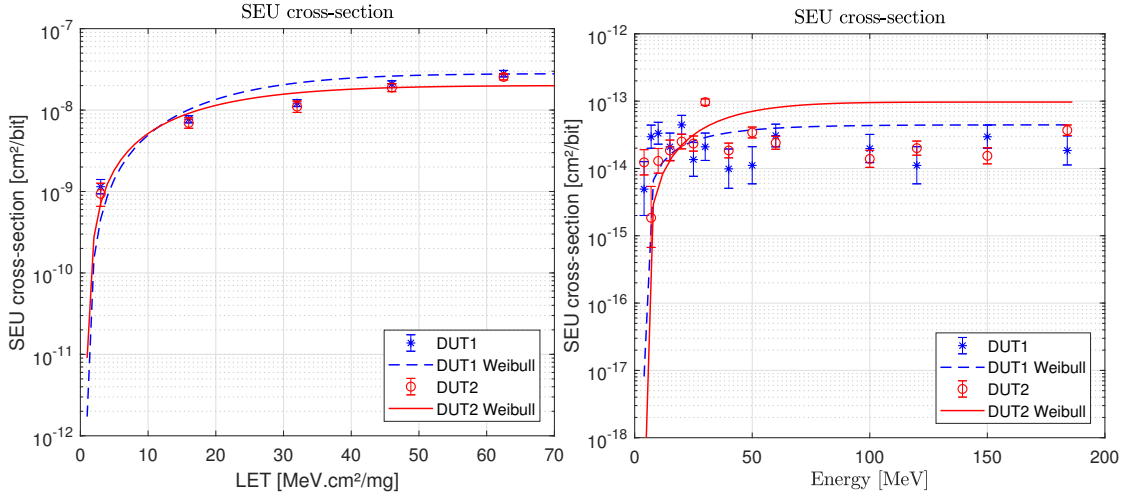
The integral LET spectrum becomes essential for in-orbit error rate predictions, especially for SEEs as discussed in more detail in the following section 2.3.2.

2.3.2 Error rate determination

To determine or predict the error rate in orbit, two parameters are important: (1) the SEE cross-section (σ), and (2) the integral LET spectrum of the radiation environment as discussed in the previous section 2.3.1. The cross-section can be viewed as the probability that a type of event will occur in a given radiation environment and is typically expressed in cm^2 per device/system. For memory devices, the cross-section is additionally divided by the bit-capacity of the memory (cm^2 per bit). The cross-section thus defines the SEE response of the devices under particle irradiation as defined in equation 2.1

$$\sigma_{event}(E_{Proton}, \mathrm{LET}) = \frac{N_{events}}{F} \tag{2.1}$$

N_{events} is the number of SEE events and F *(Fluence)* the total number of particles per cm^2 ($\# \cdot cm^{-2}$) and constitutes the integrated particle flux ($\# \cdot cm^{-2} \cdot s^{-1}$) over a certain time period. The cross-section is given over particle energy for protons or the LET for heavy-ions as shown in the example given in Figure 2.14.



(a) Cross-section vs. LET

(b) Cross-section vs. energy

FIGURE 2.14: Cross-section example for heavy-ion irradiation over the LET (a) and the proton beam energy (b)

In principle, the cross-section is discretely evaluated for multiple energies and LETs, displayed as dots in Figure 2.14. The bold and dashed lines thereby depict a fitting curve that takes into account possible Poisson fluctuations on event counts that allow for the bounding of the SEE rate at a given confidence-level. This becomes especially important if the event numbers counted are low and statistical errors no longer become

negligible. A commonly used fitting method is the Weibull function as given in equation 2.2:

$$\sigma(E_{Proton}, \mathrm{LET}) = \sigma_{sat} \left(1 - e^{-\left(\frac{\mathrm{LET} - \mathrm{LET}_{th}}{w} \right)^{s}} \right) \tag{2.2}$$

The LET_{th} is the LET or energy (for protons) threshold which is the lowest tested value affecting the device or system that leads the SEEs occurring. The saturation cross-section (σ_{sat}) represents the maximum number of events being counted in relation to the exposed particle fluence. W (width) and s (shape) are fitting parameters for the Weibull function and need to be determined to achieve the best fit result [35]. Other fitting methods can be applied, such as the two-parameter Bendel function, which is often used for cross-sections at proton irradiation [36].

Furthermore, uncertainties need to be taken into account on the cross-section as given by equation 2.3:

$$\delta\sigma_{event} = \sqrt{\delta N_{events}^2 + \left(N_{events} \cdot \frac{\delta F}{F} \right)^2} \tag{2.3}$$

The term $\frac{\delta F}{F}$ is the uncertainty of the fluence being measured during the test (e.g. $\pm 10\,\%$) and the term δN_{events} is the variance on the measured number of events. It is assumed that SEE events are random and that the probability of events follows a Poisson distribution. The variance on the number of events is then calculated from the chi-square distribution for a given confidence-level (e.g. $95\,\%$). Thus, in cross-section figures, error-bars are presented with lower and upper boundaries showing the variance of counted numbers of event and thus their confidence (see Figure 2.14).

To further investigate the error rate prediction, two pieces of information need to be derived from the cross-section: (1) the LET or energy threshold, and (2) the cross-section saturation (σ_{sat}). A simple approach for calculating the error rate is to multiply the cross-section saturation (σ_{sat}) with the integral flux (Φ) of the radiation environment prediction, which is extracted from the LET or energy threshold of the cross-section (LET_{th}):

$$Rate = \Phi(\mathrm{LET}_{th}) \cdot \sigma_{sat} \tag{2.4}$$

Figure 2.15 on the following page illustrates the integral flux-extraction from the LET_{th}. One has to consider that units of the LET from the integral flux and the cross-section differ by a factor of 1000 (mg to g). This approach is a very basic method for determining

and evaluating the in-orbit error rates. However, considering the complex statistical analysis of the test results (e.g. Weibull fitting to determine the real energy or LET threshold and cross-section saturation), tools such as OMERE or SPENVIS should be preferred for more accurate error rate predictions.

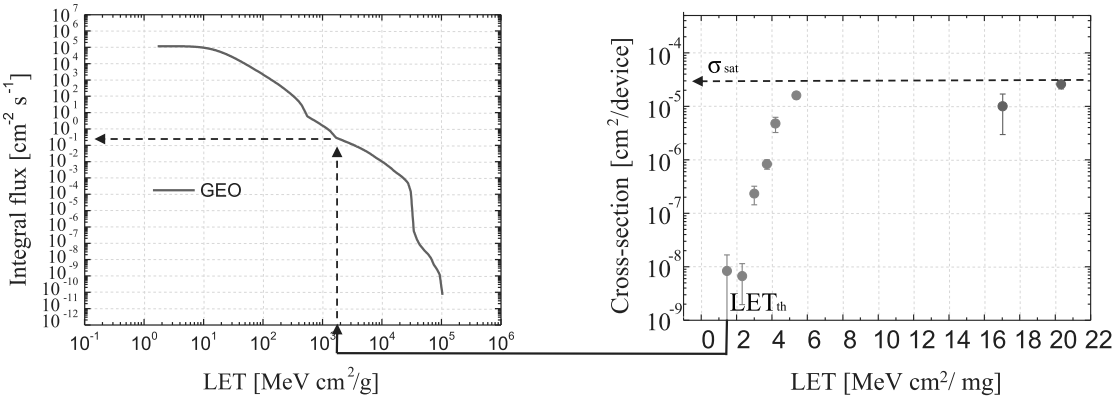


FIGURE 2.15: Illustration of integral flux-extraction from cross-section results, according to [34]

Chapter 3

Software-defined radio systems in space flight

This chapter presents the state-of-the-art for SDR systems in space flight. A general overview of SDR is briefly introduced with its main intention as well as its technical history and evolution. SDR technologies have been identified as having potential advantages for space flight and have been used for various missions in the past. However, recent SDR systems in space flight have shown limitations and disadvantages compared to the latest technologies, evolved for terrestrial wireless applications such as for mobile services like 4G, video broadcasting systems (e.g. DVB-x2) or other high-data volume throughput applications.

3.1 The software-defined radio

Wireless communication has become an essential part in daily lives. With the exponential growth of needs, radio systems were required to become smaller, more flexible and cost-efficient. In the 90s, the first works have been published that introduce a software radio concept that use software instead of traditional hardware (HW) radio system designs [37–40]. Various definitions can be found to describe radio systems that are described by software: software-based radio (SBR), SDR or just software radio (SR). The SDR Forum, working in collaboration with the institute of electrical and electronic engineers (IEEE) P1900.1 group, has worked to establish a definition of SDR that provides consistency and a clear overview of the technology and its associated benefits [41]. An SDR allows features such as updating and upgrading through simple re-programming, without redeveloping or replacing the hardware on which the specific radio application runs. This upside has resulted in one of the most important factors: the reduction of development and hardware costs.

The most common concept and architecture for a high-level SDR is presented in 3.1 and consist of an *antenna system*, an *RF front end*, a *digital front end* and the *digital baseband* (or digital back end).

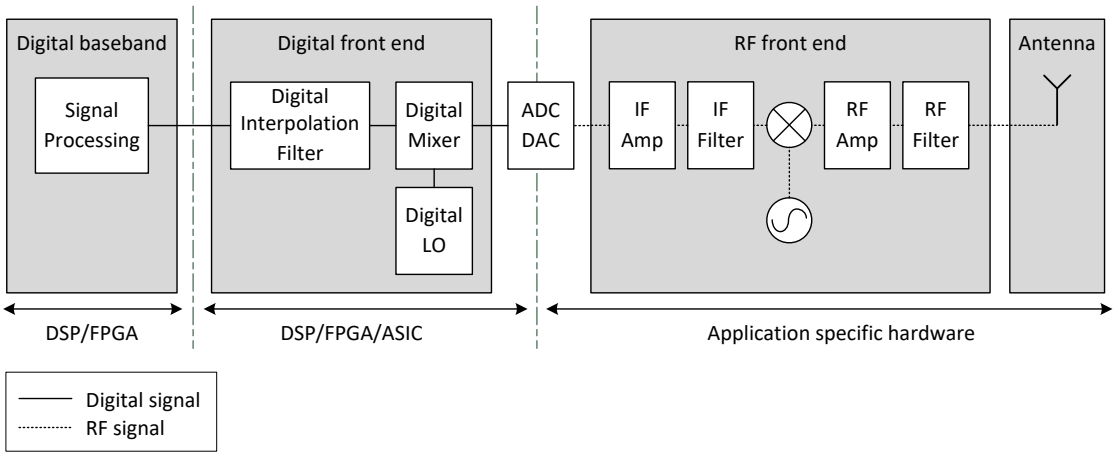


FIGURE 3.1: High-level system architecture of common SDR systems

Typically, the RF front end is tailored and designed to application-specific requirements such as the frequency band selection, as well as the amplification of the received and to be transmitted waveform from or to the antenna(s). Another major function of the RF front end is to down-convert the high-frequency signals to an intermediate frequency (IF) that is designed to interface with the analog-to-digital converter (ADC) and digital-to-analog converter (DAC), respectively. ADC and DAC devices represent the interface between the digital and RF domains and are also specified by the application-specific requirements. Because the main advantage of an SDR is its flexibility and the capability of simple reconfiguration by software, the digital domain plays an essential role in such system. A digital front end is often used in SDR systems to further convert the digitized signal from or to the baseband and to perform pulse shaping through digital interpolation filters [42]. Digital front ends are typically implemented into FPGAs, but specially designed application-specific integrated circuit (ASIC) are also commonly used. In the digital baseband, further signal processing takes place which for example includes the frequency shift compensation, the clock recovery, the modulation/demodulation, encoding/decoding or encryption/decryption of the digital data. The baseband signal processing is then usually a programmable implementation and can take place in several different technologies, such as in digital signal processors (DSP), general purpose processors (GPP), FPGA or in programmable system-on-chip (SoC) [38, 43]. Depending on the technology being used, the digital front end could also be implemented on the digital baseband hardware. Some SDR architectures also allow a direct conversion (zero-IF or homodyne architectures) from or to the digital baseband, making a digital front end obsolete [44].

3.2 Software-defined radio systems in space flight missions

The advantages of SDR technologies have also been identified by the space flight community [45, 46]. SDRs were initially used for experimental payload designs, primarily used by universities and research institutes for small satellite and CubeSat missions due to their high integrity and low-power consumption [47]. Agencies such as the national aeronautics and space administration (NASA) started their investigation into SDR system development to ensure re-usable and re-programmable radio systems for their space flight missions in the early 2000s [48, 49]. One focus of NASA was the development of an autonomous radio receiver for deep space missions. One scenario described by [50] is the use of such autonomous radios as a communication relay systems between two or more distant planetary rovers. This scenario is also applicable to other kinds of spacecraft. Intelligent and autonomous radio systems that are capable to reconfigure on their own to the specific radio characteristics of each individual spacecraft or rover ease scheduling processes and reduces the time required to reconfigure the systems, controlled via ground stations on Earth. Moreover, these systems may be able to handle unpredictable and anomalous events, such as signal degradations due to Doppler shifts or unknown or unfamiliar properties of the signal transmission.

The first highly capable SDR developed by NASA, *Electra*, was presented in [51] to support the upcoming decade of Mars exploration. Electra is based on a compact design with a radiation-tolerant FPGA that is used to perform baseband signal processing, such as carrier tracking, timing recovery and digital demodulation. In Europe as well, the European space agency (ESA) carried out dedicated funding for the development of SDR-based communication systems in their ARTES 3-4 program [52]. As one example, ESA funded the development of an S-Band telemetry, tracking and control (TTC) transponders for their first six ESA-class 3 FORMOSAT-7 spacecraft [53]. The interest in, and need for, reconfigurable radio systems technology increased rapidly and so SDRs became state-of-the-art in space communication systems.

However, one of the biggest challenges during recent years has been to establish a high level of reliability for those systems, which has also limited the potential use of SDRs. One major reason is that the electronics required for flexible radio systems such as DSPs or FPGAs are not widely available in space-qualified grade and, if they are, these are very expensive, require long lead-times and have much less performance compared to commercial technologies designed for terrestrial applications.

SDR systems developed by commercial space industries need to guarantee a high level of reliability, and risk acceptance in using non-space qualified electronics is not given in many space missions. On the other hand the survey of SDRs being designed and used for satellite communication, presented in [54], shows an increasing interest from

universities for SDR technologies in their CubeSat missions. Due to their very limited budgets, the use of space-qualified hardware is not usually considered and thus, the use of commercial electronics is unavoidable but also offers more flexibility and more efficient performance with lower power consumption. As a conclusion and based on the available SDRs on market, two categories are defined: (1) high reliable, space-qualified SDRs that are specially designed for the harsh environment in space, and (2) high-risk, low-budget SDRs which are commonly used for small-satellite and CubeSat missions. Due to the different design approaches and mission requirements, a wide gap in terms of performance, costs and reliability has opened up, which will be discussed in more detail in section 3.3.

3.3 Limitations and disadvantages

As mentioned in the previous section 3.2, SDRs have already been used in several past space flight missions and have become state-of-the-art for radio systems on spacecraft. However, due to differing mission requirements, the available SDR-based (communication) systems show large variations in their design approaches and thus, in their costs, performance and desired reliability. In this section, the major differences between both types of available system are discussed to highlight their advantages, disadvantages and limitations and to evaluate methods and possibilities for developing a cost-efficient and powerful radio system that is also able to fulfill a broad range of different requirements concerning reliable operations in space.

TABLE 3.1: Comparison of the pros and cons between space-qualified SDRs and low-budget SDR systems for CubeSat and small-satellite missions being used as spacecraft communication systems

Space-Qualified SDRs	**CubeSat SDRs**
Pros	
High reliability	Low development and manufacturing costs
Compatibility	Short lead-times
Qualification	Performance and power efficiency
Documentation	Many suppliers
Manufacturing transparency	Size and weight
Cons	
Lead-times and costs	Non-transparent manufacturing
Few available suppliers	Non-conformance
Lower performance	Inadequate documentation
Power consumption	Fewer frequency bands
Form-factor, size and weight	Reliability

Table 3.1 presents the pros and cons of space-qualified and CubeSat SDRs, where the definition of CubeSat is used as synonymous for high-risk and low-cost SDR design approaches. High-risk acceptance is thereby directly correlated to a poor reliability. This is clarified by the failure rate of past CubeSat missions. Studies by Swartwout reported a failure rate of about 40 % among university built CubeSats [55, 56], whereby a set of failed missions can be linked to thermal and radiation issues [57]. Besides the most obvious differences, the reliability approach and costs, other important factors need to be considered for a comparison. On one hand, space-qualified systems support a well documented and transparent qualification and manufacturing process, while CubeSat systems do not usually provide such detailed information. This is basically owing to the use of COTS electronics where each vendor could not guarantee product traceability, parts-screening and end-of-life information. CubeSat technologies are often pronounced and advertised by having flight-heritage, once their use has been demonstrated on a space mission. However, the environment, specifically the influence of radiation, will significantly change from orbit to orbit (low Earth orbit (LEO), geostationary orbit (GEO) or deep space) and the date of mission. This means that a system that has been proven to operate for example in a LEO for one year is not guaranteed to survive or to operate properly at a different altitude or over an expanded lifetime. Thus, the pronounced statement *flight heritage* needs to be seen carefully. On the other hand, the space-qualified electronics used in high-reliably SDR systems are much less efficient, require longer lead-times and are often subject to export control regulations.

Due to the rapidly growing numbers of CubeSat missions in the past decade, a certain market has been established comprising many companies that have been founded or spun off from universities. Thus, a series of radio systems (incl. SDRs) for CubeSats and small-satellites mission are available from different enterprises, mainly for TTC applications or scientific/Earth observation payloads such as aircraft or vessel tracking. Commonly known vendors for CubeSat technologies are ISIS Space, EnduroSat, GomSpace or Nanoavionics. One issue, specifically related to ground-to-satellite communication (TTC), is that companies develop their own standards and protocols, e.g. the CubeSat Space Protocol [58]. Hence, it becomes hard to be compliant with certain mission requirements and this could necessitate extensive modifications to other spacecraft systems. Space-qualified TTC systems are usually designed and specified by the recommendation of commercially used standards, as defined in the consultative committee for space data systems (CCSDS) or European cooperation for space standardization (ECSS). Those standards are often not feasible to handle for universities and their spun-off enterprises.

Another disadvantage of SDR-based communication systems in CubeSat missions is the limitation of available operable frequency bands, which are mostly restricted to ham radio frequency bands, such as very high frequency (VHF) and ultra high frequency (UHF)

as depicted by [59]. Operations in ham radio frequency bands are free of charge to use and require a ham radio license. Since there are no specified bands for spacecraft communication TTC, users have to deal with very narrow available bandwidth and interference by other users. For commercial space missions, dedicated and allocated frequency bands, typically in S-Band, are used for ground-to-satellite communication and vice versa. The required allocation procedure needs are coordinated by the international telecommunication union (ITU) and are usually expensive and not affordable for universities and their spun-offs.

3.4 Summary

This chapter introduced the history and principles of SDR systems and how they have been used in past and present space flight missions. Due to the conservative approach of the commercial space industry, the advantages of SDRs have only been partially exploited because of the limited availability of space-qualified electronics. With the growing number of CubeSat missions, reconfigurable radio systems have become more popular and have expanded the market. However, the approach of those systems is completely different from space-qualified SDRs of the commercial space industry and not sufficient for most types of commercial space flight mission. The main differences between space-qualified and CubeSat SDR-based communication systems have been presented and their advantages and disadvantages highlighted. The wide gap between both approaches is the major driver for this work, which aims both to develop a small integrated radio system that uses all the possible benefits of SDR technologies, and provides a high level of reliability with respect to commercial space flight mission requirements.

Chapter 4

A novel approach to a highly integrated and radiation-tolerant solution for multi-band radio applications in space systems

This chapter sets out the design approach of a highly-integrated and radiation-tolerant solution for multi-band radio applications in space systems. As discussed in chapter 3, available SDRs for space applications differs markedly with respect to costs, performance and reliability concepts. The design aspect presented here will combine the benefits of both given state-of-the-art SDR systems and reduce their limitations and disadvantages. The main goal is to develop a system that is primarily cost-effective but which can also handle the dangerous radiation influences in space and that takes into account the highest possible degree of reliability. This is clearly not possible with the use of space-qualified or RadHard electronics only and requires a careful selection of EEE components in the system design. The challenge in this selection process on one hand is to identify whether the required electronics are available on a space-qualified, RadHard level and whether their use makes sense with respect to the overall system view. For system-critical electronics which are not available RadHard or space-qualified, a detailed investigation into whether and how they can be used in the desired SDR architecture is crucial.

It has to be mentioned that space-qualified electronics may not be inherently immune to radiation, as for RadHard devices. There are devices available that cover all qualification standards for space but do not consider radiation. To avoid misunderstandings, it is assumed for this work that space-qualified electronics are also RadHard.

4.1 System design description

As mentioned in the introduction to this chapter, one of the key design drivers is cost efficiency. This includes manufacturing costs as well as development costs. The development costs are thereby not limited to the initial system design. One has to consider redesigns and specific modifications with respect to the desired application, operated by the SDR. One typical application, as mentioned in section 3.2, is the TTC system for spacecraft communication, but the SDR could also be used for satellite-bus related subsystems such as a global navigation satellite system (GNSS) or global positioning system (GPS) receivers for altitude determination and control. Furthermore, Earth observation payload such as for signal detection of automatic identification system (AIS) from ships/vessels [60] or automatic dependent surveillance broadcast (ADS-B) messages transmitted by an aircraft [61] are often implemented in SDR systems. However, all these applications are operated in different frequency bands and require specific RF devices such as filters, amplifiers or frequency mixers. Based on the principles of SDR, namely digital signal processing, these modifications are usually required for the RF front end. For this reason, a board separation of the RF front end and the baseband processing unit (BPU) is desirable. In this case, the development and manufacturing costs are limited only to the RF front end board if application-specific modifications are required. Based on the complexity and number of devices used on the RF front end board, the manufacturing costs are just a fraction compared to the costs of the BPU (Motherboard). Figure 4.1 shows a high-level system design of the proposed SDR architecture.

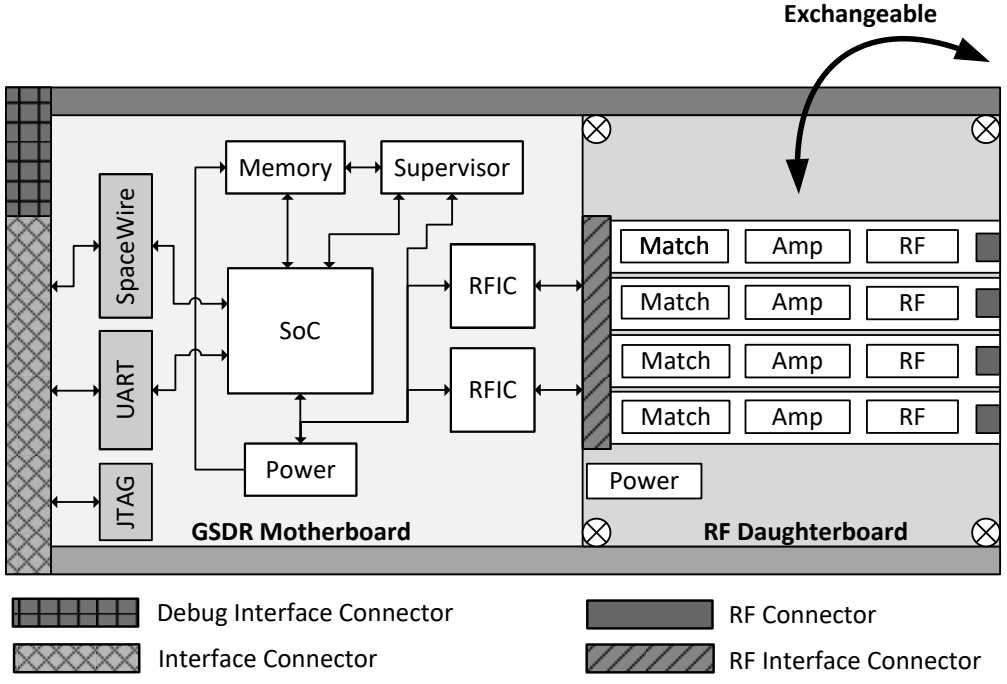


FIGURE 4.1: High-level system design of the proposed SDR architecture.

To support a broad range of different applications on the SDR, it is also important to provide adaptable sampling rates of the ADC and DAC such as described in [62]. Oversampling could result in powerful operations in the BPU and on the other hand, a too low sample rate would limit the number of possible applications since the Nyquist–Shannon sampling theorem must be followed [63]. With the increasing demand to reduce the cost and size of communication equipment, the traditional method of off-chip system design components has been moving to on-chip designs to integrate as much of the wireless transceiver functionality as possible into a single technology [64]. This RFIC technology has become very popular in the past decade and is available for different kinds of application such as for mobile phones, wireless local area network (WLAN), ultra wideband (UWB), GPS and bluetooth devices [65–67]. The latest RFIC technologies, usually developed for wideband mobile applications such as 3G or 4G, allow the programmability of different functionalities such as sampling rates, mixing frequencies and RF filter bandwidths [68, 68]. The transfer of this technology into classic SDR architectures enables the operation of several applications in different frequency bands on a single radio platform and allows a simple and clear separation to RF-specific front end devices. This novel design approach is what is further defines as generic software-defined radio (GSDR). With respect to improving system reliability for the desired operations in space, it is further important to identify which technology of the GSDR system approach is required and what qualification-levels are available. Therefore, the system architecture is divided into functional blocks as depicted in the system breakdown structure in Figure 4.2.

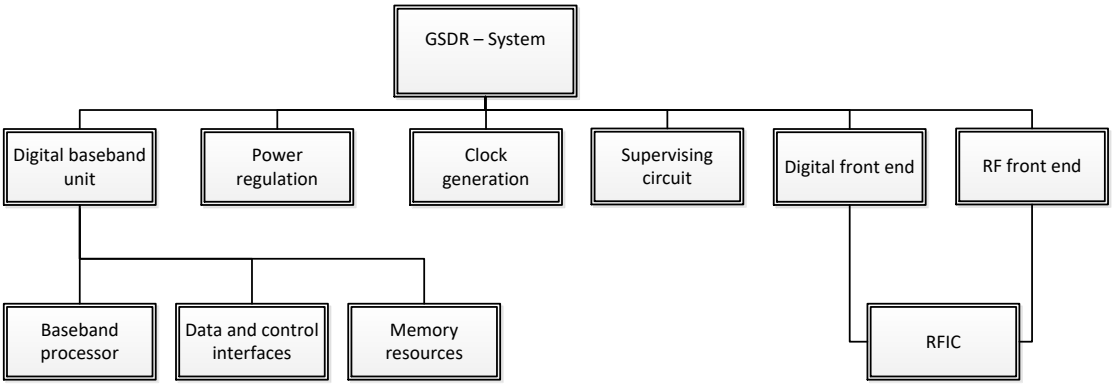


FIGURE 4.2: GSDR system breakdown structure.

Below, these functional blocks are described with their intended system-relevant functionalities. Following the definition of a classic SDR architecture from section 3.1 (see Figure 3.1), the BPU is sub-categorized into the baseband processor (BBP), the data and control interfaces and the memory resources. Due to the intended use of the latest RFIC technology, the digital front end and the RF front end functional blocks can be combined (RFIC).

- **Baseband processor**
  The BBP is one of the core devices for the BPU in the GSDR system architecture. The BBP is responsible for digital data processing, whether this is related to application-specific signal processing, e.g. modulation and encoding for TTC, or the implementation for communication (e.g. protocols) to other external systems such as the on-board computer (OBC) of a spacecraft. For the BBP, formally DSP, FPGA or SoC, as also known from state-of-the-art SDR systems, are used.

- **Data and control interface**
  To support access to the GSDR, multiple types of interface are implemented in the design to interconnect with other external systems. These interfaces are for example required to provided the signal-processed application data in real-time or to obtain system-relevant information such as internal temperatures, configuration status or other health conditions of the radio system (housekeeping data). Interfaces are also important for controlling or configuring the GSDR, e.g. for the reconfiguration of application-specific data processing or general system updates. Depending on the required data rate, different electrical standards such as RS422 or low-voltage differential signaling (LVDS) are considered. For initial programming of system configuration and to support direct access to the BBP, a joint test action group (JTAG) interface is mandatory.

- **Memory resources**
  Volatile and non-volatile memory are used to provide computing resources to the BBP and data storage capabilities for sensitive data, such as boot and system critical configurations. The memory resources are separated into static and dynamic memory devices with different purposes as described as follows:

  - **Static memory**
    The usually implemented static memory is a non-volatile flash device that contains sensitive data (e.g. boot images and configuration data) that are required by the system. This type of memory can also be used for intermediate data storage of payload or system-status data. Those data can be requested on demand by external systems (e.g. spacecraft OBC).

  - **Dynamic memory**
    The GSDR system uses dynamic memory devices (e.g. double data rate (DDR)3-synchronous dynamic random-access memory (SDRAM)) to provide computing resources to the BBP. The dynamic memory is generally required by the system software or the operating system (OS) and is essential in the signal processing chain between the RFIC device, the BBP and the static memory for data storage.

- **Power regulation**
  Power regulation is usually independent of the general function (signal processing) of an SDR, but is a key part of any kind of electronic system. Even if the complexity compared to other functional groups, e.g. the BPU or RFIC, seems to be low, the power regulation unit has a direct impact on all system electronics and needs to work reliably under all circumstances. Due to the GSDR system's complexity, including various types of devices and electronics, different sub-voltages domains are required and this leads to a large number of power regulators. Thus, the power regulation unit also becomes complex (e.g. due to power-up sequences), specifically with the desired approach to develop a highly integrated and cost-efficient radio platform.

- **RFIC**
  The RFIC is one of the most important devices in the system, since it shall compromises the RF front end, digital front end and ADC/DAC functionalities. Due to the latest RFIC technologies, highly integrated solutions for SDR platforms become feasible. The RFIC is the bottleneck device when it comes to reliable operation in the intended space environment since it is relatively new on the market and potentially not designed and developed for space applications.

- **Clock generation**
  Almost every digital device in the GSDR system requires a reference clock to provide accurate data processing. In minor cases, the same clocking source can be used for multiple devices but in general each device requires its own specific clock input. Thus, one has to consider different types of clocking sources (e.g. frequency, signal type and stability), that could lead to functional system disturbances once their performance degrades and hurts their specifications.

- **Supervising circuit**
  A supervising (or supervisor) circuit observes the functionality of the system and monitors sensitive components to prevent data corruption and destructive damage, for instance due to radiation effects. The supervising circuit is usually not intended for classic SDR architectures but has an essential role if the design is to be used in space and cannot be designed with devices that are fully space-qualified or RadHard.

Each functional block has an important role in the system and is implemented with active electronic devices. Clearly, all those devices have certain dependencies on each other and failure propagation is an important criteria for the selection of system critical devices. For the specific selection criterion (e.g. the use of RadHard or COTS electronics), a detailed analysis of possible failure propagation and its impacts on the system-level reliability is discussed in the section 4.2.

4.2 Hybrid system design approach

Due to the fact that some necessary technologies for the GSDR system design approach have not been specifically developed for space applications nor a radiation environment and that the main goal is to develop a highly integrated and cost-efficient radio platform, the use of non-space-qualified, RadHard devices is unavoidable. The major questions within the development process are: how to select electronic devices with the appropriate qualification level. When is high-qualification level mandatory and when are COTS devices useful and sufficiently effective and reliable. However, it is generally agreed that there is always a trade-off between required reliability, costs and performance and there is no generic process for the selection of electronic components. The following section lays out the specific selection process for GSDR development.

4.2.1 Selection criteria for system-critical devices

The selection criteria of devices is performed for each functional block (Figure 4.2 in the GSDR system). Within this approach, firstly a tailored failure mode, effects and criticality analysis (FMECA) is performed on the functional block level to identify potential failures and their severity to the own and more important to other external systems. For the development of a radiation-tolerant system design the FMECA process applied here is strongly focused on failures induced by radiation effects. Secondly, a technology assessment and rating is made to evaluate which required functionality and technology is available on different qualification-levels. Based on the FMECA severity analysis and the assessment/rating results, specific devices are selected for the GSDR functional blocks. The use of COTS is essential and indeed unavoidable for this development. Thus, it is important to identify their risks and to define criteria for selecting appropriate COTS devices for their desired use in space.

4.2.1.1 FMECA

The FMECA is a common method in the reliability assurance and failure analysis that creates a link between potential failures, the causes of those failures and their impact on other functional blocks or in the overall mission [69]. Specifically for space missions, the ECSS has introduced its own standards according to FMECA principles and requirements [70]. The presentation of the assessment is structured with respect to the following logic:

1. The hardware will be decomposed in a fashion that allows for the simplest analysis possible. The depth of detail in any failure analysis is limited to the point where

necessary isolation and recovery procedures can be defined. In practice, units are treated as far as possible as black boxes, and any failures observable from the outside will be dealt with.

2. For each failure, a typology of classifications has been introduced in order to distinguish between failures causing system loss, system degradation and failures without any system impact.

The following Table 4.1 lists the possible severity categories to be used:

TABLE 4.1: FMECA severity categories, according to [70].

Severity level	**Severity number (SN)**	**Severity category**	**Failure effect**
1	4	Catastrophic	Propagation of failure to other systems, assemblies or equipment
2	3	Critical	Loss of functionality
3	2	Major	Degradation of functionality
4	1	Negligible	Minor or no effect

Table 4.1 also shows the *severity number (SN)* applied at the different severity categories with associated failure effect. To provide a criticality ranking of assumed failure modes according to ECSS-Q-ST-30-02C [70], besides the definitions of the severity-levels and their respective SN, a *probability number (PN)* needs to be considered. The SN should be assigned to the corresponding failure modes/effects and the PN shall be assigned corresponding to the probability of occurrence of the assumed failure mode. The severity classification and therefore relevant SN-ranking is assigned independent from possible redundancies in the system. Thus, existing device or component redundancy does not affect the severity classification.

TABLE 4.2: PN and DN levels, limits and numbers, adapted from [70].

PN level	**PN limits**	**PN/DN**	**DN level**
Very likely	$P > 1 \times 10^{-1}$	**4**	Extremely unlikely
Likely	$1 \times 10^{-2} < P \leq 1 \times 10^{-1}$	**3**	Unlikely
Unlikely	$1 \times 10^{-4} < P \leq 1 \times 10^{-2}$	**2**	Likely
Extremely unlikely	$P \leq 1 \times 10^{-4}$	**1**	Very likely

A quantitative PN-ranking approach can be used when specific failure rates and probability of occurrence data are available (e.g. from equipment datasheets or test reports). The PN is hard to determine at an early stage, especially on radiation effects when not enough data are available for COTS devices and which probably need to be investigated by testing. Often, the PN is given as a qualitative number or expression (very likely to extremely unlikely) by engineering judgment and is determined based on experience

for the expected radiation effects in electronics and technology. The limits provided in Table 4.2 are tailorable and depend on the application-specific requirements. According to [70], a *criticality number (CN)* can be calculated including a factor for the probability of detection of failure modes (*detection number (DN)*). The DN is multiplied by the product of SN and PN as shown in equation 4.1 and this affects the CN for each individual failure mode by potential detection and recovery processes, as applied specifically in section 5.3 for selected system-critical COTS devices.

$$\mathrm{CN} = \mathrm{SN} \cdot \mathrm{PN} \cdot \mathrm{DN} \tag{4.1}$$

Figure 4.3 shows a three-dimensional criticality matrix. The CN ranges from 1 to 64 depending on the probability of detection and potential recovery (DN). The classification of CN strictly depends on the accepted risk for the mission or, in the case of the work presented here, the selection of system-critical devices.

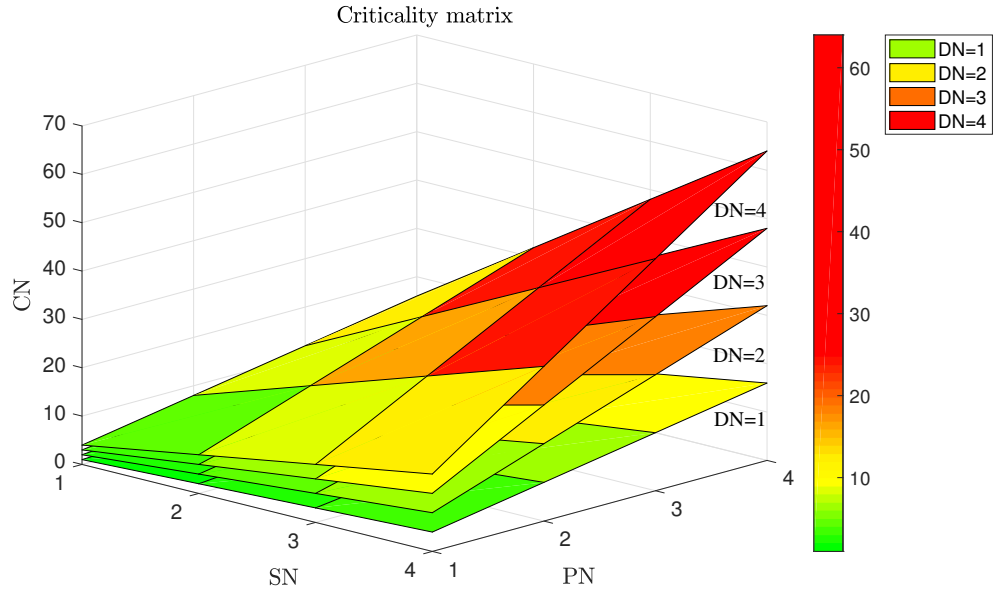


FIGURE 4.3: Criticality number (CN) matrix with applied limits for this work; see section 4.2.1.4, according to [71].

Similar to the FMECA (according to ECSS-Q-ST-30-02C), Michael Gates et al. have presented a systems engineering approach specifically tailored to criticality analysis for SEEs and their propagation [27, 72]. Their single event effect criticality analysis (SEECA) is a useful approach for the following presented procedure of the selection criteria for system-critical devices and is partly applied here. However, SEECA does not take into account the selection of qualification-levels but provides a clear structure of functional analysis based on SEEs and is also used for the FMECA and a failure recovery and mitigation analysis. Mitigation strategies that could be applied to functional blocks

where a certain amount of risk can be accepted are not directly involved in the selection criteria and implemented FMECA presented here, but will be analyzed and discussed separately in the system-level design and verification section 6.1.

4.2.1.2 Technology assessment description

Followed the FMECA analysis, a technology assessment is performed to evaluate potential candidates for the proposed functional blocks. This technology assessment includes a also rating of given technologies by certain criteria as presented as follows:

- **Level**
  Represents the best or highest available qualification-level of the rated technology or device.
- **Review**
  The review rating describes the available product traceability and notification options by the manufacturer of the desired devices (or technology).
- **Complexity**
  Complexity of devices and technologies may differ and needs to be taken into account for certain ratings. For example an FPGA has a high complexity compared to linear power regulators. With complexity, mostly the availability of higher qualification-levels decreases and radiation tests become mandatory which could also lead to long-term and expensive investigations where dedicated risk assessments may need to be applied.
- **Performance**
  Comparing performances of potential candidates is an important factor, especially when space-qualified options are available which often perform less well than state-of-the-art COTS EEE parts.
- **Costs**
  Costs are probably one of the main drivers for development. Higher costs are often associated with higher qualification-levels and should therefore be taken into account in the rating for the device and in the technology assessment.
- **Data**
  Specifically if RadHard or space-qualified options are not available, information about flight-heritage and radiation tests becomes necessary when using COTS solutions. The rating of available data is essential when non-space-qualified parts are chosen, since additional radiation tests could be avoided if risk assessment is deemed to be acceptable.

The rating follows a poor-to-excellent scale as presented in Table 4.3 and is especially important when intended qualification-levels from the FMECA severity analysis are not available and trade-off-decisions need to be made.

TABLE 4.3: Technology assessment and rating.

Not applicable	Poor	Moderate	Neutral	Good	Excellent
n.a.	- -	-	-+	+	++

4.2.1.3 The use of COTS parts in space applications

The use of COTS EEE parts in critical applications has a long history. For example, the U.S. Secretary of Defense William Perry's 1994 directive officially initiated the transition to use of COTS parts in military applications (also known as the Perry Memo) [73]. Since the use of COTS EEE parts in military applications has been proven to be viable, it was only a matter of time before the use of COTS started to be a driver in space applications. A host of papers, books and guidelines have already been published examining the use of COTS components in spacecraft systems [74–76].

For many spacecraft manufacturers, the use of COTS EEE parts is only an option if the performance and cost are essential drivers for the mission and no space-qualified options are available. Even if it has been proven that COTS devices were operated successfully in space, it is important to discuss their use in terms of initial parts selection, the assessment of their suitability for use in space and the resulting overall system reliability.

One major issue is that COTS parts differ and are unequal, because commercial industry cannot be forced to follow dedicated specifications and standards familiar from military and space applications. Moreover, it is also unrealistic to require commercial industry to go along with those certifications, audits and qualification commitments since they are not aiming to sell components in low volumes. Even if many manufacturers are certified to ISO9001 standard [77], COTS parts' qualifications and product traceability could vary dramatically. Usually, quality assurance for COTS devices is based on a statistical process control (SPC) due to high-volume production. The SPC is a scientific, data-driven methodology for quality analysis and results in a substantially higher quality of outgoing parts the greater the production volume. The qualification methodology for military or space-grade EEE parts on the other hand is based on testing and evaluation (e.g. by ECSS-Q-ST-60-13C [78]), because the statistical quality assurance approach of SPC is not applicable for low-volume production. To ensure a reliable use of COTS parts in space applications, several factors such as manufacturers' information and sufficient technological knowledge, based on heritage data or up-screening test results, are essential to evaluate the risk and apply further mitigation strategies.

The following points should be considered to ensure precaution in the selection of COTS EEE parts for space flight missions and to minimize the risk.

- Monitoring of obsolescence, part life cycles and counterfeit detection
- Product traceability and manufacturers' information (e.g. quality assurance, fabrication site, process information and control, lot/date code availability and lot homogeneity)
- Available and replicable data relating to long-term performance
- Temperature constraints
- Material identification (RoHS, out-gassing, risk analysis)
- Up-screening capabilities
- Available information on radiation tolerance (TID and SEE)

Often, large offsets by increased de-rating factors are taken into account for space applications, resulting in stringent reliability requirements. These offsets could be overrated and are not strictly applicable. For example, in many space applications the actual temperature conditions are mostly stable (e.g. inside the spacecraft) and will not exceed the limits for which most COTS parts are specified. Of course, there are minor cases and exceptions in which electronics are used outside the spacecraft and where temperature ranges could vary dynamically and dramatically, thus potentially exceeding the specified ratings of industrial-grade COTS devices.

Another consideration that needs to be taken into account is that most COTS parts are surrounded by a plastic encapsulation which can out-gas volatile materials, such as oxygen under vacuum conditions. These materials could condense onto sensors, optics and solar cells and will degrade their performance. This risk needs to be assessed for each mission and could be mitigated by hermetically sealed housing to limit out-gassing. Enhanced plastic options like the COTS plastic encapsulated microcircuit (PEM) are available in some cases, that avoid out-gassing and which are also specified with extended temperature ranges (e.g. -55 to +125 °C). Many researchers have shown that plastic encapsulations can be used in military and space applications and may be more reliable compared to their ceramic equivalents [79–81]. However, an appropriate housing of the system using well-placed and limited venting-holes also reduces the risk of out-gassing effects to optics.

An additional example is mechanical environmental stress, such as vibration or shock, that are often associated with space- or military-qualified parts. These stresses generally

occur only for a short duration (during launch or separation) for space missions and COTS parts would usually not be critically affected by them [82].

However, even if some requirements might be overrated and can then be neglected, there is an upcoming trend to improve COTS parts' reliability with additional up-screening of industrial-grade COTS parts to a higher qualification-level, as discussed in [83–85]. Those parts are often termed *QCOTS*, *COTS+* or *enhanced product (EP)* components and can be found in automotive electronics council-certified, or compliant automotive parts [83] (e.g. AEC-Q100 [86]). Up-screening processes can include destructive physical analysis (DPA), temperature cycling and burn-in tests to remove initial failures or additional electrical functionality tests. These are carried out by the semiconductor manufacturer or third parties. Up-screening processes are applied according to Mil-Std 883, JESD-22/26 and MIL-PRF 55365 standards and could be performed on the complete fabricated lots. Anyhow, COTS+ devices are currently rare on market, up-screening levels and details vary from vendor to vendor and minimum orders of quantity (MOQ) are often high for the end-user resulting into higher mission costs.

One interesting key feature of COTS+ components is that they are usually batched and typically assembled by a controlled baseline. Thus, product traceability is improved, counterfeiting can be insured against and changes to the fabrication technology are known which all have an important effect on the Radiation hardness assurance (RHA) COTS parts. Depending on the manufacturer, important information such as process change notification or batch codes of the COTS device is also provided without additional up-screening processes. It is comparatively likely that commercial-grade versions of space-grade components will contain the same die and are fabricated on the same hardened process [87]. Those particular items of information, for sure, are not usually provided by the manufacturer and, even if they are, this information will not guarantee the devices' or components' functionality in the space environment. Thus, even if COTS+ devices are available, the product traceability is clear and well documented, the remaining bottleneck is therefore the missing information about radiation hardness.

Radiation effects are the most critical environmental stress to the devices that cannot be neglected, unlike for temperature ranges, plastic encapsulations or mechanical stress. In any case, one has to carry out radiation testing and characterization if data are not available or the semiconductor technology is inherently immune to radiation such as for semiconductors that are based for example on gallium nitride (GaN), silicon carbide (SiC) or gallium arsenide (GaAs) [88–92]. All these wide band-gap technologies have a very robust response to TID effects and DD but could on the other hand be sensitive to SEEs [93–96]. The radiation hardness with respect to SEE is extremely depending on the application and type of operation, such as for high-voltage power devices or in RF applications [97–100]

4.2.1.4 Guidance for selecting system-critical devices

From this vantage point, it is evident that COTS devices come in different types of qualification and screening-level. It has been proven in several missions that their use in space applications is possible with an appropriate risk assessment. However, the trade-off between risk, performance and cost is often high and complex and a generic selection approach is hard to define.

Based on the FMECA severity analysis performed on each individual function block in the GSDR system design, a part selection procedure is performed in the form of a guidance, presented in the flow chart in Figure 4.4.

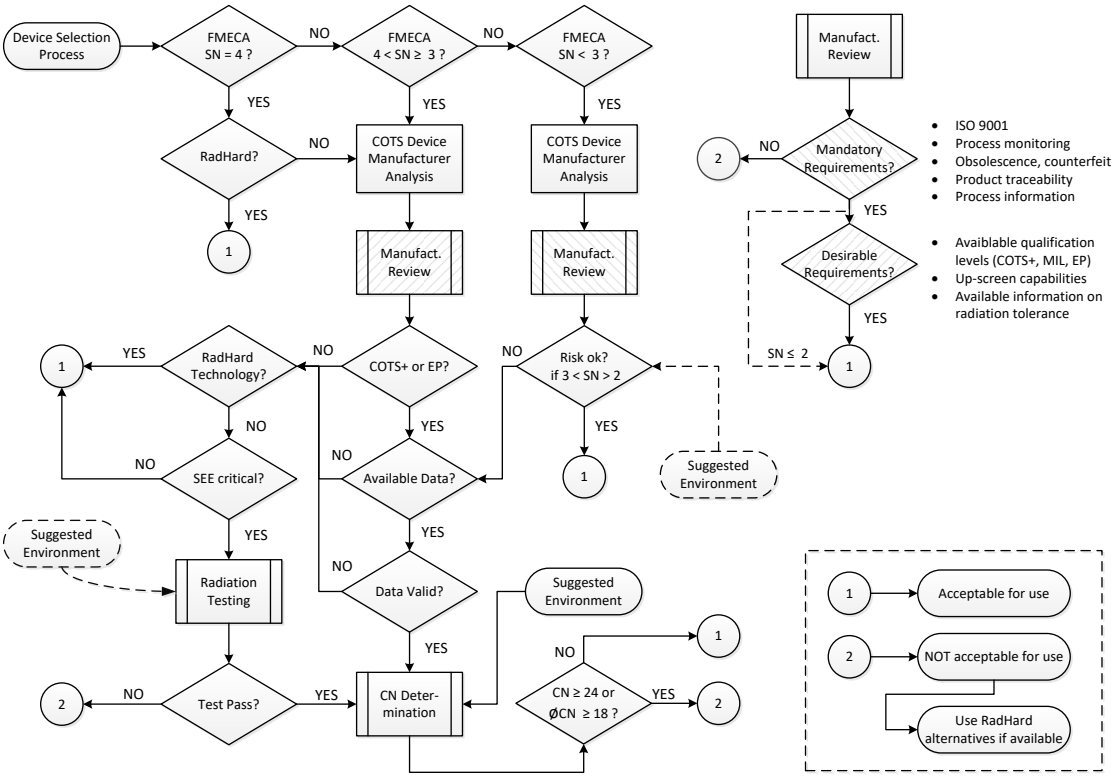


FIGURE 4.4: EEE part selection flow chart, based on FMECA test results, according to [71].

This procedure will allow a more secure selection based on analytical results of the FMECA, specifically with respect to radiation effects and their failure propagation to external systems and within the GSDR architecture. The selection approach set out here considers an early-phase definition when high qualification-level devices such as RadHard EEE parts should be used and when COTS solutions are desirable. Several stages of analysis, such as manufacturers' reviews, available data surveys and specifically radiation testing are mandatory before they are acceptable to use. Again, risk assessment and costs are important drivers. The intended selection procedure should try to find a valid balance between these factors. Risk assessment should take place in several steps

of the device selection process, such as in the manufacturers' review in cases where one or multiple requirements are not met. Other examples for specific risk assessment are in the data validation (radiation test data) e.g. when process information regarding the selected devices differs from the data that have been investigated or the depth of detail of the devices' characterization when radiation testing were applied (e.g. only TID testing).

In the selection approach set down here, it is not been considered to use the analyzed and tested devices for a later commercialization, which would require further actions such as up-screening and evaluation processes, including lot homogeneity verification and extensive testing on multiple samples as envisaged by [78, 101–103]. At this stage, the presented approach can be viewed more as a pre-evaluation of whether COTS EEE parts can be accepted for space missions, primarily with respect to radiation effects.

The selection procedure starts with a separation of the severity analysis, presented in section 4.2.1.1. The separation is categorized as follows and can be also referred to Table 4.1:

- **SN = 4**
  If one item of the FMECA severity analysis is declared as catastrophic, a RadHard device is mandatory. If the functionality is not available in the required qualification-level, the procedure for COTS evaluation has to be followed.
- **4 < SN ≥ 3**
  If the SNs are lower than four and greater than or equal to three, the use of RadHard devices is not mandatory and COTS solutions are desirable. One has then to follow the evaluation procedure as described in Figure 4.4 and in the text below. A criticality analysis for the specific device chosen is mandatory at the end of the selection process based on existing test data and the suggested environment to allow acceptance of use.
- **SN < 3**
  If the SNs are less than three, a use of COTS with the mandatory manufacturer review is acceptable as described below. In case where the SNs for the functional block differ but are less than three, a specific risk assessment is required to determine whether the potential technologies or devices are required for further investigations into radiation effects (category $4 < \mathrm{SN} \geq 3$) or if the expected effects from radiation are negligible (for instance, the technology intended to be used is less sensitive to TID effects). The risk assessment can include the suggested environment in the early phase to avoid further investigations and thereby the required CN determination.

When COTS parts are desirable in the system design, specifically if RadHard devices are not available for the desired functionality, one has to firstly follow a manufacturers' review. As described previously in section 4.2.1.3, several requirements need to be met by the manufacturer and these need to kept in mind by the system designer when using COTS EEE parts. The review is divided into two steps:

(1) mandatory requirements, and (2) desirable requirements, which are relevant for selected devices falling into the category $4 < \mathrm{SN} \geq 3$. The mandatory requirements include verification of provided product traceability, process information, and general qualification standards, pertaining to the process line as set down by the manufacturer. Especially product traceability is an important part of the review process, since one needs to know if lot information, semiconductor technology (e.g. 65 nm CMOS) and qualification procedures/standards are provided to the end-user. During the second part of the review, (2) desirable requirements, information about other, higher qualification-levels of the intended parts (e.g. automotive or military-grade) or up-screening capabilities by the manufacturer are collected. If those alternatives, such as COTS+ or EP, are available, their use should be preferred. In the next step, one has to collect information about available data, such as flight-heritage and published up-screening information about the to be selected devices, which could include burn-in tests.

Of greater interest are radiation test data. If such data are available, a validation is mandatory since semiconductor processes might have changed, manufacturing sites have moved or qualification-standards changed. If data are not available or valid for the devices, further investigations are required which primarily include radiation effects. Radiation testing is generally unavoidable, but in minor cases not required if the semiconductor technology has been proven to be radiation-tolerant [88–91]. Nevertheless, as mentioned in section 4.2.1.3, it is possible that technologies that are not sensitive to TID and DD effects might potentially be affected by SEE. Thus, it is mandatory to further investigate their robustness based on available data or to undertake specific risk assessments. Radiation testing and characterization is often complex and expensive. Thus, tailored test requirements and conditions (see section 2.2) can be applied to the suggested environment (e.g. mission orbit and time) instead of testing according to standards such as for the ECSS. Once the test has been passed successfully or the given data are valid, the device goes through a criticality analysis where the PN data derived from the test results are taken into account for specific suggested environments. The PN is taken from event rate predictions and the DN determined by proper mitigation techniques that can be applied. The tailored limits for the PN are provided in Table 4.2 and are discussed with regard to specific critical COTS devices for the desired GSDR system in section 5.3.

The CN for each expected classified error of the FMECA should not exceed 24 and an average CN should not go above 18. However, the CN thresholds can be modified to the

specific mission (quality assurance) requirements. If these criteria are met, the device intended for the functional block is acceptable for use. If the CN exceeds the limitation, a RadHard alternative is recommended or another device should be investigated. In terms of time constraints, risk assessment should be carried out to avoid long iterations, and specifically to avoid expensive testing on multiple parts. In cases of referenced test data that are approved and valid, time is not critical at this point, especially if RadHard alternative solutions are available.

For SN < 3, it is acceptable to use devices without further investigations into radiation effects. However, the recommendation and preference should be for using parts with available test data.

4.2.2 Baseband processor

The FMECA results for the BBP functional block are presented in Table 4.4. Since the BBP is a central unit of the GSDR system, one would assume that the criticality-level for such a device would be very high.

TABLE 4.4: FMECA severity analysis on the BBP functional block.

ID	Failure mode	Failure causes	Failure effects	SN
BBP.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
BBP.2	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
BBP.3	HW Failure	SHEs, non-recoverable state	permanent loss of system functionality	3
BBP.4	HW Failure	SEFIs, recoverable state	temporary loss of system functionality	2
BBP.5	SW Failure	SEU/MBU/SEFIs, OS crash	temporary loss of system functionality	2
BBP.6	SW Failure	SEU/MBU/SEFIs, SW thread/process crash	temporary loss of system-parts' functionality	1

However, considering that catastrophic is classed as failures affecting external systems such as the spacecraft, the BBP would not be that problematic if permanent damage of the devices can be prevented and functional interrupts are acceptable. Since the severity number for the BBP functional block is ≤ 3 and will not directly affect external systems, a COTS solution is considered. Expected failures are either HW- or SW-related. Critical damage and hence a permanent loss of system functionalities are SEL or high current states that can lead to a thermal destruction of the devices if not prevented. Long-term

degradations due to TID are also reasonable but often not very critical since shielding is usually applied and mission durations can be short (e.g. LEO satellite missions). However, environments with high dose rates and longer operational lifetimes may be considered and specific radiation dose analysis is required. Non-recoverable states due to stuck-bits (SHE) are possible in ASIC and FPGA implementations and could also lead to a permanent loss of system functionality. The probability of these effects is however quite low. So-called soft-errors, or SW-related failure are recoverable and only leads to a temporary loss of system functionality. These are typically based on SEU, MBU or SEFIs in the OS or specific SW applications.

As mentioned, the BBP can be implemented in a DSP, FPGA or SoC. Table 4.5 firstly shows a brief technology assessment and overview for all possible types of implementation.

TABLE 4.5: Technology assessment for potential baseband processors units.

Device	**Techno.**	**Level**	**Review**	**Complex.**	**Perform.**	**Costs**	**Data**
DSP	n.a.	All	n.a.	++	-	++	-+
ASIC	n.a.	All	n.a.	-	++	- -	n.a.
FPGA	n.a.	All	n.a.	+	-+	+	++
SoC	n.a.	All	n.a.	-+	+	+	++

ASIC designs are also possible but not desirable due to long development times and high costs. Qualification-levels are available from commercial-grade up to space-qualified devices, particularly on FPGA. DSPs are also available in different types of qualification-level, but are not recommended for the GSDR design since they perform less well and are limited by the presence of input and output pins for accessing and controlling additional electronic systems. Therefore, an FPGA would be required anyway to enhance the interface capabilities. SoCs are devices combining a processor (DSP) and an FPGA fabric and this make them an ideal technology for the GSDR purposes. Table 4.6 on the following page features a list of possible candidates for the BBP.

Based on the FMECA severity results in Table 4.4, a space-qualified solution has not been considered, nor is one as yet available for SoC technologies. FPGAs represent an alternative solution but these are not recommended due to their high costs and relatively low performance capabilities compared to commercial devices that are available in acceptable qualification-grades e.g. automotive-grade with extended temperature rates and available manufacturing and process information. Many of the presented COTS solutions in Table 4.6 have already been investigated for their performance under radiation conditions and are also used in other space missions.

TABLE 4.6: Device assessment for potential baseband processors units.

Device	Techno.	Level	Review	Complex.	Perform.	Costs	Data
Xilinx Zynq-7000	28 nm CMOS	Mil.	+	-+	-+	++	++
Xilinx Ultra-scale	16 nm FinFET	Mil.	+	-	-+	-+	+
Altera Cyclone-V	28 nm CMOS	Auto.	-+	-+	-+	++	+
Microsemi Smart-Fusion	130 nm CMOS	Mil.	+	-+	-+	++	+

The Zynq-7000 SoC from Xilinx has been chosen for the GSDR system as the BBP device since it compromises very good power-to-performance balance, it is available in different quality-grades (industrial to military/defense), detailed manufacturers' information is provided and it is broadly tested in the space and radiation community [104–107]. However, as is evident in Figure 4.4, a determination of CN is mandatory with the available data and is presented in the discussion that features in section 5.3.1.

4.2.3 Data and control interface

The data and control interface (CTRL) represent a direct electrical connection to external systems. They can therefore affect those systems and is thus related to catastrophic failures as shown in the FMECA severity results in Table 4.7 on the following page. Moreover, potential failure may result in damage to the (internal) system itself.

Any kind of degradation, whether this is long term due to TID or by transient effects (SEEs), could propagate to cause further damage to external and are thus classified with a catastrophic severity number (4). SETs could lead to invalid data transmission in both directions. These failures are less critical and mainly result into an invalid command or telemetry, which can be detected and potentially corrected with error correction codes (ECC). Besides the catastrophic failure classification, one has to consider that all those effects can lead to a permanent damage to the GSDR system and result in a continuous loss of function.

Fortunately, interface devices such as drivers or receivers for RS422 or LVDS standards are available in space-qualified options and considered in the GSDR system design. A technology assessment for potential devices on the data and control interface functional block is therefore not performed.

TABLE 4.7: FMECA severity analysis on the CTRL functional block.

ID	Failure mode	Failure causes	Failure effects	SN
CRTL.1	HW Failure	SELs or high current states	catastrophic failure affecting external systems	4
CRTL.2	HW Failure	TIDs, long-term degradation	catastrophic failure affecting external systems	4
CRTL.4	HW Failure	SETs, critical transients	catastrophic failure affecting external systems	4
CRTL.5	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
CRTL.6	HW Failure	SETs, critical transients	permanent loss of system functionality	3
CRTL.7	HW Failure	SETs, non-critical transients	corrupted data transmission/interpretation	2

4.2.4 Memory resources

The memory resources are separated into static and dynamic devices. Both types are used for different operations, such as for data storage and configuration files on static memory devices or computing resources on a random access memory (RAM) of the OS or SW applications/processes. The FMECA severity analysis results for both types memory resource are presented in Table 4.8 and Table 4.10, respectively.

Static memory device

The results for the static memory device presented in Table 4.8 show no catastrophic failure category which affects external systems (SN $\leq$ 3) and may be acceptable as a COTS solution.

TABLE 4.8: FMECA analysis on the static memory resources functional block.

ID	Failure mode	Failure causes	Failure effects	SN
MEM_S.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
MEM_S.2	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
MEM_S.3	HW Failure	SHEs, non-recoverable cell	permanent loss of system functionality	3
MEM_S.4	HW Failure	SEUs/MBUs recoverable state change	temporary loss of system functionality	2
MEM_S.5	HW Failure	SEFIs, recoverable functional interrupt	temporary loss of system functionality	3

However, static memory devices specifically serve as a critical element for the system operation since they store important configuration and boot files which could lead to a permanent non-operation scenario and thus a loss of functionality. The probability of invalid boot data by SHEs or SEUs/MBUs is relatively low, but strictly depends on the technology used and on their storage size and density. Non-recoverable information damage could occur by bad-block readings (if possible) and different partitions can be used as backup (if sufficient storage size is provided). SEUs and MBUs could be detected and recovered, e.g. by applied ECCs and continuous verification/scrubbing.

One has to carefully consider what technology can be used and what qualification-levels are available. The technology assessment for static memory devices is therefore presented in Table 4.9.

TABLE 4.9: Technology assessment for potential static memory devices.

Device	**Techno.**	**Level**	**Review**	**Complex.**	**Perform.**	**Costs**	**Data**
MRAM	130-180 nm CMOS	Space	+	+	- -	-	++
NOR Flash	90-250 nm CMOS	Auto.	n.a.	-	-	+	-+
NAND Flash	16-50 nm CMOS	Auto.	n.a.	-+	++	++	++
3D-Plus NAND Flash	50 nm CMOS	Space	++	-+	++	-	n.a.

Magnetoresistive random-access memory (MRAM) devices are inherently immune to radiation-induced SEUs or SEFIs. However, the control circuitry surrounding the memory array is based on a CMOS process and thus could be susceptible to radiation and could result in SELs as investigated in [108, 109]. Moreover, the memory density of MRAM is very limited and not suitable for the GSDR system. NOR flashes are also limited in their memory density compared to NAND flashes and and have been less investigated with respect to radiation effects. The investigations of [110, 111] show that NOR flashes are inherently more sensitive to radiation-induced leakage current and fail at much lower TID levels than do NAND flashes. Thus, the NAND flash technology is the most promising candidate since they have the required density to store important data and is also supported by the Zynq-7000 BBP. NAND flashes have been investigated in deeper detail under radiation conditions as presented in [112–115]. RadHard solutions are not available but radiation-tolerant devices are provided by third parties, which use up-screened and radiation-tested dies developed by commercial manufacturers

[116]. These may be considered as alternative solutions if the intended commercial parts do not meet the suggested environmental requirements or if further testing is required.

Dynamic memory device

The GSDR requires a DDR3-SDRAM device for dynamic data processing. For DDR-SDRAM devices, no RadHard options are available. However, there have been a set of studies on these kinds of device with respect to their behavior under radiation conditions published in [117–119] which can be used for the device selection process. Possible failures are presented in Table 4.10.

TABLE 4.10: FMECA severity analysis on the dynamic memory resources functional block.

ID	Failure mode	Failure causes	Failure effects	SN
$MEM_D.1$	HW Failure	SELs or high current states	permanent loss of system functionality	3
$MEM_D.2$	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
$MEM_D.3$	HW Failure	SHEs, non-recoverable cell	permanent loss of system functionality	3
$MEM_D.4$	HW Failure	SEUs/MBUs recoverable state change	temporary loss of system functionality	2
$MEM_D.5$	HW Failure	SEFIs, recoverable functional interrupt	temporary loss of system functionality	2

The severity results show no catastrophic SN but several potential examples of permanent loss of system functionality are possible. These relate to long-term degradation and destructive SEEs, commonly SELs or high current states. SHEs are possible but due to the required high density of data storage more or less negligible, since the OS accesses the DDR3-SDRAM and can carry non-operational cells to avoid their occurrence. Soft errors due to SEUs/MBUs are also not of concern, since they are not expected to appear in higher numbers that would exceed the required memory resources compared to the total amount of storage capacity and ECCs that can be applied. SEFIs in the control logic that may lead to a full functional interruption are more critical but are expected to occur much less often than SEUs/MBUs. However, SEFIs are recoverable in this model.

A device assessment for the required DDR3-SDRAM is provided in Table 4.11 on the following page. The radiation-tolerant solutions of 3DPLUS for the NAND flash and the DDR3-SDRAM [120] are considered for the GSDR system design, but these are not necessarily mandatory if process information and product traceability are provided by the commercial manufacturer of the desired memory devices. Radiation effects that are evaluated and expected in the selected NAND flash devices are presented in section 5.1.2, as well as in section 5.1.3 for the DDR3-SDRAM, respectively.

TABLE 4.11: Device assessment for potential dynamic memory devices.

Device	Techno.	Level	Review	Complex.	Perform.	Costs	Data
DDR3	10s nm CMOS	Auto.	+	-+	+	++	+
Rad.-Tol. DDR3	10s nm CMOS	Space	++	-+	+	- -	n.a.
DDR3-MRAM	10s nm CMOS	Auto.	+	-	-+	-	- -

DDR3-MRAM technologies are still under investigation and development, thus they are at this stage only potential candidates for future revisions of the GSDR. Both the dynamic and static memory devices that are intended to be used require a criticality determination based on the referenced radiation test results. These determinations are presented in section 5.3.2 and section 5.3.3.

4.2.5 Power regulation

The FMECA severity analysis results for the power regulation functional block are presented in Table 4.12. Similar to the data interface and control unit, the power regulation could affect external systems directly and is therefore related to instances of failure propagation classed as catastrophic.

TABLE 4.12: FMECA severity analysis on the power regulation functional block.

ID	Failure mode	Failure causes	Failure effects	SN
PWR.1	HW Failure	SELs or high current states	catastrophic failure affecting external systems	4
PWR.2	HW Failure	TIDs, long-term degradation	catastrophic failure affecting external systems	4
PWR.3	HW Failure	SETs, critical transients	catastrophic failure affecting external systems	4
PWR.4	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
PWR.5	HW Failure	SETs, critical transients	permanent loss of system functionality	3
PWR.6	HW Failure	SETs, non-critical transients	corrupted data transmission/interpretation	2

A mitigation or reduction of possible catastrophic failures could be implemented with a dedicated central power input device such as galvanic isolated DCDC converter which is then selected RadHard. However, system-internal failure propagation, e.g. by critical

SETs that cannot be filtered of the power regulator or by degradation of the output voltage by TID could lead to a serious damage to the powered devices in the GSDR system. Thus, all power devices should be taken RadHard and no further determination is required.

4.2.6 RFIC

Highly integrated RFICs as mandatory for the GSDR system design are rare on market and are still relatively new. There are hence few choices for selecting proper devices for this functional block. Moreover, RadHard solutions are normally not available since they are usually designed for terrestrial applications, specifically for mobile services. However, this key technology plays an essential role and is fortunately not associated with catastrophic failures, as evidenced by the severity analysis presented in Table 4.13.

TABLE 4.13: FMECA severity analysis on the RFIC functional block.

ID	Failure mode	Failure causes	Failure effects	SN
RFIC.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
RFIC.2	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
RFIC.3	HW Failure	SHEs, non-recoverable state	permanent loss of system functionality	3
RFIC.4	HW Failure	SEFIs, recoverable state	temporary loss of system functionality	2
RFIC.5	HW Failure	SEUs/MBUs/SEFIs, invalid data	corrupted data for transmission or reception	2
RFIC.6	HW Failure	SETs, invalid data	corrupted data for transmission or reception	2

Besides potentially destructive damages that could lead to a permanent loss of system functionality (TID or destructive SEEs) soft errors that cause temporary loss of system functionality or corruptions in data are more likely to occur. RFICs are usually highly integrated circuits with complex structures and numerous functionalities that can be controlled. State-machines and configuration registers being used are susceptible to SEEs leading to a functional interruption (SEFI) or invalid data transmission/reception. Short-term (transient) data corruption that can affect single bits or even bit sequences is also possible. SETs may occur in different stages, whether on the RF data or on the digitized samples.

Since RFIC devices are new there have been no investigations done so far in terms of radiation effects. Thus, the author's own characterizations are essential if following the

device selection approach set out in Figure 4.4. Only two potential candidates have been found for the RFIC (shown in Table 4.14) that allow programmable RF tuning and which integrates ADC and DAC. Both manufacturers, Analog Devices and Lime Microsystems, use a 65 nm CMOS process for their RFIC and both devices have similar features. However, the LMS7002M [121] only supports a frequency range from 100 kHz to 3.8 GHz whereas the AD936X supports up to 6 GHz. Due to the available product and process information of Analog Devices (e.g. lot/date code, change notification, single fabrication site) and its device's performance, the AD9361 has been selected for the RFIC in the GSDR system design.

TABLE 4.14: Device assessment for potential RFIC devices.

Device	Techno.	Level	Review	Complex.	Perform.	Costs	Data
AD936X	65 nm CMOS	Indust.	+	-	++	-+	-
LMS7002M	65 nm CMOS	Indust.	-	-	+	+	- -

Specifically for the AD9361 [122], dedicated radiation tests are considered and are an important aspect of this PhD thesis. These investigations are discussed in detail in section 5.2. The presented radiation test results are taken as input for the required CN determination and are outlined in section 5.3.4.

4.2.7 Clock generation

The FMECA severity results for the clock generation functional block are shown in Table 4.15. This functional block is not responsible for any catastrophic failure to external systems. However, expected degradation could lead to functional failures and further degradation of the systems.

TABLE 4.15: FMECA severity analysis on the clock generation functional block.

ID	Failure mode	Failure causes	Failure effects	SN
CLK.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
CLK.2	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
CLK.3	HW Failure	SEFIs, recoverable state	temporary loss of system functionality	2

Clocking is required for different parts of the GSDR, such as for the BBP and RFIC. Clocking sources are usually to be defined as temperature-stable and should hold their output specification over a long period. The experiences of radiation effects on crystal

oscillators are quite rare and only a few researches relevant to this issue are available [123–126]. Two acknowledged issues around crystal-based oscillators are an accumulated (TID) degradation of stability and a drift of the oscillator frequency [125, 126]. Radiation tests have shown that oscillators may withstand very high doses for space ($\geq$1 Mrad(SiO_2)) with a relatively low degradation. Transient effects causing a destructive damage are not known. Some studies have mentioned that pulsed radiation effects may cause a loss of oscillation which is recoverable by power-cycling the device [123, 124]. Based on the expected effects and their potential failures due to radiation, a space-qualification is not mandatory but at least an automotive-grade level should be considered.

Devices that require a clock signal, such as the BBP or RFIC, allow a broad range of input frequency and can be re-calibrated or tuned to the radiation-induced offset oscillator frequency if required. However, since a significant frequency drift is not expected at a dose level of several 10s to 100s krad(SiO_2) and most near-Earth mission will not achieve those values in their lifetime, such effects are of minor concern. Oscillators are available in different types and qualification-level. Based on the requirements of the previously selected devices for the BBP and RFIC, three technologies are desirable: (1) temperature controlled crystal oscillator (TCXO), (2) voltage controlled crystal oscillator (VCXO) and (3) oven controlled crystal oscillator (OCXO), as shown in Table 4.16.

TABLE 4.16: Technology assessment for potential oscillator devices.

Device	**Techno.**	**Level**	**Review**	**Complex.**	**Perform.**	**Costs**	**Data**
TCXO	n.a.	All	n.a.	+	+	++	-
VCXO	n.a.	All	n.a.	-+	-	+	-
OCXO	n.a.	All	n.a.	-	-+	- -	-

The most important features of the desired oscillator technology are the frequency stability, jitter and phase-noise performance. VCXOs are generally less stable compared to TCXO and OCXO. The best stability is provided by OCXOs but they require a stable environmental temperature and are thus not recommended for the GSDR application. However, the power consumption of the latter is relatively high. TCXOs are highly stable over a broad range of temperatures and are thus the best technology for the BBP and RFIC. Due to the fact that the severity number is fairly low (2 to 3) and that it is known furthermore that specifically TID is not so critical, a criticality determination has not been made and the TCXO selected has not been further investigated or tested. However, at least an automotive-grade device is desirable for satisfying the required manufacturing review.

Since two AD9361s are used for the RFIC functional block, a clock-buffer is also required for the TCXO signal distribution. For such components, RadHard and space-qualified

devices are available but these often fail to meet the performance required for the AD9361 in terms of signal type (low-voltage CMOS), jitter or phase noise. Expected failures of such devices are listed in Table 4.17.

TABLE 4.17: FMECA severity analysis on the clock generation functional block.

ID	Failure mode	Failure causes	Failure effects	SN
BUFF.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
BUFF.2	HW Failure	TIDs, long-term degradation	permanent loss of system functionality	3
BUFF.3	HW Failure	SEFIs, recoverable state	temporary loss of system functionality	2

Critical failures can be SELs and high current states leading to a destructive effect on the devices. Furthermore, TID may lead to a degradation of the device's performance (e.g. noise enhancement or extended jitter) and finally to a total loss of function if the exposed radiation exceed the limits. Minor publications referring to radiation test results are available for such devices. However, test data in [127] have shown a very robust response in terms of neutron-induced SEEs and TID. Vendors offer radiation-tolerant and RadHard solutions, but with limited performance compared to COTS devices.

TABLE 4.18: Device assessment for potential clock generation devices.

Device	Techno.	Level	Review	Complex.	Perform.	Costs	Data
CDCLVC-1310	BiCMOS	Indust.	-+	-+	++	++	-+
ADCLK-846	180 nm CMOS	Indust.	+	-+	-+	+	++
CDCLVP-111	BiCMOS	Indust.	-+	-+	-+	+	++
CDCLVP-111-SP	BiCMOS	Space	++	-	-	- -	n.a.

Table 4.18 shows the device assessment for potential clock generation and distribution devices. For the clock-buffer device, a non-space-qualified solution is desired and additional investigations specifically with respect to radiation effects have been considered during the GSDR system development to establish the best RF performances for the RFIC. Further investigations have been undertaken for the CDCLVC1310, which has already been evaluated by [127]. In cases where the selected devices fails under radiation or the performances degrades heavily, a fallback option to a radiation-hardened solution has been implemented in the system design by a dual-footprint on the printed circuit board (PCB).

The selected device has been recently tested under proton irradiation and γ-rays and results confirm their robustness for TID and SEEs. Such results are not, however, within the scope of this thesis but are intended to be published soon. A further determination of criticality is mandatory.

4.2.8 Supervising circuit

The supervising circuit is a critical functional block in the GSDR system, since it should mitigate radiation effects within the system on the hardware-level by detecting functional interrupts and should prevent destructive damages, for example by sub-voltage SELs that can not be detected by the primary power input. A detailed description of the implemented supervising circuit is presented in chapter 6, but to identify the severity and criticality of all devices within that functional block, the main devices are listed below:

- HW-watchdog (HW-WD)
- Timer (TIM)
- Power switches (PWR-SWT)
- Current and voltage sensing (CVS)

Logically, it is mandatory to ensure that the devices representing the supervising circuit will not fail under radiation. Thus, even if those devices do not cause a catastrophic-related failure according to the results of the severity analysis presented in Table 4.19 to Table 4.22, they should be used RadHard or at least need to be radiation-tolerant.

TABLE 4.19: FMECA severity analysis on the supervising functional block - watchdog.

ID	Failure mode	Failure causes	Failure effects	SN
HW-WD.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
HW-WD.2	HW Failure	TID, long-term degradation	permanent loss of system functionality	3
HW-WD.3	HW Failure	SHEs, non-recoverable state	permanent loss of system functionality	3
HW-WD.4	HW Failure	SETs, short functional interrupt	temporary loss of system functionality	2
HW-WD.5	HW Failure	SEFIs, recoverable state	temporary loss of system functionality	3

The HW-WD (FMECA severity analysis in Table 4.19 on the previous page) supervises the core voltage of the BBP and requires a continuous pulse (heart-beat) signal that verifies the functional operation of the OS or SW application of the GSDR. Destructive events such as SELs or TID-related degradation could lead to a malfunction of the device resulting to a permanent loss of the system functionality. An instance of an SHE on the watchdog, for example on the reset output or on the heart-beat input, could cause a stuck fault state and thus a permanent loss of the system functionality. Short-term fault states by SETs or SEFIs are of minor concern since they are recoverable and not expected to occur very frequently. Even though if a severity would allow the use of (verified) COTS devices, a RadHard solution is preferred due to the supervising circuit is a critical block that should reliably monitor and control the system.

To allow a self-shutdown and thus prevent a destructive event within the GSDR system, a power MOSFET is integrated in the input power stage and operated as a power switch. Once an event is detected (e.g. by the HW-WD), the MOSFET is ordered to shut down the power supply. Table 4.20 gives the FMECA results for the power switch unit.

TABLE 4.20: FMECA severity analysis on the supervising functional block - switch.

ID	Failure mode	Failure causes	Failure effects	SN
PWR-SWT.1	HW Failure	SEBs	catastrophic failure affecting external systems	4
PWR-SWT.2	HW Failure	SEGRs	catastrophic failure affecting external systems	4
PWR-SWT.3	HW Failure	TID, long-term degradation	catastrophic failure affecting external systems	4
PWR-SWT.4	HW Failure	TID, long-term degradation	permanent loss of system functionality	3

Since the MOSFETs are directly interfacing with external systems and potentially destructive events are SEB and SEGR, they could lead to a catastrophic failure. TID effects could either lead to an incorrect shutdown causing a permanent loss of system functionality or even to a catastrophic case affecting or damaging external systems. Thus, a space-qualified or RadHard solution is mandatory.

The FMECA severity analysis for the timer is presented in Table 4.21 on the following page. The timer is responsible to re-enable the power supply once it has been shut down by a protection mechanism (e.g. HW-WD). The timer initially holds the power switches in an off-state and will release them after a certain time period. Potential failures could be destructive events that cause a permanent loss of the timer and thus a non-functional recovery process of the GSDR. Long-term degradation could cause a longer (or shorter) shut down period that could extend to a critical state and lead to a permanent loss of system functionality.

TABLE 4.21: FMECA severity analysis on the supervising functional block - timer.

ID	Failure mode	Failure causes	Failure effects	SN
TIM.1	HW Failure	SELs or high current states	permanent loss of system functionality	3
TIM.2	HW Failure	TID, long-term degradation	permanent loss of system functionality	3
TIM.3	HW Failure	TID, long-term degradation	temporary loss of system functionality	2

As for the watchdog, a RadHard solution is currently preferred due to the supervising approach of the system.

Sub-voltage and sub-current sensing is implemented to detect uncertainties within the system that probably can not be observed on the primary input. These could include micro-latchups on specific devices that usually have a very small power consumption but are still potentially sensitive to SELs. Many devices are furthermore very sensitive to supplied voltage variations, hence voltage supervising is recommended. Table 4.22 shows the FMECA severity results for the current and voltage sensing (CVS) functionality.

TABLE 4.22: FMECA severity analysis on the supervising functional block - CVS.

ID	Failure mode	Failure causes	Failure effects	SN
CVS.1	HW/SW Failure	SEU/MBU/SEFIs, wrong voltage or current value	temporary loss of system functionality	2
CVS.2	HW Failure	TID, long-term degradation	temporary loss of system functionality	2
CVS.3	HW Failure	TID, long-term degradation	permanent loss of system functionality	3

The implementation of the CVS is done by high-precision shunt resistors that generate a voltage drop-off which is then amplified with a current-sensing amplifier. The voltage is captured by the BBP Zynq ADC and evaluated by means of a software process. In case of an increase in the current, the software releases the power switch to perform a system reset. Sub-voltages are also monitored by the BBP in the same manner as for current sensing. In this case, multiple failures can occur causing temporary loss of system functionality, either by SEU/MBU/SEFI within the Zynq device and by SW malfunctions. Long-term degradations by TID, e.g. in the current sense amplifier gain could potentially cause a permanent loss of system functionality but are not expected even on longer mission durations.

More likely are deviations in the gain, which can be mitigated by adjusting the current-sensing tolerances in the evaluation software. Due to the fact that SNs are low and that

the ADC of the selected Zynq-7000 has been investigated, as has the performance of the current-sensing amplifiers, further device investigations are unnecessary. Drifts by the current-sensing amplifiers and the resulting current values can be compensated for by software modification which reduces the probability of long-term degradations by TID.

Since the ADC of the COTS Zynq-7000 is used to evaluate the voltage-drop of the amplified shunt resistors and due to the fact that the analyzed severity is relatively low, it is decided to choose the current-sensing amplifiers also in automotive-grade (AEC-Q100). However, up-screening in terms of RHA is currently under consideration (risk assessment).

A further description of the supervising functional design and its implementation follows in section 6.1 of chapter 6.

4.3 Summary

This chapter has given a detailed overview of the system design description of GSDR and its development methodology was presented. As the primary intention is to design a cost-efficient system with a novel approach to supporting multiple-frequency bands, the use of COTS devices is unavoidable. However, since the design should be operated reliably in space applications, a significant phase of the design process is to evaluate the criticality of the entire system. In order to do so, individually functional blocks have been categorized, e.g. baseband processor or power regulation. A radiation-specific FMECA has been performed to identify either the mandatory need for RadHard EEE parts or to ascertain whether COTS devices are suitable to use. The part selection process for each functional block follows the results of the FMECA severity analysis, and technology and/or device assessment has been carried out to decide which COTS part or technology is preferred to be used. From system point of view, a hybrid system design using RadHard and well investigated COTS devices represents the most effective solution. System-critical devices such as the Zynq, NAND-flash, DDR3-SDRAM or the AD9361 as RFIC that are preferred for use in a COTS solution are discussed in more detail in chapter 5. The criticality of system-relevant COTS devices, based on their evaluated radiation effects, has to be finally determined to ultimately decide whether they are acceptable for use in a certain environment (e.g. LEO or GEO) or not.

The presented unique selection process for the use of COTS parts in space systems, as well as the novel design approach of the GSDR, have been previously published by the author of this thesis in shorter versions in [71, 128, 129].

Chapter 5

Radiation effects on system-critical COTS devices

Based on the FMECA severity analysis and the technology and device assessment of the GSDR system design (section 4.2), multiple functional blocks will be implemented in a COTS solution. In this chapter, the critical COTS devices being used are presented and discussed based on recent experimental results with respect to radiation effects that either have been published or where the author's own analysis were mandatory. An overview of system-critical COTS devices is introduced in section 5.1. Devices that have been chosen for the GSDR system design are presented in the light of more detailed information on radiation effects. Section 5.2 then sets out the detailed investigation on radiation effects of the selected RFIC device. The author's own analysis was required for this device since no data have been published at this point and the device is responsible for the major intended functionality of the GSDR system. Finally, the criticality determination based on the FMECA approach is performed and discussed in section 5.3.

5.1 System-critical COTS devices

COTS devices that represent the core electronics of the GSDR are the baseband processor, volatile and non-volatile memory resources and the RFIC devices. As already mentioned in the technology and devices assessment section (section 4.2), especially the favored NAND flash technology and the DDR3-SDRAM have been intensively tested under radiation and are used in many space missions. New technologies such as the SoC are very promising due to their combination of DSP and FPGA, the resulting benefits of small integrated form-factors and an excellent balance of power consumption and performance. In recent years, especially the Xilinx SoC product family Zynq-7000 have been

broadly tested and investigated for their performance under radiation. RFIC technologies are on the other hand not well established in space applications nor have been deeply investigated for radiation effects. Since these devices allow much better performance and more flexibility they would massively impact future radio systems specifically to space applications. Due to the missing information for radiation effects on such devices, they need to be tested under different radiation conditions to ensure a reliable operation.

The following sections lay out important information about radiation test results, based on numerous publications and test reports. This is especially applicable for the chosen Zynq-7000 as BBP and the NAND flash for non-volatile memory resources as well as for the DDR3-SDRAM that are used for supporting volatile memory storage. Known issues with those devices are described to enable insights to be gained into possible failure propagation and the devices' influence on overall system performance.

The radiation test results of the AD9361 as RFIC will take up a substantial part of this chapter because of its high complexity and since it has never been tested before. The radiation test requirements and conditions, procedures and results are presented in section 5.2.

5.1.1 Zynq-7000

An architectural overview of the Zynq-7000 SoC is presented in Figure 5.1.

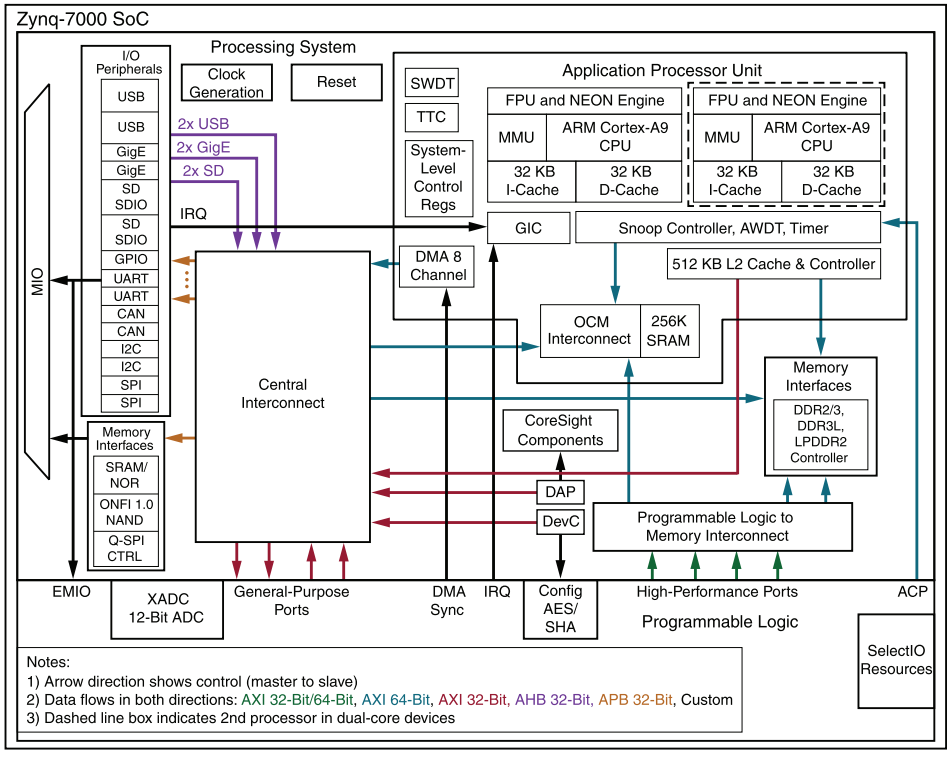


FIGURE 5.1: Architectural overview of the Zynq-7000 SoC [130].

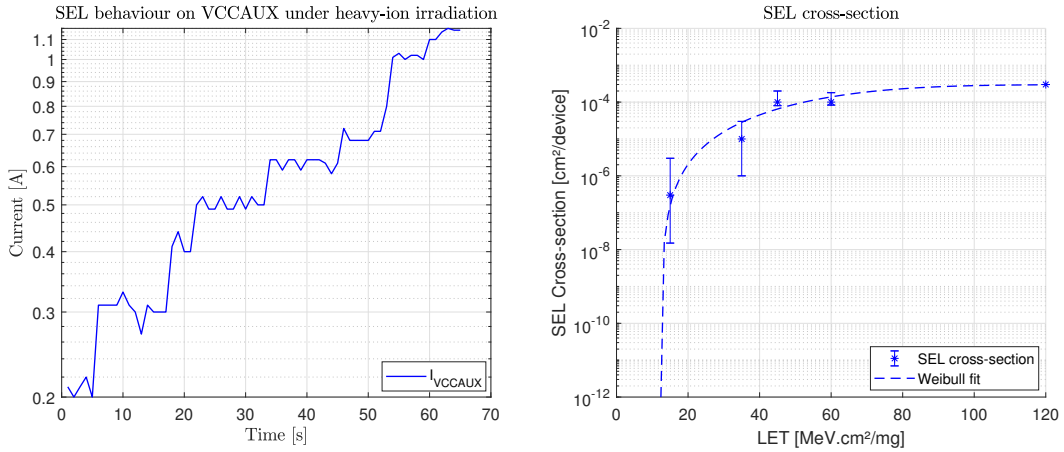
The SoC fabricated on a high-κ metal gate CMOS process with a 28 nm technology node from Taiwan semiconductor manufacturing company (TSMC). The desired component is the XC7Z020-CLG484. The Zynq-7020 integrates a programmable system (PS) using an ARM®-based dual core processor and a programmable logic (PL) with a 28 nm Artix®-7 FPGA fabric [130]. The PL is ideal for implementing high-speed logic, arithmetic and data flow processing units, while the PS supports OS implementation and the execution of software routines. Thus, the overall functionality can be appropriately partitioned between hardware and software. The PS includes a dual-core 32-bit ARM Cortex-A9 processor and two caches: (1) 32 KB L1 instruction (L1i) and data (L1d) caches per core, and (2) 512 KB L2 cache shared between both cores. A 256 KB synchronous random-access memory (SRAM)-based on-chip memory (OCM) is implemented to share data among the processor cores and the PL. External memory interfaces for DDR SDRAM and several other peripherals (e.g. universal serial bus (USB), universal asynchronous receiver-transmitter (UART) or Ethernet) are provided.

The PL block is based on the Xilinx 7-Series FPGAs (for the XC7Z020-CLG484, a 28 nm Artix®-7 FPGA fabric is used) and has 85 K logic cells, 53,200 look-up tables (LUT), 106,400 flip-flops (FF) and 220 programmable DSP slices [130]. The PL memory is separated into two groups, configuration logic bits (CRAM) and embedded block RAM (BRAM).

The communication between the PS and the PL can be implemented through OCM but also through the cache L2 or the BRAM. The type of communication can positively affect the system's reliability, execution time and power consumption [131]. With respect to radiation effects, specifically SEEs, the PS and PL may show different responses (cross-sections) and failures. SEUs in the CRAM or BRAM of the PL has a sustainable effect and reconfiguration of the programmable logic is required to correct them. Furthermore, these devices are expected to be sensitive to SETs where current pulses are randomly injected into the circuit. The PS is also expected to have a a high sensitivity to SEEs, especially due to its memories, the L1 and L2 caches or the OCM that will be affected by SEUs.

Recent publications of [105–107, 132, 133] have demonstrated the performance of the Zynq-7000 under different radiation conditions from TID effects up to proton and heavy-ion irradiation to investigate the SEE response. These studies thereby mainly show the same behavior but although different test conditions and test procedures were applied. The most information that these studies provide is that no destructive events causing a permanent damage of the Zynq-7020 have been shown. However, SELs have been observed on the auxiliary voltage supply (VCCAUX), as illustrated in Figure 5.2 on the following page [105]. Similar effects were investigated by the Kintex®-7 FPGA fabric that is used in the higher-class SoC of the Zynq-7000 series (ZC7030 to ZC7100) [104, 134]. These SELs appear in current steps (approx. 125 mA) depending on the

particle flux and without any observable changes in functionality. The investigations of [104, 105, 134] showed a relatively slow increasing of the current (seconds) and the LET threshold of SELs is approx. $15\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$.

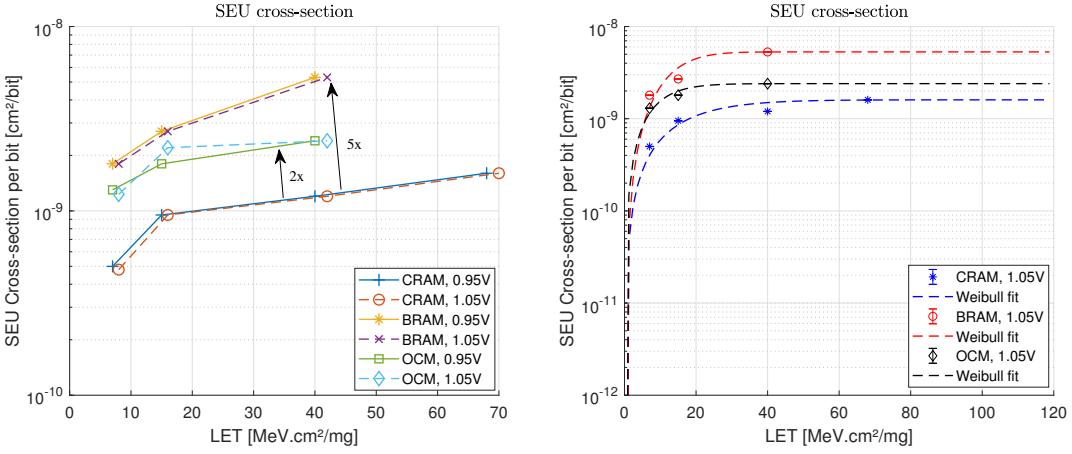


(a) SEL event (b) SEL cross-section

FIGURE 5.2: SEL / current step phenomena in (a) and the corresponding cross-section in (b) of the Zynq-7020 (W=20.00, S=1.00) FPGA under heavy-ion irradiation, according to [104, 105].

The saturation cross-section is about $3.0 \times 10^{-4}\,\mathrm{cm}^2$/device according to [104]. Power cycling is required to recover from this event and to prevent destructive damage of the device. The SEL event rate was observed to increase at higher temperatures.

In terms of the SEU evolution of the memories, static and dynamic testes were applied. In [106, 131, 132], the static test was performed for the lowest (0.95 V) and highest (1.05 V) supply voltage rating for the core.



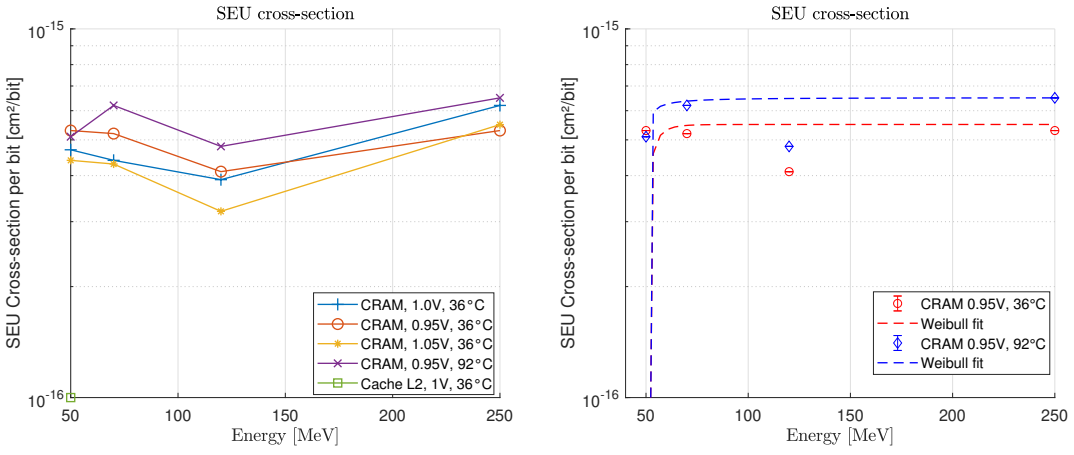
(a) SEU cross-section (b) SEU cross-section with Weibull fitting

FIGURE 5.3: SEU cross-section per bit for the CRAM, OCM and BRAM under heavy-ion irradiation (BRAM: W=14.11, S=1.77; CRAM: W=18.42, S=1.28; OCM: W=9.72, S=1.32), according to [105, 131].

The test procedures for BRAM, OCM and the Cache L2 were programmed to these memories with a known pattern ($AAAAAAAA_{hex}$) prior to irradiation and to validate and compare the content after irradiation. The configuration memory of the PL (CRAM) was configured with a bitstream consisting only of zero patterns (0_{bin}).

The work of [131, 132] has demonstrated that the CRAM cross-section and OCM cross-section differ by a factor of two. The BRAM cross-section is five times higher than the CRAM cross-section, as illustrated in Figure 5.3 that shows the cross-section of CRAM, OCM and BRAM under heavy-ion irradiation. Voltage dependencies of the cross-section have not been observed. Similar cross-section results have been observed in the work of [105] where slightly different static test conditions have been applied (different test pattern programmed and compared), as well as for the BRAM cross-section of the Kintex®-7FPGA fabric according to [104].

Proton (static) tests were also applied specifically for the CRAM, as presented in Figure 5.4. Supply voltage dependencies were not observed during proton irradiation. With increased temperature (92 °C) a cross-section variation of about 20 % at 250 MeV with 0.95 V supply voltage was noted. In the studies of [105, 131], it has been found that an average 20 SEUs in the CRAM are necessary before a SEFI can be observed in the design output (depending on the logic density and logic masking). Thus, soft-error mitigation mechanisms on the CRAM that could detect and correct single bit-flips on-the-fly may prevent functional interruption and further failure propagation.



(a) SEU cross-section

(b) SEU cross-section with Weibull fitting

FIGURE 5.4: SEU cross-section per bit for the CRAM under proton irradiation at different temperature and supply conditions (W=20.31 S=2.18), according to [132].

Dynamic tests are conducted especially to evaluate the response of the processor (PS) to radiation. The investigations of [106] are intriguing since they evaluated the processing performance in different configurations with respect to enabled and disabled caches. The application running in the core of the ARM Cortex-A9 processor is a sequence

of multiple matrix multiplications. Depending on the enabled caches the execution time was evaluated which is significantly improved by enabling all caches (92 % faster). Two types of failure were evaluated during irradiation: (1) errors within the results of the multiplication sequence, and (2) interrupts of the application sequence (SEFI). The test results presented in [106] were obtained at an LET of $4.5\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$ and an average flux of approx. 584,000 particles per cm^2/s. The highest cross-section for errors in the multiplication results is $1.54\times10^{-12}\,\mathrm{cm}^2/\mathrm{bit}$ enabling all caches. Disabling all caches results in a cross-section of $9.5\times10^{-15}\,\mathrm{cm}^2/\mathrm{bit}$. The SEFI cross-section is about $8.25\times10^{-13}\,\mathrm{cm}^2/\mathrm{bit}$ with all caches enabled but only a magnitude smaller if all caches are disabled ($2.85\times10^{-13}\,\mathrm{cm}^2/\mathrm{bit}$). It has been found that especially the cache L2 causes a high number of errors and seems to be very susceptible for SEUs. This phenomenon has also been observed in [135] where the Zynq-7020 was exposed to neutron irradiation. In this study, the Zynq-7000 was running an embedded Linux OS and hundreds of errors were reported by the Linux kernel. Analysis of these log-files verified that about 75 % of the system crashes were originated by the L2 cache. Disabling this cache improved the error rate by a factor of 160 [131].

Another more practical and complex dynamic test has been carried out under proton irradiation and was published by Hiemstra et al. [107]. In this work, a Sobel video processing algorithm was executed on an embedded Linux OS. The data being processed by the Sobel algorithms were supplied by an HDMI interface to the board and the resulting image was then provided by way of a second HDMI video interface to a monitor. The test was performed at a proton energy of 105 MeV and the main objective was to evaluate either both the processing interferences of the application and full system crashes of the Linux OS. The cross-section results are $5.70\times10^{-9}\,\mathrm{cm}^2/\mathrm{processor}$ for the Sobel video processing algorithm and $6.61\times10^{-9}\,\mathrm{cm}^2/\mathrm{processor}$ for the Linux OS crashes.

5.1.2 NAND flash

Non-volatile memory is required by the GSDR either to support a boot device which holds system-relevant configuration files' software modules and parameters and to provide an (intermediate) storage medium for received data. Based on the FMECA severity analysis presented in section 4.2.1.4 and in Table 4.9, the NAND flash technology has been selected since it provides the best performance in terms of storage capacity, costs and data availability. In this section, radiation effects that have been investigated by [112–115, 136, 137] are presented to further understand their effect on the GSDR system design. Unfortunately, not all NAND flash devices were able to be used, since the Zynq requires specific compatibilities, especially if ECC is to be used [138].

The particular device selected is the Micron 8 Gb (MT29F8G08AAAWP) NAND Flash memory, based on a 50 nm CMOS technology. The device uses a floating gate NAND cell, providing a standard interface for pin and functional drop-in compatibility, and comes in a 48-pin TSOP package. The NAND flash is organized in 1Gx8 (bit) with a block size of 256Kx8 and 64 pages per block. Each page is able to store one 8-bit word per column, with a total number of 4096 columns per page. Due to 128 redundant columns, the total page size is 4224x8 [115]. NAND flashes usually have minor bad blocks which can be screened-off. The company Micron specify that no more than 80 of the 4096 blocks are bad. Micron qualifies their automotive-grade NAND flashes according the AEC-Q100 which fulfill the manufacturing review requirements (Figure 4.4).

Four main contributions are taken as a reference with respect to radiation effect investigations of the MT29F8G08AAAWP that have been published by Grürmann et al. and Oldham et al. [114, 115, 136, 137]. In the following, the radiation effects on the Micron NAND flash are separated into TID and SEEs:

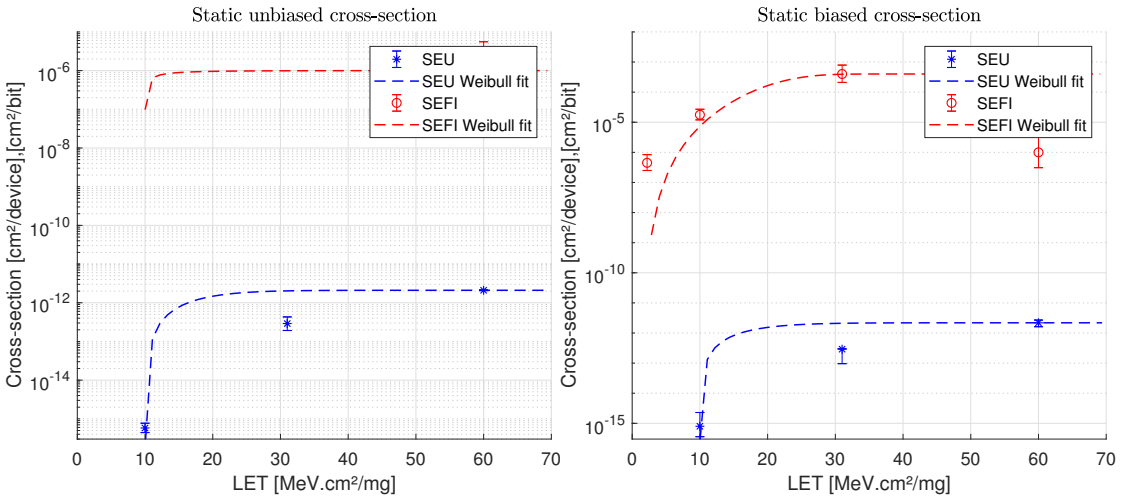
Total ionizing dose

In [115], Oldham et al., tested five samples of the 8 Gbit Micron NAND flash memory under biased conditions up to a TID level of 75 krad(SiO_2). The samples were configured with a known checkerboard pattern (AA_{hex}) during exposures, but not dynamically operated (read, write, erase). Read, write and erase operations were performed at different TID levels. For all devices under test (DUT), no errors were observed at any dose level up to 50 krad(SiO_2). At 50 krad(SiO_2), all tested samples showed a few zero-to-one errors (3 to 12) in the initial checkerboard pattern (AA_{hex}). Erase and re-program operations were successful which indicates that the devices are still fully functional. At 75 krad(SiO_2), all samples showed functional failures where the erase operation did not perform as expected. The numbers of bad words significantly increased (up to 144,561). Furthermore, the write-function resulted in a large number of errors so it can be assumed that the erase and write function suffered from the device's exposure to radiation. Nevertheless, 50 krad(SiO_2) is quite a high dose level considering that, for a typical LEO mission, doses lot lower than 50 krad(SiO_2) (inside the spacecraft) will be achieved.

Single event effects

An SEE characterization has also been performed for the selected MT29F8G08AAAWP and was published and discussed in [114, 136, 137]. In [114] by Oldham et al., heavy-ion testing was performed on four samples of the MT29F8G08AAAWP up to an LET of 58.8 MeV $\cdot$ cm^2/mg. The DUT was exposed under different operational scenarios, including static and dynamic tests in biased and unbiased condition. The use of ECC was not considered in these studies. In static test sequences, the DUTs were programmed to a known checkerboard pattern (AA_{hex}) and read out after irradiation to verify the device cross-section per bit (SEU). Under non-biased condition, SEUs were noticed on

every particle shot down to the lowest LET tested ($2.2\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$). Surprisingly, SEFIs in the controlled logic of the NAND flash have also been observed where the complex logic (including charge pump, buffers, decoders, internal microcontroller etc.) was not empowered to perform for example read, write or erase operations. Errors in the control logic were noticed when the DUT was powered up after irradiation to read the bit errors for the SEU evaluation. A reset or power-cycle of the DUT was required to read out the data again or re-program the memory device. The cross-section results for static tests under unbiased and biased conditions are presented in Figure 5.5.



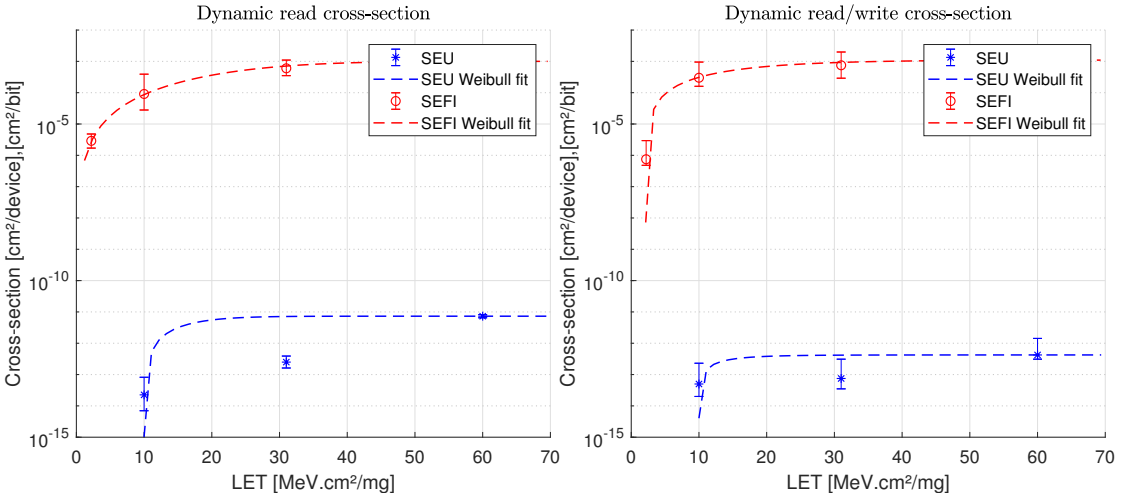
(a) Unbiased condition (b) Biased condition

FIGURE 5.5: Cross-section for the static test under (a) unbiased and (b) biased condition (unbiased: W=3.50 S=0.79; biased: W=8.65 S=1.35), adopted from [114].

For unbiased devices, only a single SEFI was recorded at the highest tested LET. The SEU cross-section saturation is at approx. $2.1 \times 10^{-12}\,\mathrm{cm}^2/\mathrm{bit}$. Under biased condition, the SEU rate is similar, but the SEFI cross-section significantly increases due to the powered control logic. SEFIs were observed at an LET of $10\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$ and the cross-section saturation is at about $4 \times 10^{-4}\,\mathrm{cm}^2/\mathrm{device}$.

Dynamic tests were carried out in two different ways. The first test is in read-mode where the DUT is continuously read out during irradiation. In this configuration, static bit errors were counted in addition to erroneous read operations that occur due to transient noise in the reading circuit and were subtracted after irradiation for reading errors. As SEFIs requires a reset or power-cycle of the DUT, the reading or transient errors get lost and only static bit errors could be determined afterward (like on the static test). Thus, the SEU cross-section differs slightly between static and dynamic test modes. However, the most critical part is the control logic of the NAND flash that needs to be evaluated in more detail, specifically under dynamic operations. The SEFI cross-section for the dynamic read-mode is presented in Figure 5.6 (a) and is relatively higher compared to static test modes. The second dynamic test mode is performed by read, erase and write

operations during irradiation. The DUT is read block-by-block and if an error is detected the block is erased and re-written. The SEFI cross-section presented in Figure 5.6 (b) is higher than for other test modes due to the higher voltages of the charge pump that are required to perform the erase and write operations. These effects were also observable on the power consumption of the DUT that results in a temporarily high current states and which can be correlated to SEFIs during write and erase operations.



(a) Dynamic read mode (b) Dynamic read/erase/write mode

FIGURE 5.6: Cross-section for the dynamic test for (a) read mode and (b) read-/erase/write mode (read: W=28.17 S=2.24; read/write: W=18.52 S=1.34), adopted from [114].

SELs have not been observed during irradiation. However, it has been found that these high current states and spikes may cause critical damage to the devices leading to irreversible destructive failure (DF). High current spikes occurred also in static biased mode but never led to any destructive damage to the DUT.

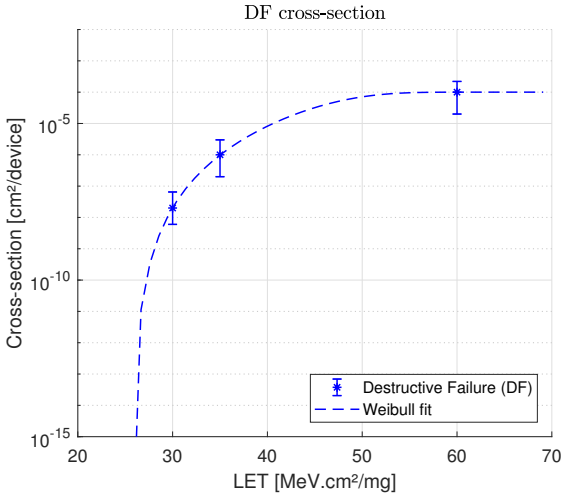


FIGURE 5.7: Cross-section for destructive failures (W=23.32 S=5.03), according to [139, 140].

The corresponding cross-section for DF is presented in Figure 5.7 on the previous page as evaluated by [139, 140].

5.1.3 DDR3-SDRAM

Dynamic memories that are required by the GSDR to provide computing resources for OS and software applications are based on DDR3-SDRAM technology. Fortunately, such devices have been intensively evaluated for radiation effects in the context of the ESA RadHard memory study [140]. This study took place from 2011 to 2014 with several test campaigns on TID and SEE evaluation under proton and heavy-ion irradiation. Several manufacturers and devices were investigated from 2 Gbit to 4 Gbit devices. The only devices not being obsolete at this point are the Micron DDR3-SDRAM with 2 Gbit (MT41J256M8HX.15E:D) and 4 Gbit (MT41J512M8RH-093:E). Both devices are supported by the Zynq BBP which is important if ECC is to be enabled. As for the NAND flashes, Micron qualifies the automotive-grade DRAMs according to AEC-Q100 (selection criteria). In the following, the radiation test results on both devices are highlighted to discuss their use in the GSDR system design and to evaluate potential failure propagation and their influence on the overall system performance.

Total ionizing dose

TID testing has been carried out on both SDRAMs, 2 Gbit (MT41J256M8HX.15E:D) and 4 Gbit (MT41J512M8RH-093:E). For the 2 Gbit device, six samples have been exposed to γ-rays under ambient and elevated temperature (80 °C) for unbiased condition. The total dose achieved by the DUTs is about 400 krad(SiO_2). For ambient temperature, only a single error (1-to-0 transition) was observed. At elevated temperature, the DUTs showed higher number of random errors and a weak response to band error pattern which appears in several error regions with different error intensity [141]. Biased condition has not been evaluated for the 2 Gbit device.

The 4 Gbit device has been tested in more detail under unbiased and biased conditions. In unbiased condition, 10 samples were irradiation and showed no errors under ambient temperature and only few errors (in both directions) at elevated temperature (80 °C), similar to the results observed on the 2 Gbit device [142]. During the in-situ testing (biased condition), the DUT is initially written with a pseudo-random pattern and continuously read in 15 minute intervals to compare the content and determine the errors. The DUT is then overwritten to the original pattern and the procedure is repeated until the target total dose of 400 krad(SiO_2) has been achieved or the DUT fails. The supply current of the whole DUT is measured during irradiation. The idle current increased from 9 mA to 116 mA during irradiation as illustrated in Figure 5.8 on the following page.

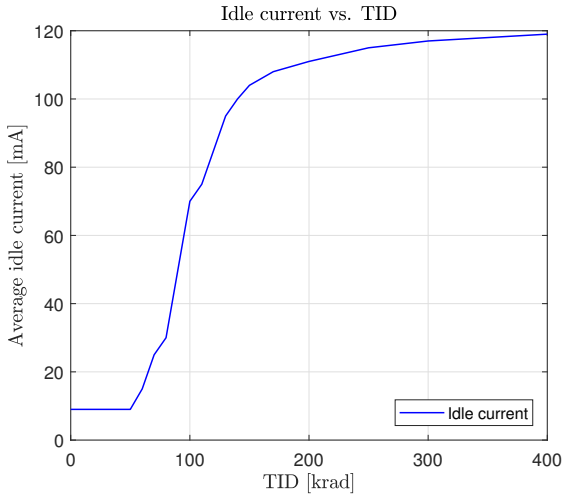


FIGURE 5.8: Average idle current vs. TID of the 4 Gbit DDR3-SDRAM, adopted and modified from [143].

The first bit errors were observed at around 90 krad(SiO_2). The number of errors rapidly increased, similar to what had been observed for the idle current. The error density that has been determined is about 1.2×10^{-2}.

Single event effects

SEE testing was performed on heavy-ion and proton irradiation. Heavy-ion tests were conducted on five 2 Gbit Micron devices (MT41J256M8HX.15E:D) and proton testing has been carried out on six Micron MT41J512M8RH-093:E with 4 Gbit data storage. Thus, primary focus is made on the radiation effects evaluation of the 2 Gbit device which is based on a 50 nm CMOS technology. Due to the complexity of the devices, different test modes were tested, as described in [140, 144]. To evaluate the SEE response the devices were written with a checkerboard pattern (AA_{hex}) prior to irradiation and verified to detect stuck bits that are cells which always read a fixed content independent of the data written to them. In storage mode, the devices are irradiated without any activity, except the required idle sequence (auto-refresh) that is performed every 7.8 μs. After the devices have irradiated to the target fluence, the data are read and compared to the initial written values. In storage mode, SEUs and SEFIs organized in rows and columns are evaluated for errors. These SEFIs consist of many bit errors occurring in a single row or column that are typically caused by a failure in the control circuit (not counted as MBUs). In read mode, the devices are continuously read. The third mode includes a continuous read and write operation which represents the most practical scenario.

HEAVY-IONS

The cross-section results for SEUs in all three modes are presented in Figure 5.9 on the following page. The results have been adopted and modified for common illustration purposes. The Weibull fitting has been calculated by means of the OMERE software

[32]. The cross-sections for read mode and read/write mode are very similar, except for the Weibull fitting due to the mission cross-section data for the lowest LET on read/write mode.

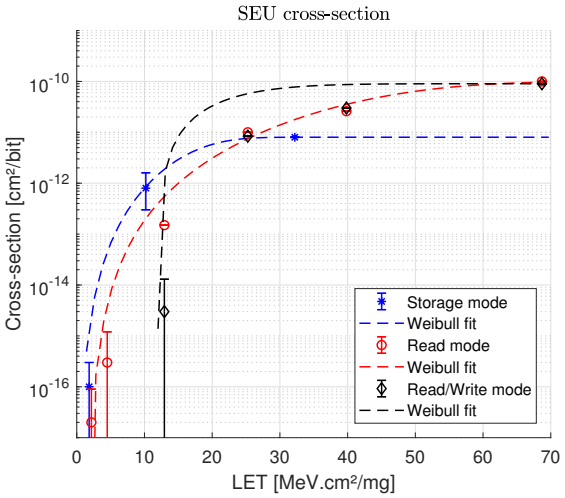
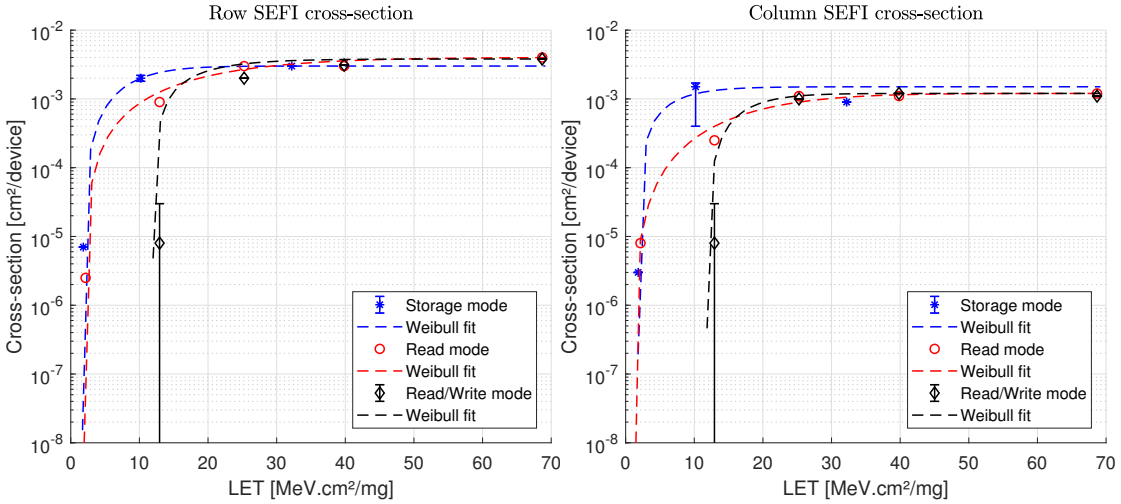


FIGURE 5.9: SEU cross-section in storage mode (W=13.15 S=1.58), adopted and modified from [118, 140].

The different cross-sections compared to the storage mode can be explained by the loss of information during the irradiation runs where a device SEFI could not be observed. Thus, it can be assumed that the SEU cross-section is more valuable for the read mode and read/write mode. Column and row SEFIs in all modes are presented in Figure 5.10.



(a) row SEFIs (b) column SEFI

FIGURE 5.10: SEFI cross-section in storage mode for (a) row SEFIs, and (b) column SEFIs (row: W=7.22 S=1.04; col: W=6.39 S=1.25), adopted and modified from [118, 140].

SEFIs, either for rows and columns, were observed at all tested LETs except for the read/write mode, as is similar to the results observed for SEUs (at a lower LET threshold). The numbers of SEFIs are in the same order of magnitude as for SEUs. As SEFIs

cause hundreds of bit errors, the failures induced by SEFIs are much higher compared to random SEU bit errors. The SEFI cross-section saturation is almost equal in all three test modes. In some cases the DUT has been affected by incident particles in the control circuit causing a persistent loss of functionality. These failures are defined as device SEFIs and can be resolved by a reset or power-cycle of the device. The corresponding cross-sections are presented in Figure 5.11 and are accumulated for all modes.

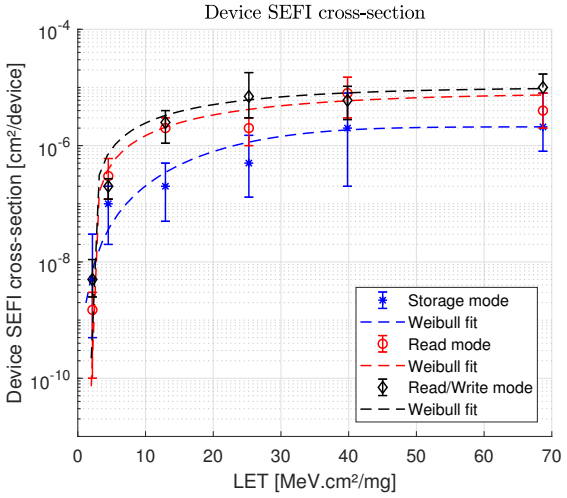
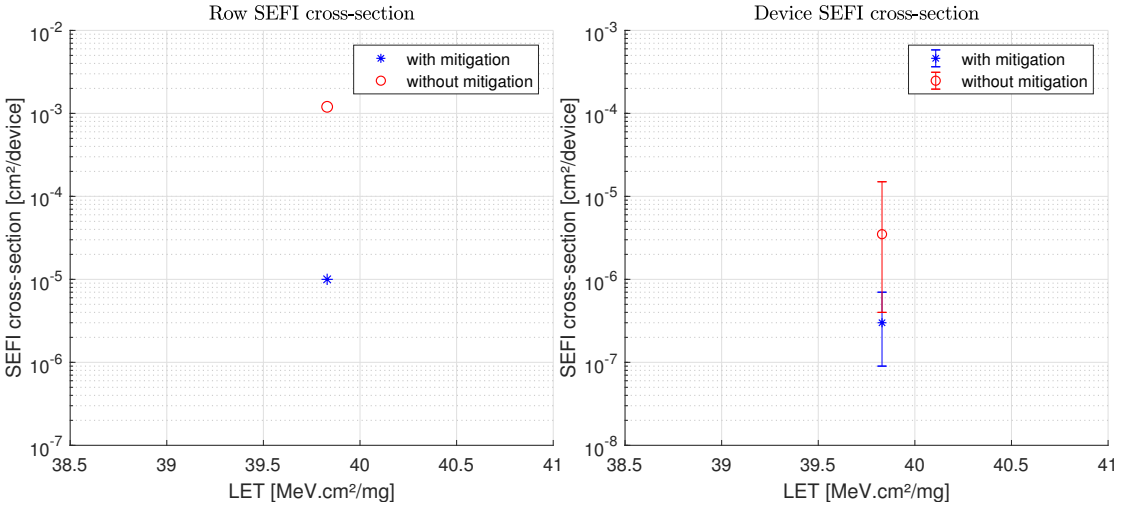


FIGURE 5.11: SEFI cross-section for the entire device for all modes (W=24.45 S=1.14), adopted and modified from [144].

[144] also showed that software conditioning (SC) can significantly improve the SEFI cross-section. With SC enabled, a set of operations is performed at frequent time intervals or after regular numbers of read and/or write operations. These operations are for example the rewriting of mode registers, resetting the internal DLL of the DUT and re-calibration of the data lane termination resistance.



(a) Row SEFIs (b) Device SEFIs

FIGURE 5.12: Effect of software conditioning (mitigation) in read and write mode to (a) row SEFIs, and (b) device SEFIs, adopted and modified from [144].

The cross-section results with and without SC for row SEFIs and device SEFIs are presented in Figure 5.12 on the previous page. Such tests were only performed on a single LET of 39.83 MeV · cm^2/mg. It has been found that the SEU response is not significantly improved with SC enabled. SEFIs' cross-sections are thereby affected by SC in the order of at least one magnitude. Especially for column SEFIs, no errors have been observed.

A further note, of the utmost importance, is that SEL or other destructive events were not observed for any test mode and LET.

PROTONS

Proton testing has been carried out by [145] only on the 4 Gbit DDR3-SDRAM that uses a 30 nm CMOS technology. Six samples were irradiated under different proton energies up to 230 MeV. The test procedures were identical to those being used in the heavy-ion test campaign. The cross-section results for SEUs and SEFIs in read/write mode are presented in Figure 5.13. The SEU cross-section is fairly low and saturates at around 4×10^{-18} cm^2/bit which remains far below the die area per bit ($\approx 2 \times 10^{-10}$ cm^2/bit). The error direction is approximately equal (1-to-0 and 0-to-1 transition). It can be observed that the SEU cross-section at energies below 50 MeV is increased compared to at higher energies. It is assumed that the SEE sensitivity is increased at feature sizes below 65 nm and direct ionization of low energy protons is more likely [146].

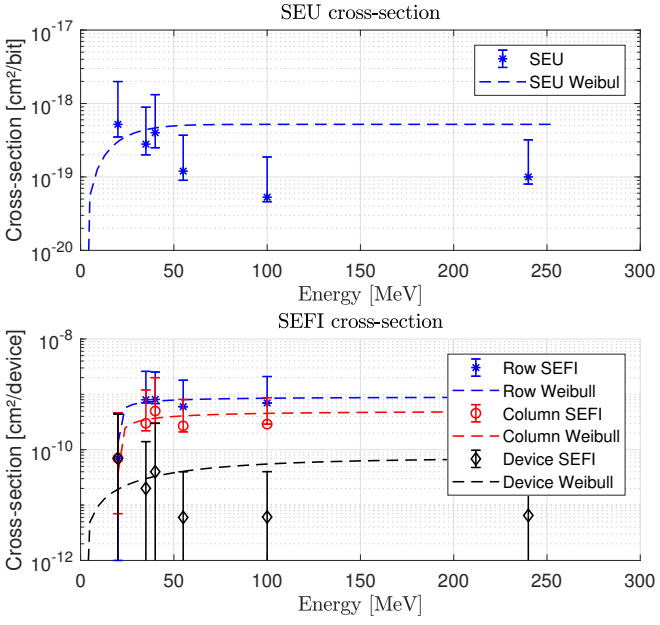


FIGURE 5.13: SEU and SEFI cross-sections in any mode, adopted and modified from [145].

Further investigation would be required to verify this phenomenon on the DUT but is not determined as critical since the cross-section is fairly low. Column and row SEFIs

were observed in a similar order at around $3 \times 10^{-10}\,\mathrm{cm}^2$/device. The device SEFI rate is about one magnitude lower. Based on the experience of the heavy-ion testing, SC should remove all these SEFIs but this has not been verified.

5.2 AD9361 - RF agile transceiver

The third and probably most important critical system devices is the highly integrated RF agile transceiver AD9361 from Analog Devices. The RFIC is more or less unique and an essential game-changing device for SDR technologies. It allows a software-based reconfiguration of various RF characteristics such as local oscillator (LO)-frequency, analog filter-bandwidth, gain-control of the input and output amplifier, sampling rates of the integrated ADC/DAC and further more. Due to the fact that the whole idea of the GSDR is based on such flexible technology and no space-qualified solutions nor radiation test data for reference is available, a detailed investigation is mandatory. In this section, the characterization of the AD9361 for TID and SEEs, under proton and heavy-ion irradiation, is presented. To highlight the complexity and high integration of the device, a functional block design of the AD9361 is depicted in Figure 5.14.

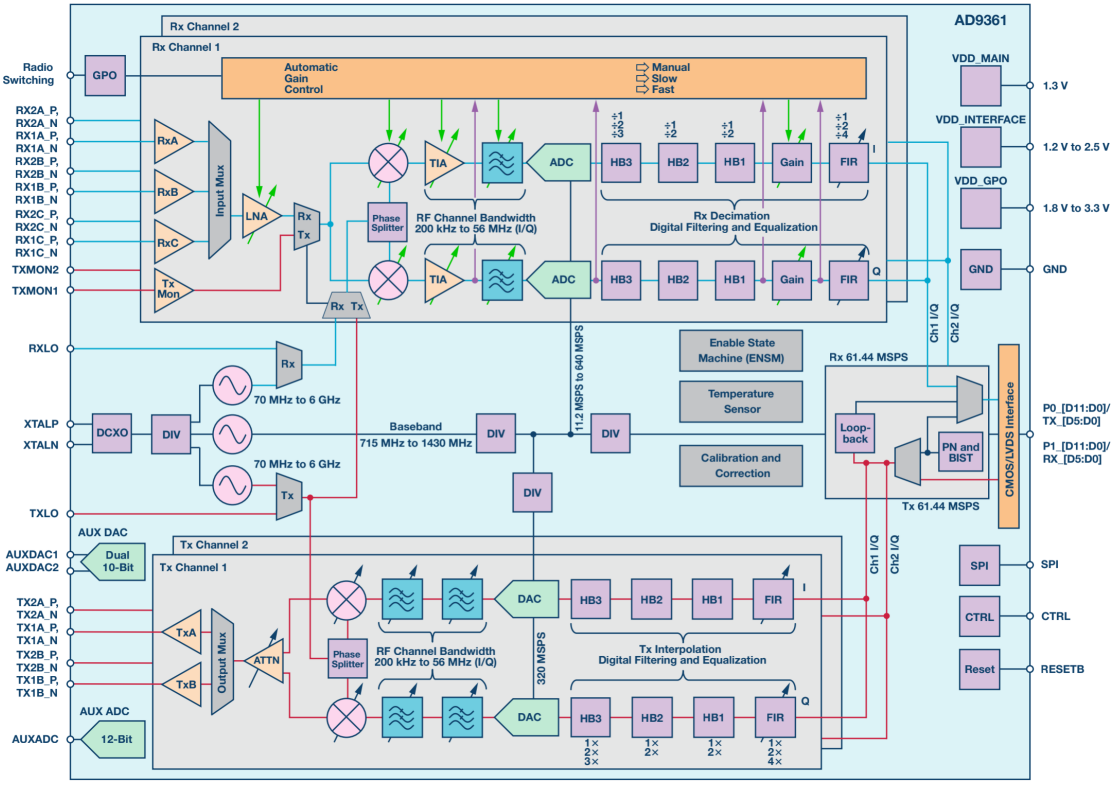
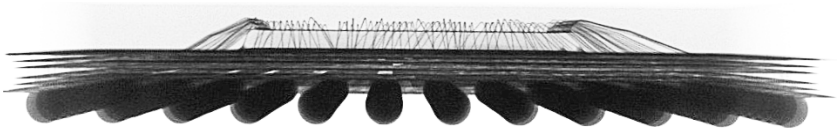


FIGURE 5.14: AD9361 RF agile transceiver functional block design, from [147].

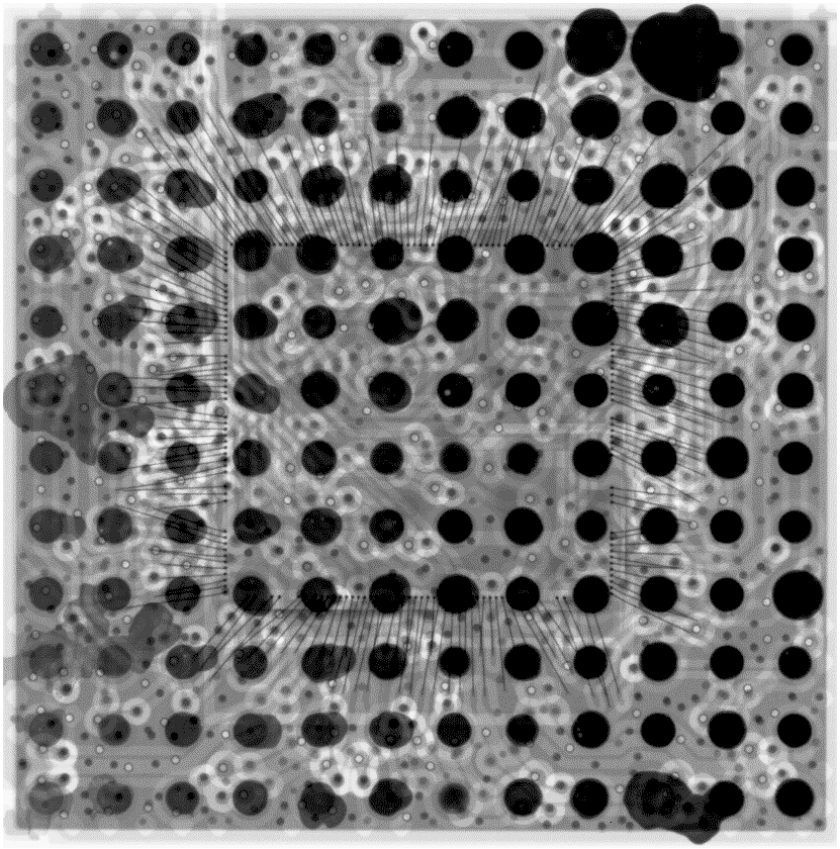
The AD9361 is equipped with a fully-integrated 2x2 receiver and transmitter chain that can be controlled and operated individually. The data are mixed into/from the baseband

without any IF. The required clocking signals (e.g. for ADC/DAC or the LO-frequency) are generated and provided by an integrated frequency synthesizer. The configuration of functionalities is register-based and can be accessed by a serial peripheral interface (SPI). More detailed information can be found in the data sheet [148].

As can be seen, radiation effects can have an impact at different stages (e.g. synthesizer, amplifiers or functional register) of the AD9361 and it is a big challenge to evaluate the response in adequate detail since probing on the die is not possible. Thus, prior tests can be executed, the development of a test methodology and procedure is mandatory for different radiation test conditions to extract as much information as possible. Firstly, the device is analyzed with respect to its technology to both, determine the susceptibility to certain radiation effects and to prepare the DUT for different tests (e.g. device de-lidding for heavy-ion).



(a) Side-view



(b) Top-view

FIGURE 5.15: X-ray picture of the AD9361 in (a) side-view, and (b) top-view, according to [149].

The RFIC is fabricated on a 65 nm TSMC CMOS process and is encapsulated in a $10 \cdot 10 \cdot 1.7\,\mathrm{mm}^3$ 144-ball chip-scale package ball grid array (CSPBGA). The molding compound of the CSPBGA is mainly based on silica and epoxy/phenol resin. An x-ray picture of the AD9361 is presented in Figure 5.15 on the previous page to portray the effective die-size and the thickness of the device encapsulation.

The die has a size of $\approx 4440 \cdot 4800 \cdot 2200\,\mu\mathrm{m}^2$ and is assembled face-up. As seen in the side-view in Figure 5.15 (a), bond-wires are connected to a PCB stack underneath that interfaces the die to the ball grid array at the bottom of the device. The plastic encapsulation above the die surface has a thickness of $\approx 280\,\mu\mathrm{m}$. Thus, heavy-ions are unable to penetrate the sensitive region and a package-opening is required. A picture of the die surface after the device has been decapsulated is presented in Figure 5.16. A metalization on top can be observed. More detailed and high-resolution pictures of the die can be found in [150].

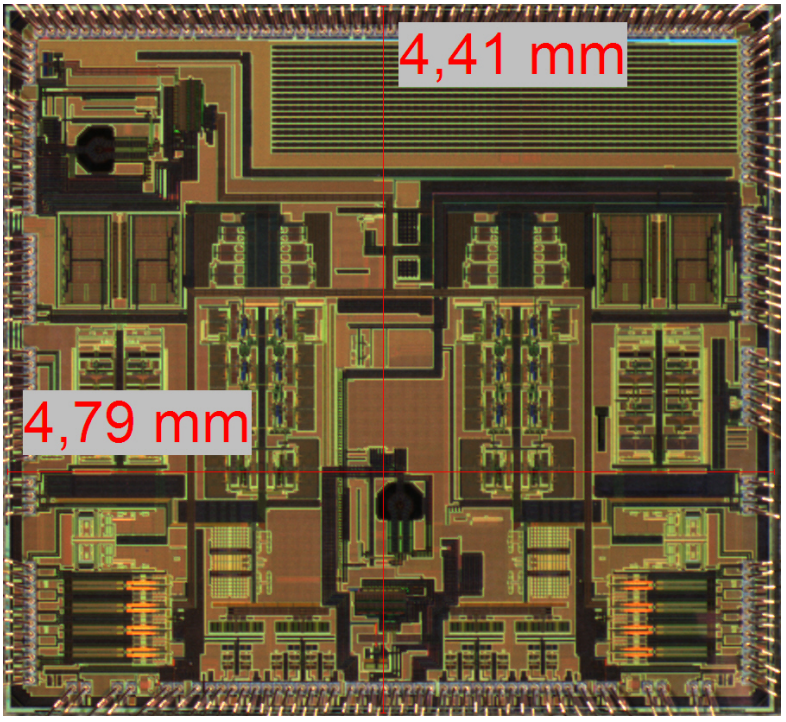
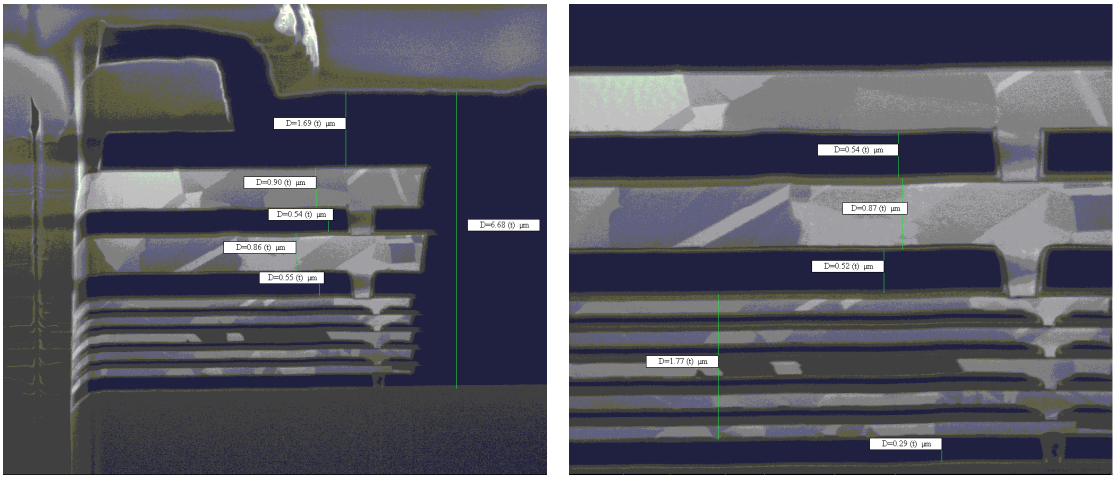


FIGURE 5.16: Picture of the etched DUT showing the AD9361 die surface and its dimensions, according to [151].

The die inspection presented in [150] also described in more detail the structure and organization of the device. At the top right corner one can see the main digital block which for example could implement the internal and programmable 128-tap FIR filter. The cells are placed in back-to-back [PFET NFET][NFET PFET]. The analog circuits are mostly FET-based and it seems to be that the digital structure is not based on a typical SRAM topology. In order to analyze the die structure in more detail, especially in terms of the observed metalization, a focused ion beam (FIB) cross-section is performed

to determine the metalization structure and to evaluate the orientation of the active region. The cross-section of the FIB is presented in Figure 5.17.



(a) FIB cross-section (b) FIB cross-section, magnified

FIGURE 5.17: FIB cross-section of the DUT showing the die structure and its dimensions, according to [151].

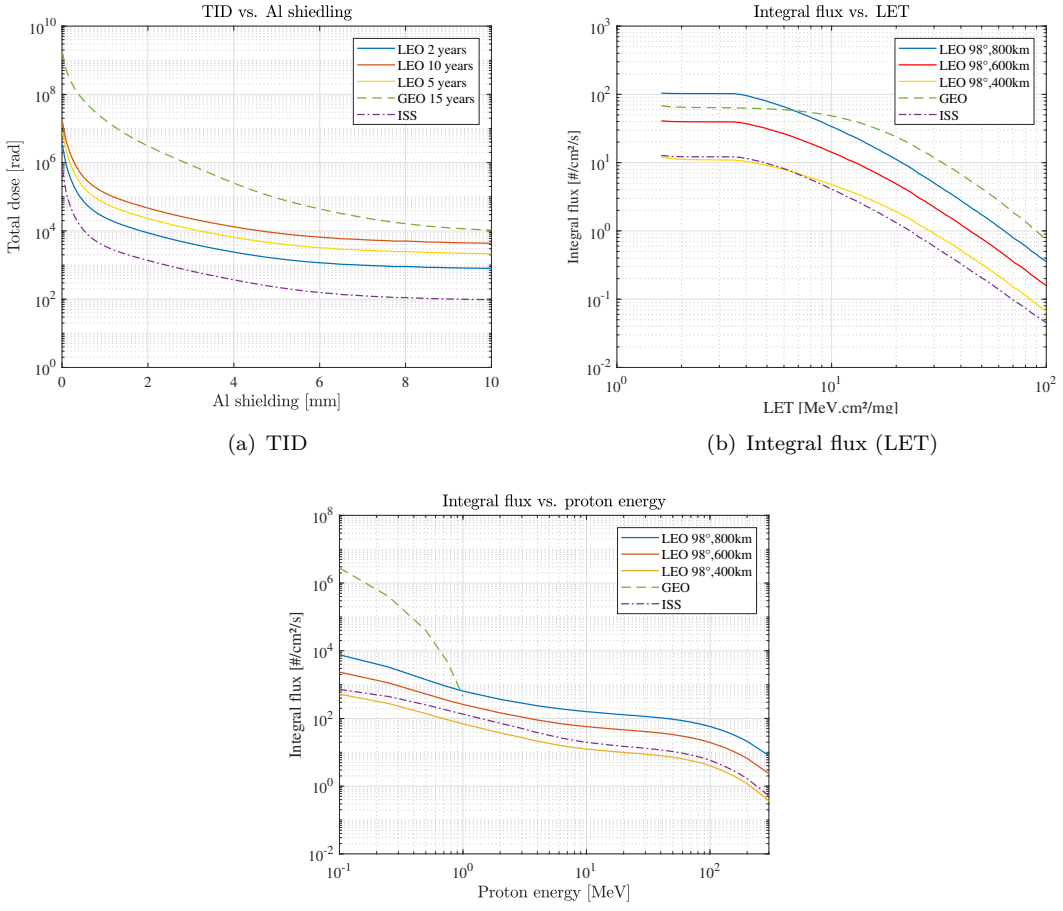
In total, seven layers of metalization can be observed. The metalization is made of copper and each layer has a thickness of approximately 250 nm to 900 nm. The presence of metalization in the die area varies in numbers and total thickness. The active area is the very thin layer above the substrate at the bottom. The substrate and infill material between the metalization layers (dialectic) are made of silicon dioxide (SiO_2).

The distance from the die surface and the active area is measured at $\approx 6.68\,\mu$m. The cross-section is lastly important for determining the effective LET in the active region when particles pass either straight through the dielectric or if they also traverse through the copper metalization layers.

5.2.1 Test conditions and requirements

Due to the fact that the TID and SEE response is unknown for the AD9361, two ways are defined in order to characterize its performance under radiation conditions. Primarily, the test requirements and conditions are according to the ESCC standards and guidelines No. 22900 for TID ([152]) and No. 25100 for SEEs ([153]), respectively. Since the focus is on the characterization and not a qualification is considered, tailoring to these guidelines and requirements is desirable. Specifically the number of samples is reduced since the complexity of testing will not allow such detailed qualification approach. In the case of the AD9361, two samples are usually tested. Since the use of radiation test facilities is very expensive (especially for particle acceleration), the target total dose, the particle fluence and the numbers of LET or proton energies may also be

tailored too. In order to determine a minimum fluence and TID that is required to test to, a calculation for most popular and suitable reference missions for the GSDR has been performed and is presented in Figure 5.18 (a) for TID, (b) integral flux vs. LET, and (c) integral flux for trapped protons. The main test purpose however, is to test according to the guidelines that are commonly used by space industries. For TID, a target dose is not specifically defined in ESCC 22900 and is highly dependent on mission requirements. Thus, assuming that 90 % of the suitable mission may be in LEO (e.g. 800 km, 98 °) a target total dose of $\geq$10 krad(SiO_2) is desired (to represent two years). According to ESCC 25100, a target fluence of $1 \times 10^{+7}$ heavy $-$ ions/cm^2 and $1 \times 10^{+11}$ protons/cm^2 is required. Considering the same reference mission, a maximum target fluence of $\approx 5 \times 10^{+9}$ protons/cm^2 at 50 MeV would be sufficient to test and could reduce the required beam time and thus the costs. For higher proton energies, the fluence decreases according to Figure 5.18 (c).



(a) TID

(b) Integral flux (LET)

(c) Integral flux (Proton)

FIGURE 5.18: Calculated TID (a) and integral flux vs LET (b) and protons (c) for popular reference missions, calculated with OMERE [32].

It is mandatory to test up to approximately 200 MeV and at least five different intermediate energies should be selected. For heavy-ions, the mission-dependent target fluence

may even exceed the required fluence according to ESCC 25100. It is not required to test against the mission fluence if sufficient numbers of errors were counted to ensure an adequate error statistic. Similar to proton testing, at least five different LETs should be selected to evaluate an appropriate cross-section and to determine the thresholds of the SEE response. For all radiation tests, the DUTs have been characterized at ambient temperature and under nominal biased conditions.

5.2.2 Total Ionizing Dose

5.2.2.1 Test facilities

For TID testing, different radiation sources can be used. The most common method is to use Cobalt-60 (Co60) that emits γ-rays to the DUT. Different test campaigns on the AD9361 have been performed at the Helmholtz-Zentrum Berlin (HZB) [154]. Co60 decays in nickel-60 by emitting β- and γ-rays. β-rays are absorbed by a steel shielding. The γ-rays have an energy of 1.17MeV and 1.33MeV and generate a dose rate from of 0.2 krad/h to 20 krad/h (in water, date: 2018), depending on the distance to the Co60 source. The irradiation area of the HZB is about 5x5 m^2 with the source placed in the center of the room. In order to achieve extremely high dose rates (several Mrad per hour), the OBELIX x-rays source of CERN [155] was used in a later test campaign to deliberately force device failures that were not achieved during irradiation with γ-rays.

5.2.2.2 Test setup

The general test setup of the TID test campaigns is presented in Figure 5.19 on the following page. The setup allows the characterization of two samples at the same time due to an independent power distribution and control circuit. The setup was usually designed for Co60-tests where there is a long distance between the control room and the irradiation area ($\geq$15 m). For the x-ray test, the same test setup is used but samples are needed to be tested one by one since the x-ray source has a narrow beam-size of about 1x2 cm^2. The DUT is soldered on a commercially available evaluation board (FMCOMMS3-EZB) and is attached to a shielded FPGA board for data processing and to establish control of the AD9361. The FPGA board supports an Ethernet interface which allows long-distance interconnection to a control computer and the evaluation SW.

Each DUT is powered by the FPGA board, which on the other hand is supplied by an individual power device in the control area. Voltage and current levels of the DUT and the FPGA board are continuously measured by a data acquisition (DAQ) module (NI9205). In order to characterize the RF performance of the DUT, each device is fully

operated and connected via RF cables (2RX2TX) to a reference transceiver system in the control area.

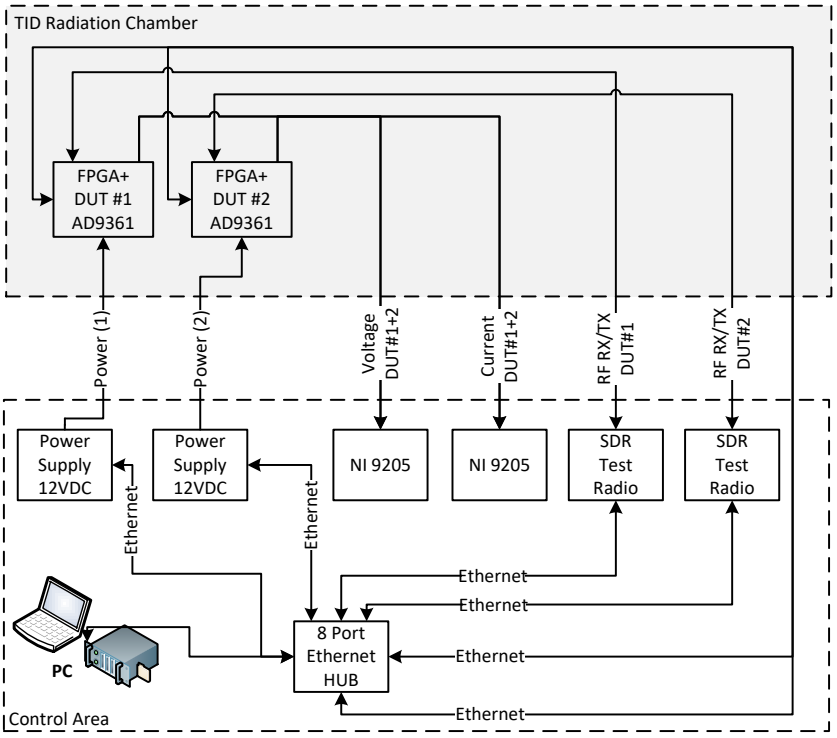


FIGURE 5.19: TID test setup for two samples of the AD9361, according to [156].

The reference transceiver system is based on the same SDR architecture including the FMCOMM3-EZB evaluation and an FPGA board. The qualitative evaluation of the RF performance under irradiation is based on the baseband data, provided in complex values (IQ). The test procedures are discussed in more detail in the following section 5.2.2.3.

5.2.2.3 Test procedure

During irradiation, an in-situ (live) test is performed which continuously transmits and receives a sine-wave on fixed transceiver configuration (e.g. AGC enabled, 2.4 GHz carrier frequency, 10 MSPS sample rate etc.). For the γ-rays test, the DUT is evaluated for degradation effects by a detailed performance test every $\approx$45 krad(SiO_2),. The performance test is based on the captured/transmitted IQ data of the DUT and its corresponding reference transceiver at different devices settings and the measured voltage and current values by the DAQ module:

SUPPLY CURRENT

The supplied voltage and current conditions are monitored independently on the type of operation whether it is the in-situ test configuration or during detailed performance tests. The supplied current is usually the main indicator in terms of degradation on

electronic devices with increased total dose. During the performance test the DUT is configured through all enable state machine (ENSM) modes and a fixed increment sweep to the operated frequency bands by tuning the LO frequency is performed (70 MHz to 6 GHz). The sweep is applied for all subsequent performance tests.

Automatic gain control

The AD9361 is equipped with an automatic gain control (AGC) unit that configures the receiver chains' amplifier according to the measured received signal strength indicator (RSSI). Each receiver chain is controlled individually. To evaluate the AGC under irradiation, a fixed sine-wave tone is transmitted from the reference transceiver device to each DUT receiver input. The transmitted output power of the reference transceiver is incrementally controlled. The selected gain of the AGC control circuit is monitored as well as the digitized RF input data.

Receiver amplifier

Similar to the AGC test mode, the receiver amplifiers are characterized to degradation of the performance (gain) with increased TID levels. In this test, the receiver gain is manually selected and the transmitted sine-wave tone of the reference transceiver is configured to a fixed output power. Thus, one can observe either degradation in the gain function and/or potential saturation changes on the input amplifiers.

Receiver local-oscillator leakage

To observe changes in the receiver local-oscillator leakage (LOL) performance, a constant sine-wave is transmitted by the reference transceiver and the DUT receiver gain is incrementally increased. The difference between the DC-offset and the captured sine-wave is evaluated vs. increased receiver gain.

Receiver filter bandwidth response

The smallest possible RF analog filter bandwidth of 200 kHz is selected. The transmitted sine-wave tone of the reference transceiver is swept through the filter bandwidth (and 4x out of band) to measure the filter response in the frequency domain. The shape of the filter is captured and compared for different TID levels.

Transmitter attenuation

To characterize the transmitter amplifier performance of the DUT and its potential degradation under irradiation, the DUT transmits a sine-wave tone with variable output power (by control of the output attenuator) to the reference transceiver. The reference transceiver is configured to a fixed receiver gain and captures the transmitted signal of the DUT for further data evaluation.

Transmitter inter-modulation distortion

A second test mode for characterizing the amplifiers' performance is to drive the amplifier to saturation and to produce inter-modulation distortion (IMD). In order to do so, two

sine-wave tones (1 MHz and 2 MHz) are transmitted to the reference receiver device. The input receiver gain is selected to a minimum to prevent the generation of inter-modulation products on its own. With the increased output power of the DUT, the reference receiver records the input signal and analyzes the inter-modulation products (3rd and 5th order). The distances between the fundamental tones and the IMD products are evaluated with increased TID.

Transmitter local-oscillator leakage

Similar to the receiver, the transmitter is also able to produce leakage power of the LO to the output signal. To observe the behavior of the transmitter LOL, the DUT transmits a sine-wave tone with adjustable output power to the reference transceiver that is configured to a fixed input gain (though small enough to not produce RX LOL). The input signal of the reference transceiver and the DC-offset are captured and is analyzed with increased transmitted output power.

5.2.2.4 Test results

The TID test results for the performance characterization on γ-rays are presented in the following Figures 5.20-5.27. For illustration purposes, only four (1.6 GHz, 2.4 GHz, 3.2 GHz and 4.0 GHz) carrier frequencies have been selected. However, for other carrier frequencies no further abnormalities nor degradations have been observed.

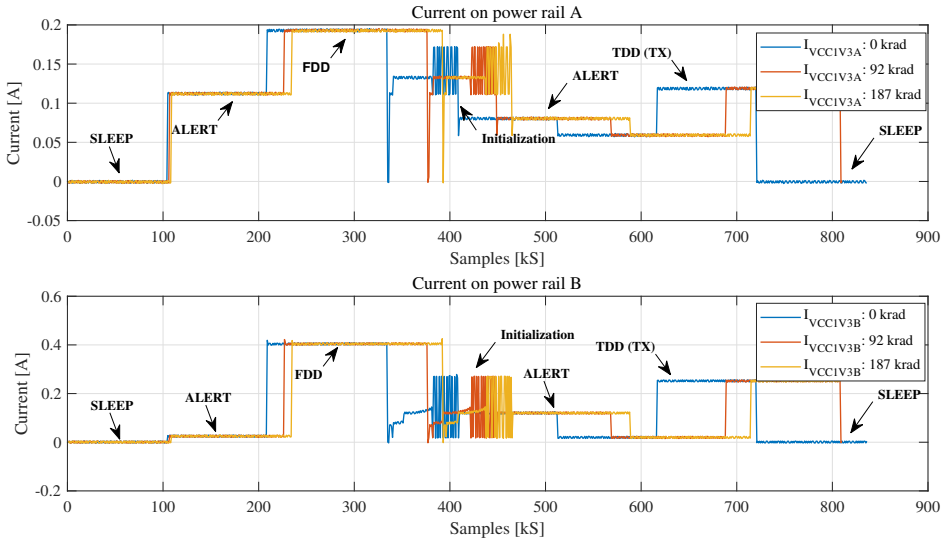


Figure 5.20: Supply current for different ENSM modes and initialization phases, according to [156].

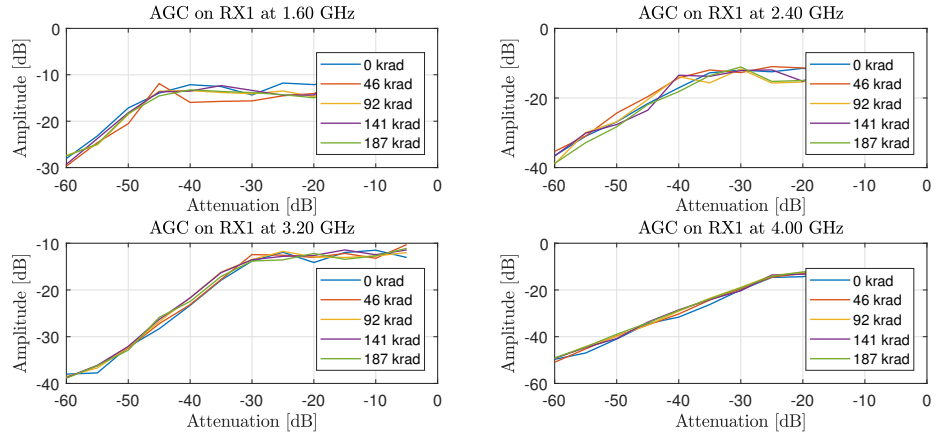


FIGURE 5.21: AGC and RX amplifier performances vs. TID, according to [156].

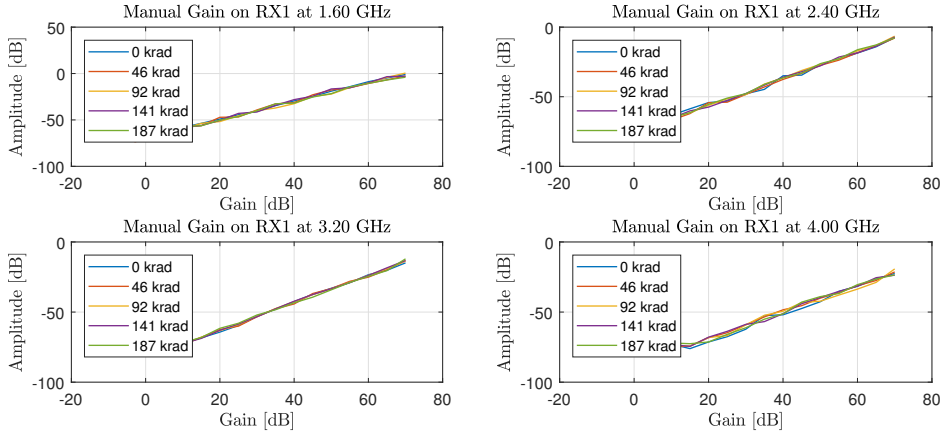


FIGURE 5.22: Manual gain and RX amplifier performances vs. TID, according to [156].

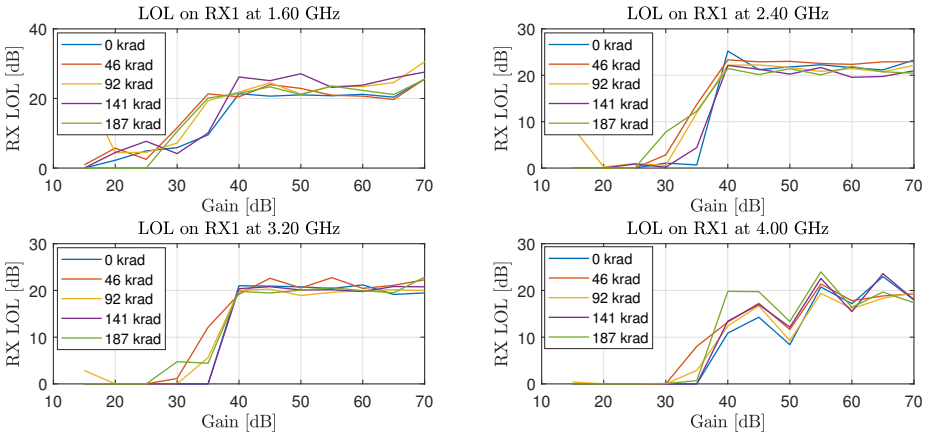


FIGURE 5.23: RX LOL performances vs. TID, according to [156].

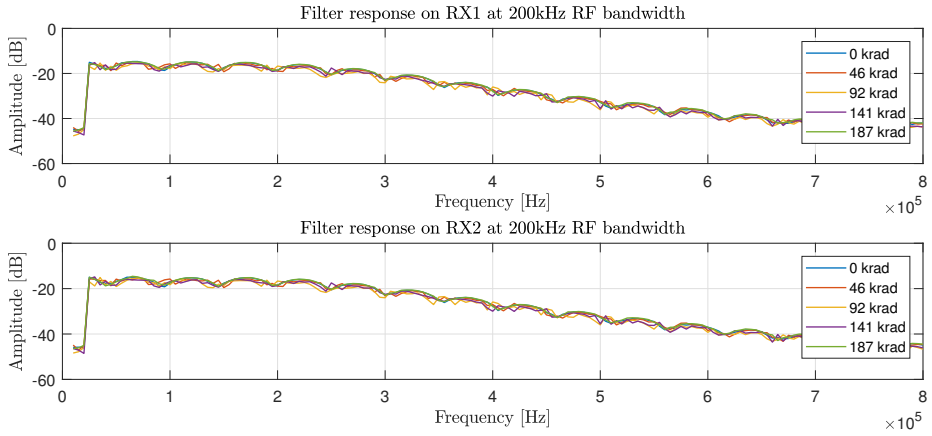


FIGURE 5.24: RX filter response vs. TID, according to [156].

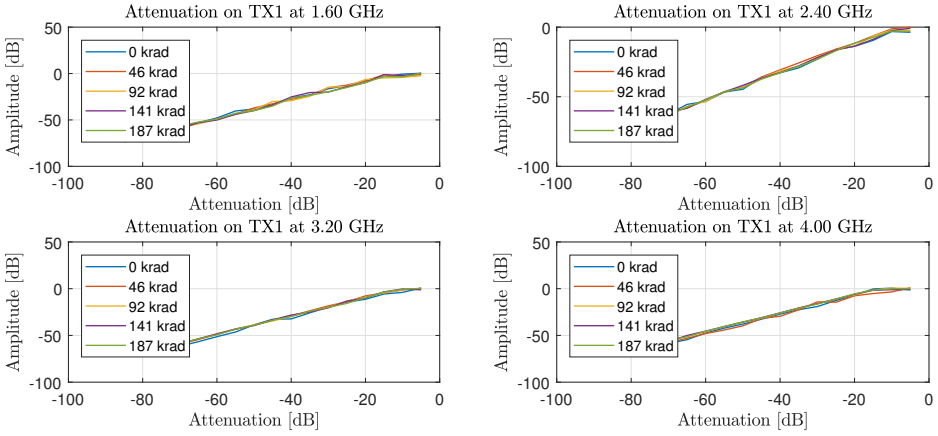


FIGURE 5.25: Attenuation and TX amplifier performances vs. TID, according to [156].

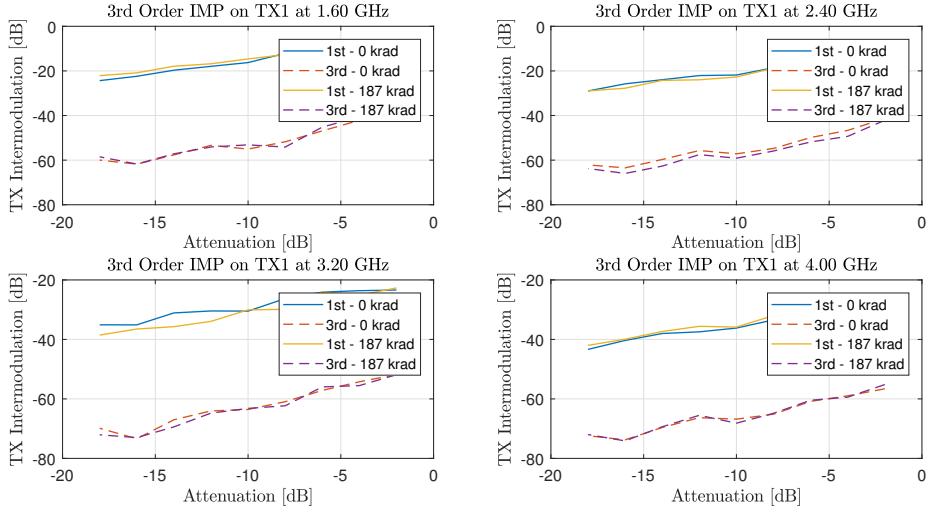


FIGURE 5.26: IMD with fundamental tone and 3rd IMP vs. TID, according to [156].

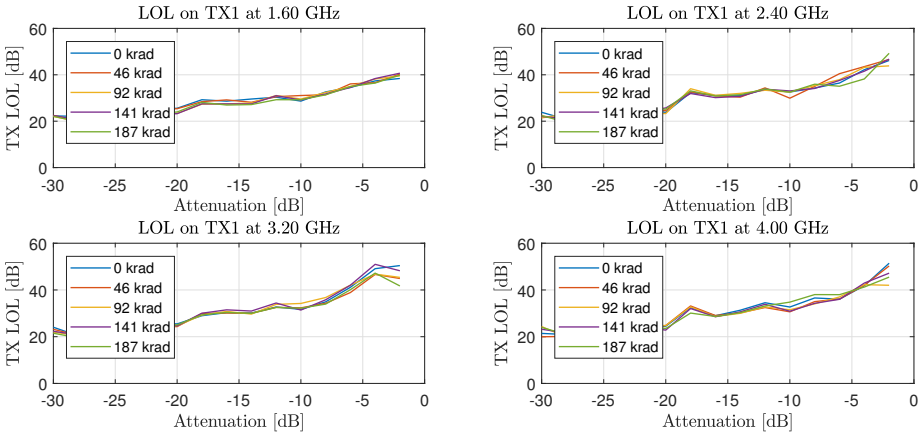


FIGURE 5.27: TX LOL performance vs. TID, according to [156].

Since the AD9361 has been proven to be sustainable to TID at dose levels of almost 190 krad(SiO_2) and no degradations have been observed, a further test campaign under x-ray irradiation was performed.

X-ray Test

In addition to the previously presented Co60-test results, an *up-to-destruction test* has been carried out in which the AD9361 was exposed to a total dose of 70 Mrad(SiO_2).

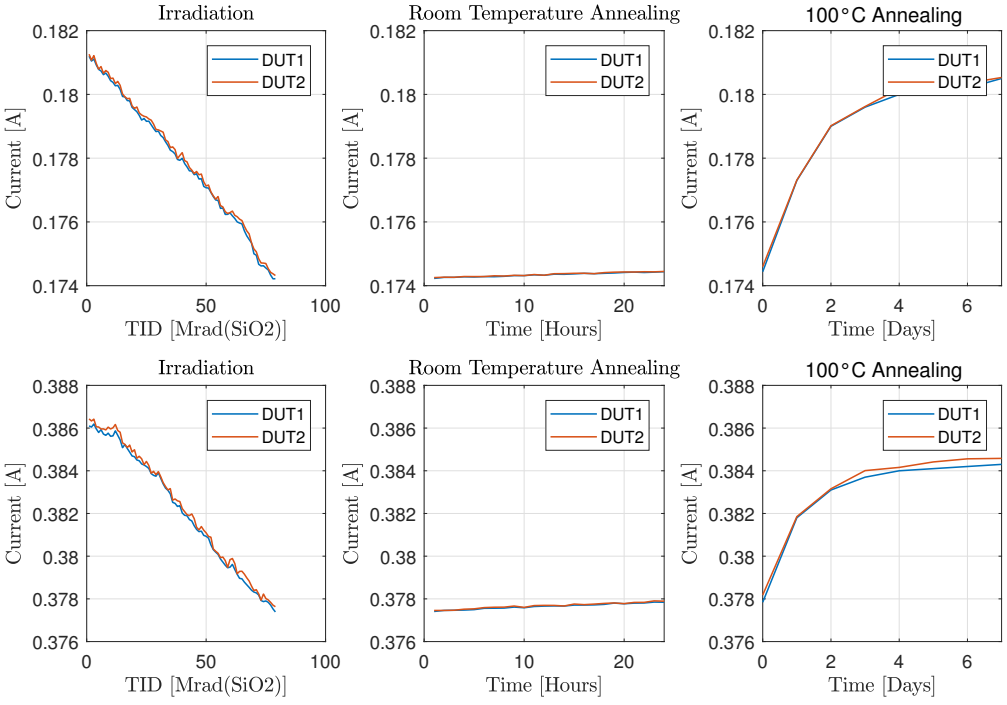


FIGURE 5.28: Supply current degradation under x-ray irradiation and annealing effects and ambient and elevated temperature, according to [157].

Degradation in terms of decreased supply current and finally a loss of functionality has been observed at ≥45 Mrad(SiO_2). Performance tests have been executed in the

same manner as for Co60. For the last test-level at 40 Mrad(SiO_2), no degradations have been found. The supplied current vs. increased TID is presented in Figure 5.28 on the previous page. Above 45 Mrad(SiO_2), the DUT was no longer able to receive and transmit data. Annealing procedures according to ECSS 22900 were applied for 24 hours under ambient temperature (21 °C) and at 100 °C for 168 hours. The DUT has been evaluated daily to observe a recovery to the initial function. Current and voltage conditions were measured as well. At ambient temperature, no functional annealing effects have been observed. A slight, linear increase of the supplied current is seen in Figure 5.28. Under elevated temperature conditions, the supplied current increased much faster and a fully functional recovery, without any observable degradation effects of the DUT performance has been observed. A further description and discussion of the test results are presented in section 5.3.4

5.2.3 Single Event Effects

5.2.3.1 Test facilities

SEE testing was performed for proton and for heavy-ion irradiation. In total two proton test campaigns have been carried out at the kernfysisch versneller instituut (KVI) at the University Groningen, Netherlands. The highest primary proton energy provided by KVI at the DUT surface is about 184 MeV and can be adjusted by aluminum degraders that are placed in the beam line, in front of the DUT.

Nom. energy [MeV]	**Al Degrader [mm]**	**Calibration [protons/cm^2/MU]**
184	0	218.57
150	31.5	191.07
120	55.5	162.11
100	69.5	134.57
70	86.5	98.79
60	0	97.55
50	4.0	93.68
40	7.5	89.17
30	10.5	80.10
25	11.7	75.34
20	12.7	63.85
15	13.5	56.46
10	14.2	55.67
7	14.5	53.56
4	14.7	50.94

TABLE 5.1: Specification of the energies (MeV) at the DUT , the resulting calibration factor (protons per cm^2 per measurement unit (MU)) and the amount of degrader material (mm, aluminum) that is required. Primary energies (184 and 60 MeV) are highlighted in bold.

The irradiation field is produced by scattering the primary proton beam using a double scatter foil method (1.44 mm Pb foil and a 0.9 mm Winhomogeneous scatter foil). These scatter foils, together with beam optics and a 100 mm diameter collimator as well as the degraders determine the field at the DUT. A list of energies used in the test campaigns to evaluate the SEE response of the AD9361 is presented in Table 5.1. In the first test campaign, the primary proton energy was selected to 184 MeV and in the second test campaign 60 MeV was chosen. An additional 20 x20 mm^2 rectangular collimator further focuses the beam to the DUT and shield-surrounded (i.e. not desired to be irradiated under test) electronics. The DUTs are mounted on a XY-Table that can be remotely configured to the desired position (DUT1 or DUT2).

A heavy-ion test was carried out at the cyclotron resource centre of the catholic university of Louvain (UCL) using the heavy-ion facility (HIF). The heavy-ion beam is produced with the UCL cyclotron Cyclone-110 and provides a heavy-ion cocktail with ≈9.3 MeV/nucleon (M/Q = 3.33). The beam size is about 25 mm (diameter) and a homogeneity better than 10 % is ensured. The ion-species that were used, their energy and LET as well as the range in silicon is presented in Table 5.2. The HIF operates under vacuum conditions. An XY-table is installed that allows to change the position and apply tilted (angle) configurations to increase the effective LET.

Ion Type	**Energy [MeV]**	**LET [MeV.cm^2/mg]**	**Range in Si [μm]**
Neon	238	3.3	202
Chrome	505	16.1	105.5
Krypton	769	32.4	94.2
Rhodium	957	46.1	87.3
Xenon	995	62.5	73.1

TABLE 5.2: Ion element, energy, LET and range in silicon (Si) based on the UCL HIF specifications that are used for the SEE characterization of the AD9361.

5.2.3.2 Test setup

The test setup to characterize the susceptibility of the AD9361 to SEEs is presented in Figure 5.29 on the following page. Similar to the setup presented for TID effects (Figure 5.19), the architecture is designed to evaluate two DUTs. For particle acceleration, however, only one sample can be irradiated at a time due to the limited beam size. Nevertheless, as the setup includes two samples that can be individually operated, this allows a quick reconfiguration and thus reduces the required beam time since no access to the irradiation area is necessary.

For proton testing, the AD9361 evaluation board (FMCOMMS3-EZB) was chosen, supplied by an FPGA carrier board (zedboard) that was locally shielded to reduce secondary particle interactions and resulting unwanted failures. For heavy-ion testing, the very first

prototype of the GSDR has been used, since the hardware configuration as used for proton irradiation does not fit into the HIF. Furthermore, the AD9361 encapsulation has been de-lidded (see Figure 5.16) to reach the active region with the provided heavy-ion beam. For protons, a decapsulation was not required.

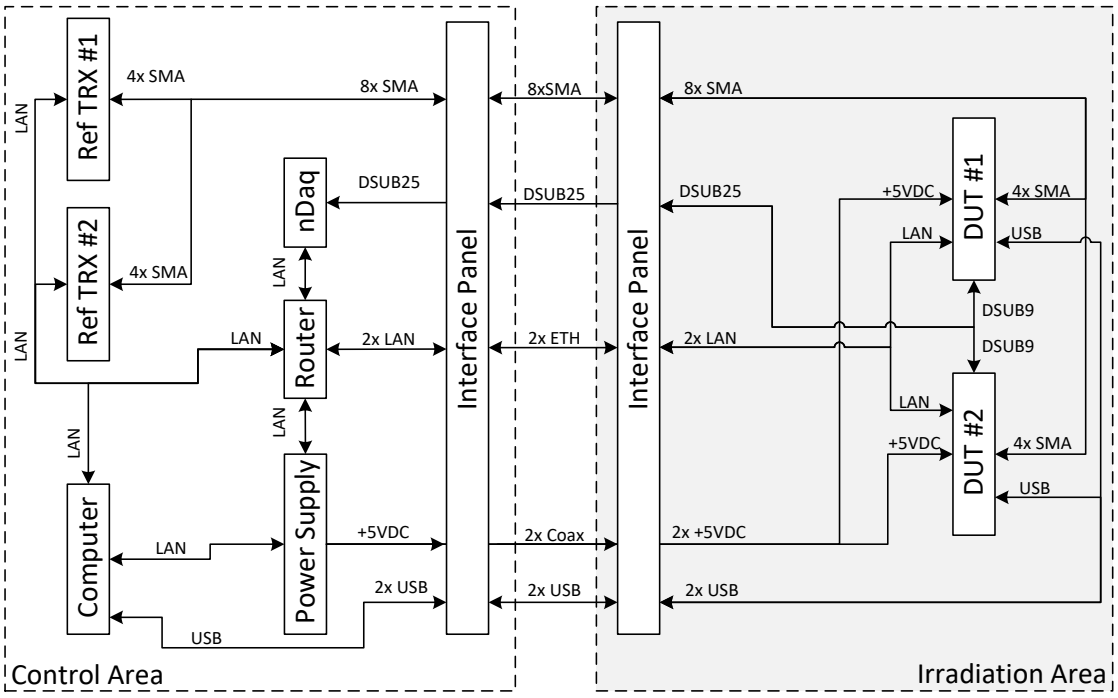


FIGURE 5.29: SEE (heavy-ion and proton) test setup for two samples of the AD9361, according to [151].

Each DUT has a corresponding reference transceiver (*Ref TRX*) that allows the exchange of RF data. All receiver and transmitter chains (2RX2TX) are evaluated on-the-fly by a control software that either counts errors, performs recovery processes or can interrupt the irradiation beam line. Voltages and current values are digitized and captured by a *DAQ* module which provides these data to the control software.

5.2.3.3 Test procedure

Since long-term degradation is not expected during the SEE test campaign (except due to accumulated dose effects, primary by low-energy protons), detailed performance tests that were used in the TID test are not considered. More likely events are SEUs and MBUs in the configuration registers, SEFIs and potentially destructive events such as SELs or high-current states. The test procedure for both proton and heavy-ion tests is presented in Figure 5.30 on the following page.

Firstly, the DUT is initialized to a known configuration (fixed RX gain, TX attenuation, LO-frequency etc.). Once the DUT is configured and data exchange confirmed, the control software releases the beam of the accelerator. Current values are monitored

individually of the functional interactions and will shut down the beam once a current limit has been exceeded.

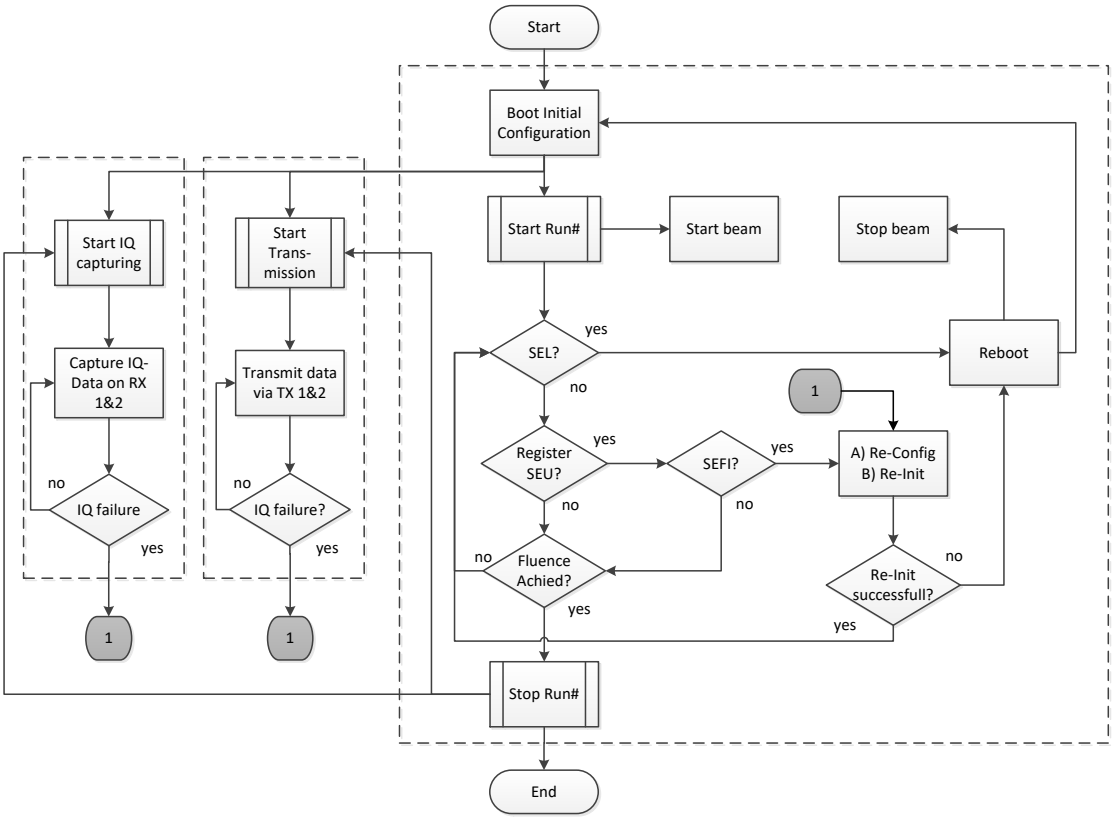


FIGURE 5.30: SEE (heavy-ion and proton) test procedure for the AD9361, according to [149, 151].

The control software continuously (once a second) reads and verifies (scrubs) the configuration registers (8-bit register map with addresses from $0x000_{Hex}$ to $0x3F6_{Hex}$) and counts the upsets. If an upset is observed, the DUT driver-related configurations (e.g. gain or attenuation values) are cross-checked by using the SPI interface. If a configuration change has occurred, the software first tries to re-write the initial values (*reconfiguration*). If the reconfiguration fails, a *re-initialization* is performed. The AD9361 has a dedicated input-pin for this purpose which needs to be triggered.

In case where the re-initialization fails, the setup (FPGA board or GSDR prototype) is rebooted. If one of the recovery actions was successful, the errors are counted and the run continues without any interruption of irradiation. The error classification for SEEs is organized as presented in Figure 5.31 on the following page. The real-time evaluation of transmitted and received RF data is essential and of primary interest since any type of classified SEFI could be observed within the baseband (IQ) data which may possibly not be recognized by driver-configuration verification as described above.

Thus, the IQ data evaluation runs in parallel and independent to the SEU and driver-related SEFI monitoring.

Furthermore, corruptions of such data are feasible, and these may not be related to the previously mentioned types of SEFI. Corruption of IQ data can be categorized into soft and hard IQ errors, according to the classification in Figure 5.31.

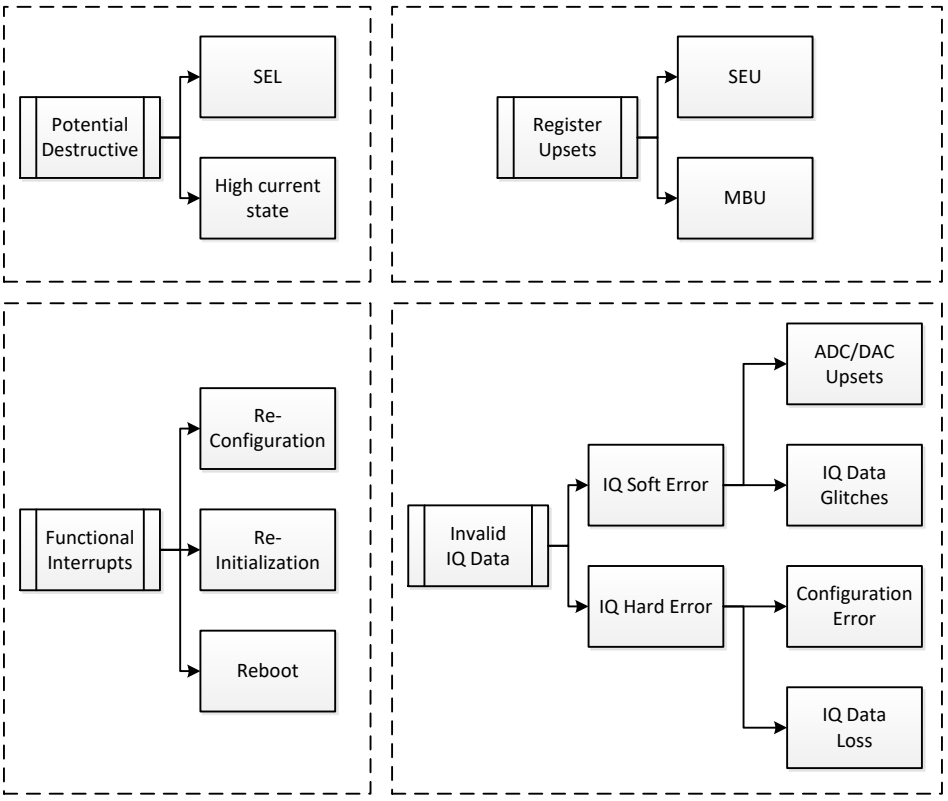


FIGURE 5.31: Error classification for the SEE test of the AD9361.

To accurately evaluate the IQ data, a sine-wave is used with a fixed amplitude and frequency. A reference curve is generated prior to transmission of data including boundaries for the amplitude (10 %) and tolerance of the sine-wave period (50 %).

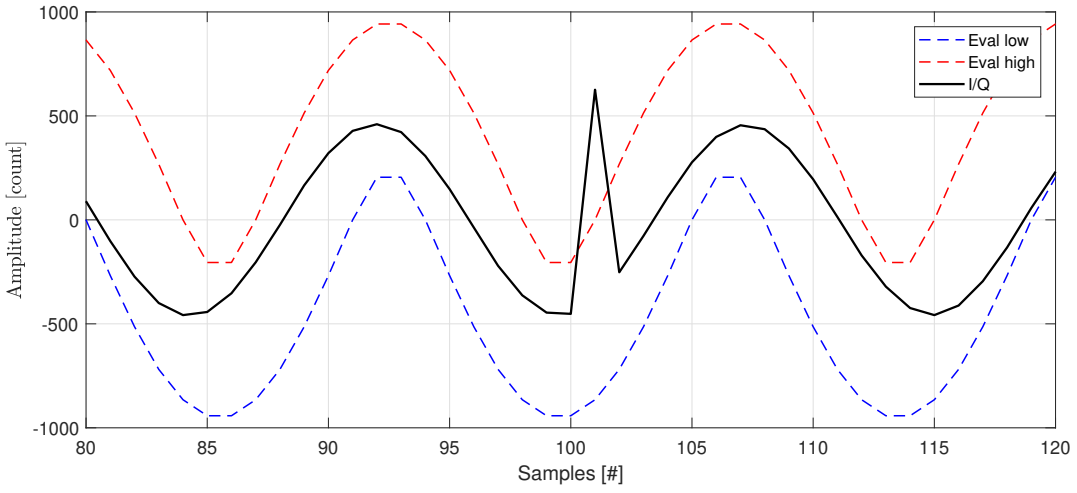
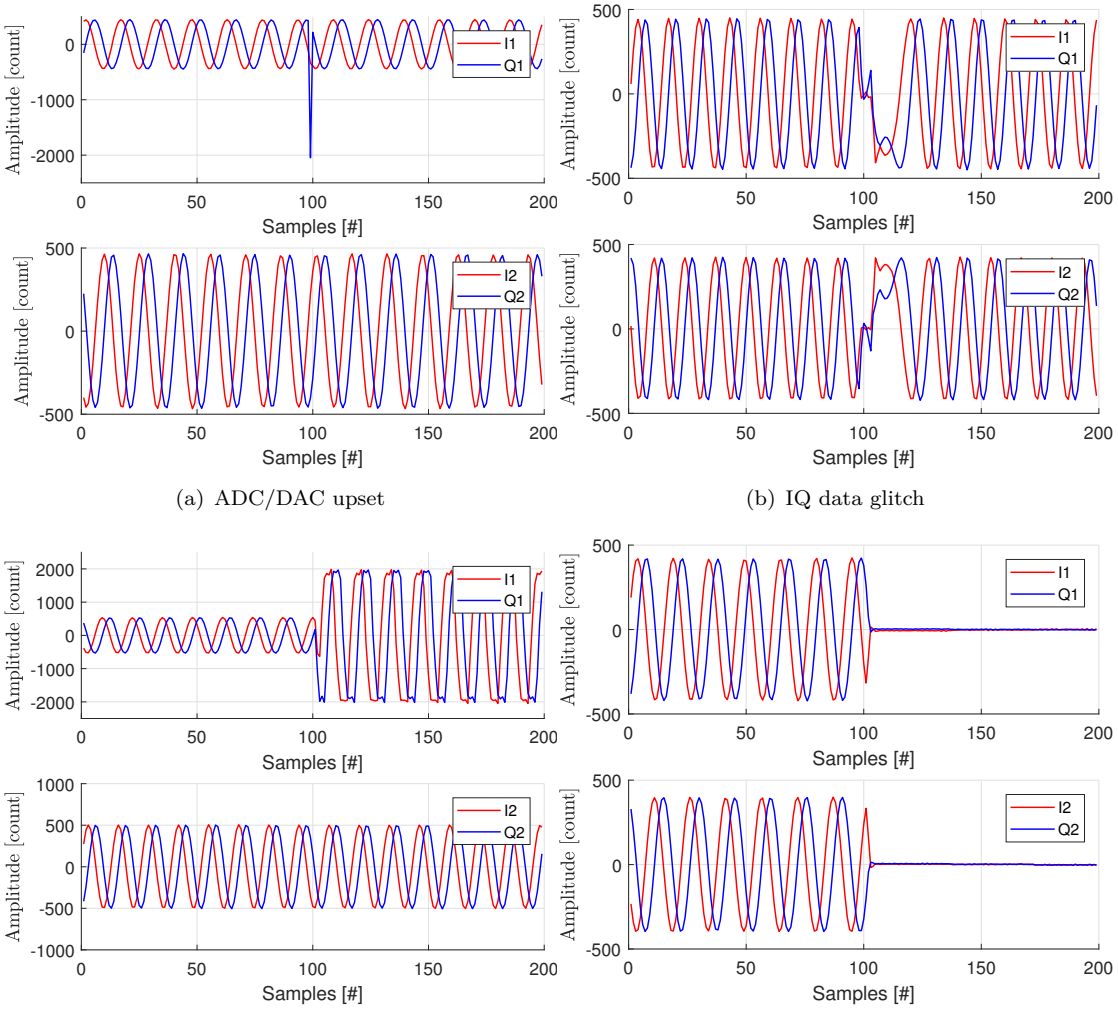


FIGURE 5.32: Reference curve with its evaluation boundaries for the in-phase/quadrature (IQ) baseband data validation with an ADC SEU as an example.

Quantization noise by the ADC is considered by accepting multiple zero-crossing of the sine-wave. An example for the reference curve with its upper and lower boundary and a corrupted data set of the IQ data (SEU in the ADC) is presented in Figure 5.32.

Expected IQ data errors are presented in Figure 5.33, including (a) ADC/DAC upset, (b) glitches in the IQ data that recover without interaction, (c) configuration error, and (d) loss of IQ data that represents a total loss of initial functions. Upsets in the ADC/DAC and glitches in the IQ data are sub-categorized as soft IQ errors. Configuration errors belong to hard IQ errors even if their impact may not be critical for some applications (e.g. a slight change in the receiver gain).



(a) ADC/DAC upset

(b) IQ data glitch

(c) Configuration error

(d) Loss of IQ data

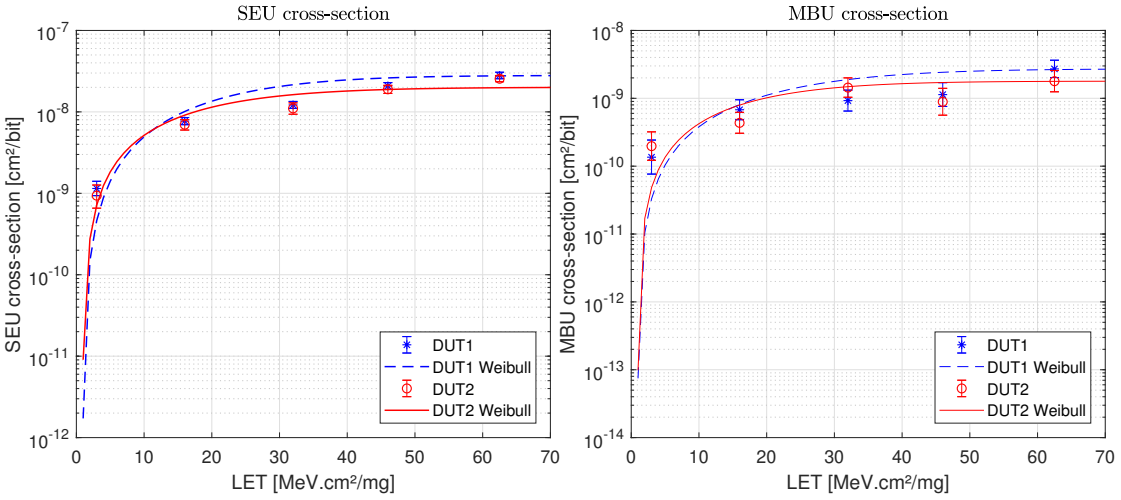
FIGURE 5.33: Classification and examples for invalid IQ data (a) ADC/DAC upset, and (b) IQ data glitches as sub-categories of soft IQ error, and (c) configuration error, and (d) loss of IQ data, as sub-categories of hard IQ errors.

5.2.3.4 Test results

Test results for the heavy-ion test and the proton test campaigns are presented in this section. Two DUTs are compared by their cross-sections for SEUs/MBUs, for driver-related SEFIs and errors in the IQ data. Error bars for uncertainties are presented according to equation 2.3 with a confidence-level of 95 %. Corresponding Weibull fitting curves are added which have been calculated using the OMERE software.

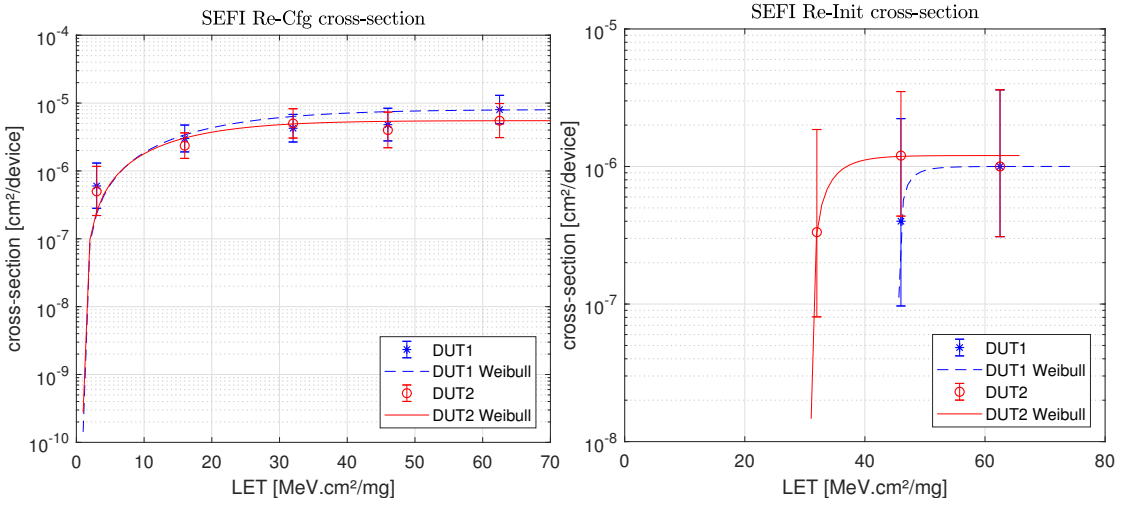
Heavy-ion test results

The cross-sections are presented in Figure 5.34 to 5.36 (according to [151]).



(a) SEU (b) MBU

FIGURE 5.34: Cross-section results for (a) SEU, and (b) MBU for both DUTs with the corresponding Weibull fitting (SEU: W=29.36 S=1.64; MBU: W=33.44 S=1.67).

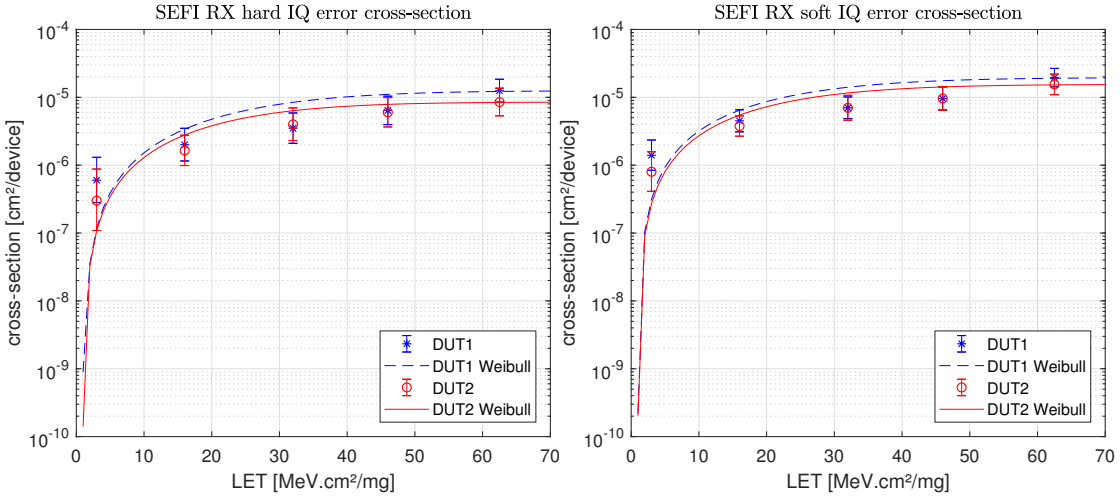


(a) Re-configuration (b) Re-initialization

FIGURE 5.35: Cross-section results for (a) reconfiguration, and (b) re-initialization with the corresponding Weibull fitting (hard: W=1.01 S=0.69; soft: W=27.09 S=1.45).

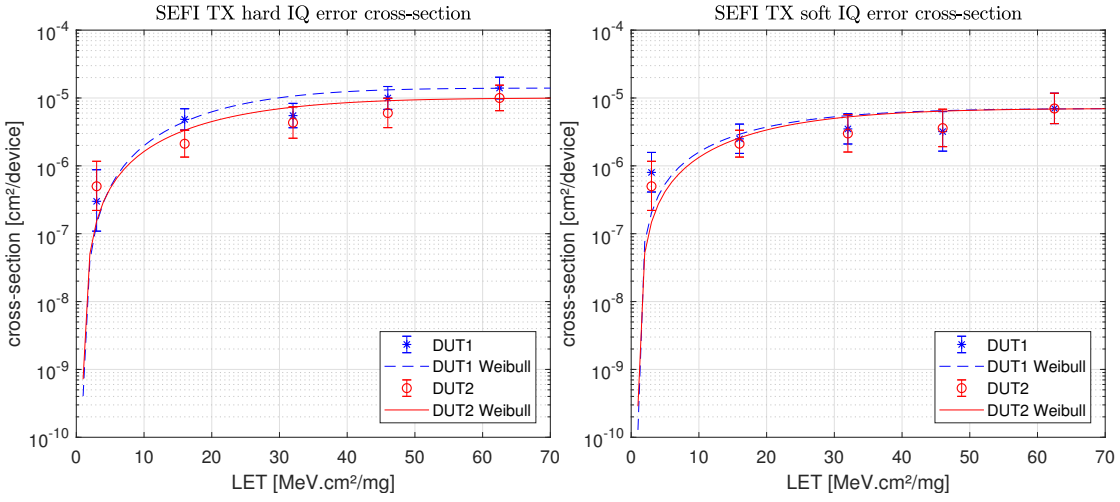
The cross-section test results for heavy-ion induced SEUs and MBUs are shown in Figure 5.34 and cross-sections for heavy-ion induced driver-related SEFIs which can either be recovered by reconfiguration or by re-initialization are presented in Figure 5.35.

The results for hard and soft errors observed in the IQ data are presented in Figure 5.36. IQ errors are separately detected on transmission and reception chains.



(a) Hard IQ error on RX

(b) Soft IQ error on RX



(c) Hard IQ error on TX

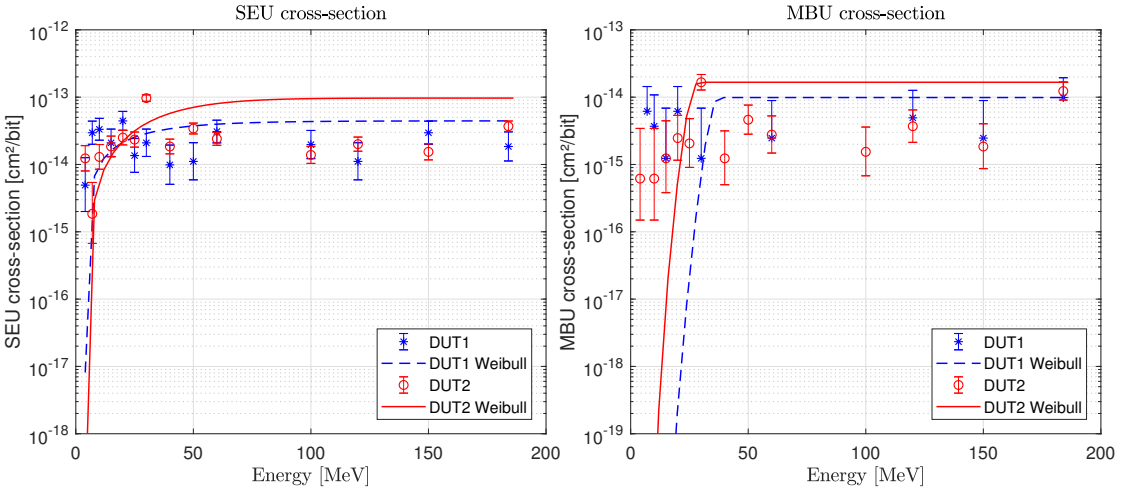
(d) Soft IQ error on TX

FIGURE 5.36: Cross-section results for IQ errors: (a) hard error on RX, (b) soft error on RX, (c) hard error on TX, and (d) soft error on TX with Weibull fitting.

Neither SELs nor other persistent malfunction or damages have been observed to an LET_{eff} of $125\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$. The test results are discussed in more detail in section 5.3.4.

Proton test results

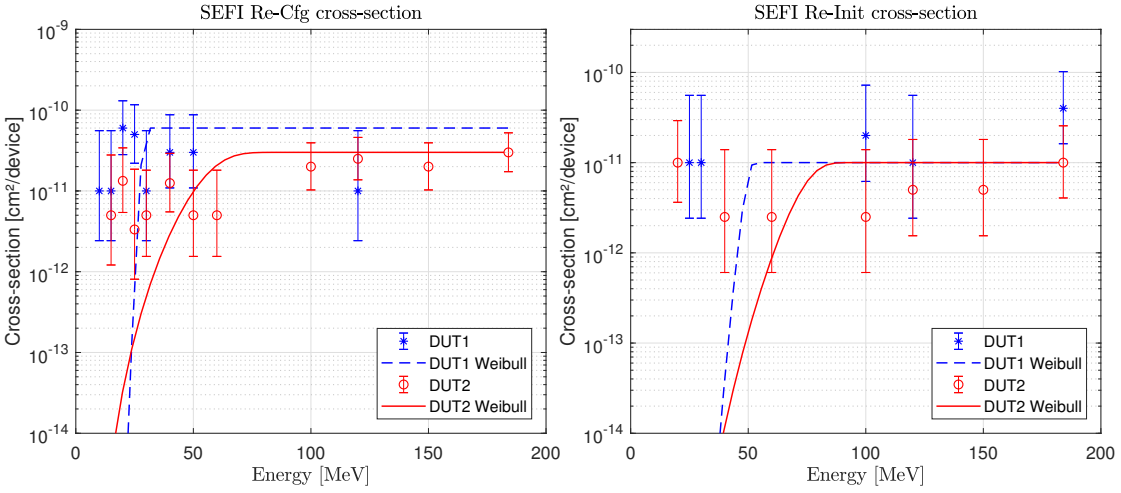
The cross-section results of SEU and MBU under proton irradiation are presented in Figure 5.37.



(a) SEU (b) MBU

FIGURE 5.37: Cross-section results for (a) SEU, and (b) MBU for both DUTs with the corresponding Weibull fitting curve (SEU: W=24.8 S=0.98; MBU: W=30.3 S=16.2, according to [149].

The results for functional interruptions (SEFIs) are presented in Figure 5.38.

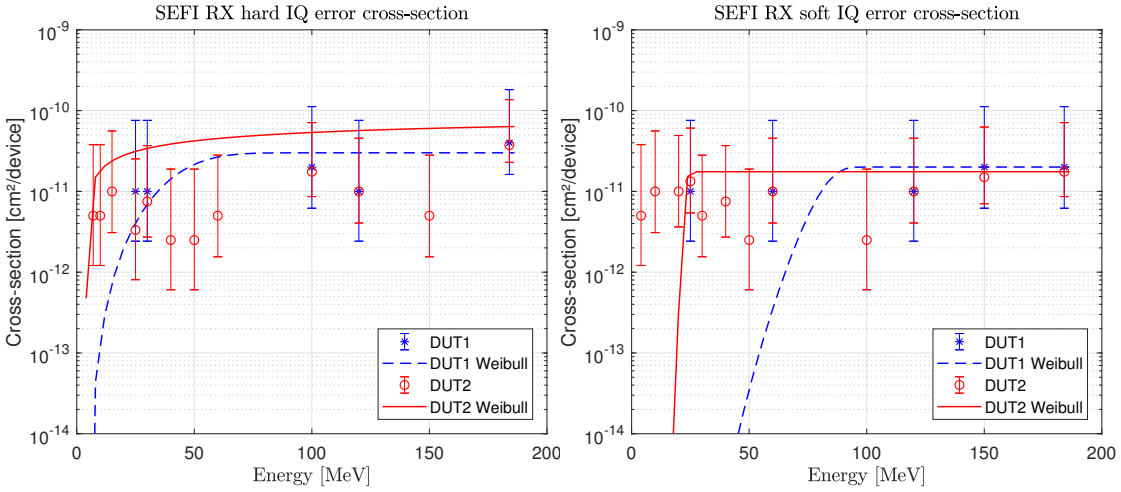


(a) Re-configuration (b) Re-initialization

FIGURE 5.38: Cross-section results for (a) reconfiguration and, (b) re-initialization for both DUTs with the corresponding Weibull fitting curve (Cfg: W=24.5 S=29; Init: W=67.8 S=13.2), according to [149].

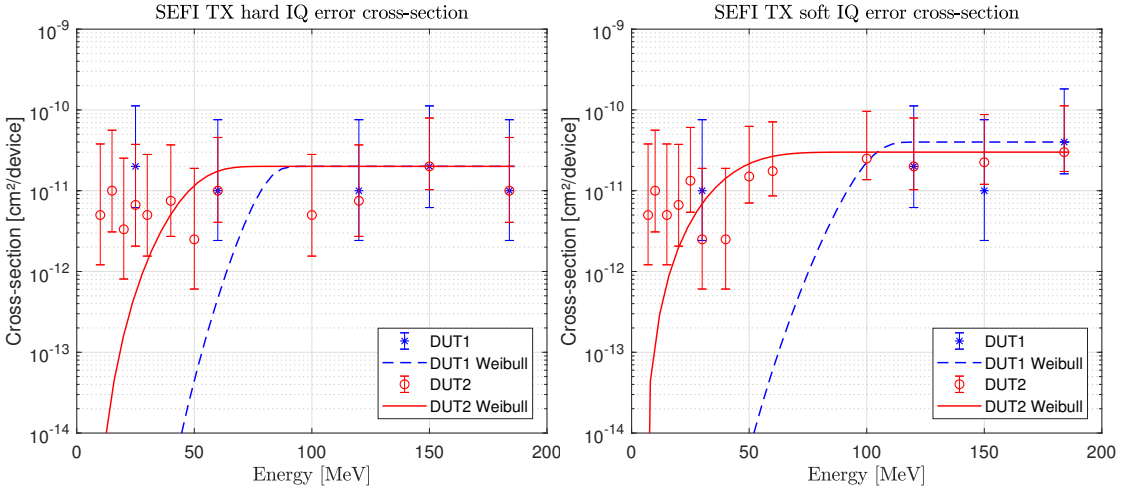
Hard and soft errors in the IQ data were observed rarely. The cross-section results for different kinds of IQ error on TX and RX are presented in Figure 5.39 on the following

page for both DUTs. It should be mentioned that the target fluence of DUT2 was 2-4 times higher than for DUT1 and thus a higher quantitative number of errors were measured. Thus, the energy threshold of both DUTs differs.



(a) Hard IQ error on RX

(b) Soft IQ error on RX



(c) Hard IQ error on TX

(d) Soft IQ error on TX

FIGURE 5.39: Cross-section results for IQ errors: (a) hard error on RX, (b) soft error on RX, (c) hard error on TX and, (d) soft error on TX, for both DUTs with the corresponding Weibull fitting curve (W≈80; S≈11).

As for heavy-ions, no destructive events such as SELs were observed during all test runs and selected proton energies. The proton test results are discussed in more detail in section 5.3.4.

5.3 Discussion

In this section, the previously presented test results for critical COTS devices in the GSDR system design are discussed. Results are summarized and error rate predictions on two reference missions (15 years GEO and two years in LEO, 98 ° and 800 km altitude) are performed for the Zynq, NAND, DDR3 and RFIC to interpret their potential risk based on the evaluated radiation effects and their criticality under worst-case conditions. Specifically the results of the AD9361 are highlighted and discussed in deeper detail.

5.3.1 Zynq-7000

Based on the published results that were referenced and presented in section 5.1.1, the following assumption can be made. As described in [133], the Zynq is sustainable to TID levels of up to 170 krad before functional interrupts were observed. Annealing effects under room and elevated temperatures were observed and functional interrupts should to be healed. Most importantly, the Zynq-7000 did not show any persistent destructive damage. The SEL phenomena observed on the auxiliary voltage supply is fairly slow and a current limitation can be applied to avoid destructive effects. Event rate predictions of [104] show that SELs may occur every 30 years (9.2×10^{-5} /device/day) assuming a GEO mission during solar minimum conditions and 100 mils aluminum shielding. For the LEO mission, the event rate is expected to be much lower. Further error rate determinations were performed using OMERE and are presented in Table 5.3.

Table 5.3: Predicted event rates for the Zynq-7000 using OMERE [32] and [107].

SEE Type	**Orbit**	**LET threshold [MeV·cm²/mg]**	**Limit cross-section [cm²/bit;dev]**	**Events/day (nominal)**	**Events/day (worst)**
SEL	GEO	$1.23 \times 10^{+1}$	2.98×10^{-4}	5.02×10^{-5}	5.66×10^{-3}
SEL	LEO	$1.23 \times 10^{+1}$	2.98×10^{-4}	2.01×10^{-5}	1.41×10^{-3}
CRAM	GEO	1.00×10^{-3}	1.60×10^{-9}	1.36×10^{-8}	3.23×10^{-6}
CRAM	LEO	1.00×10^{-3}	1.60×10^{-9}	1.04×10^{-8}	7.67×10^{-7}
BRAM	GEO	1.00×10^{-3}	5.31×10^{-9}	2.37×10^{-8}	5.80×10^{-6}
BRAM	LEO	1.00×10^{-3}	5.31×10^{-9}	1.83×10^{-8}	1.38×10^{-6}
OCM	GEO	1.00×10^{-3}	2.40×10^{-9}	4.96×10^{-8}	1.38×10^{-5}
OCM	LEO	1.00×10^{-3}	2.40×10^{-9}	4.34×10^{-8}	3.26×10^{-6}
Sobel	ISS	-	6.61×10^{-9}	-	1.2×10^{-2}
Processor	ISS	-	5.70×10^{-9}	-	1.4×10^{-2}

The most important information that can be extracted from these radiation test results is that the shared memory being used between the PS and PL plays an essential role in terms of radiation effects. The BRAM cross-section is five times higher than the CRAM

cross-section and about two times higher than for the OCM cross-section. Moreover, the sustainability of the ARM processor has been demonstrated to be dependent on the enabled caches [132, 158]. If process execution time is not an issue (for example on real-time operations), disabling certain caches (especially L2) could significantly reduce susceptibility to SEEs and thus improve system reliability. However, it is also important to examine fully operated systems that are running on the Zynq as presented by [107]. For sure, the error rates are much higher than for SEUs in the memories, but in many applications/missions a reset or reboot are tolerated if they do not occur too frequently. In the example of [107], the days until failures on ISS is about 83 days until the Sobel algorithm fails and 71 days until the filesystem/processor crashes.

Criticality analysis

To determine the CN, the predicted event rates (worst) are used for the Zynq as presented in Table 5.3. The probability depends on the suggested environment and for the criticality analysis the two previously mentioned missions (LEO and GEO) are used as a reference. The results are presented in Table 5.4.

TABLE 5.4: FMECA criticality analysis on the Zynq-7020 as device for the BBP.

ID	Orbit	Failure causes	Failure effects	SN	PN	DN	CN
BBP.1	LEO	SELs or high current states	permanent loss of system functionality	3	1	2	6
BBP.1	GEO			3	2	2	12
BBP.2	LEO	TIDs, long-term degradation	permanent loss of system functionality	3	1	2	6
BBP.2	GEO			3	2	2	12
BBP.3	LEO	SHEs, non-recoverable state	permanent loss of system functionality	3	0	-	0
BBP.3	GEO			3	0	-	0
BBP.4	LEO	SEFIs, recoverable state	temporary loss of system functionality	2	3	3	18
BBP.4	GEO			2	3	3	18
BBP.5	LEO	SEU/MBU/SEFIs, OS crash	temporary loss of system functionality	2	3	3	18
BBP.5	GEO			2	3	3	18
BBP.6	LEO	SEU/MBU/SEFIs, SW thread/process crash	temporary loss of system-parts functionality	1	3	3	9
BBP.6	GEO			1	3	3	9
BBP.Total			**Average CN (LEO):**				**9.5**
BBP.Total			**Average CN (GEO):**				**11.3**

As known from the referenced radiation test results of the Zynq, SELs were observed but only on the auxiliary voltage supply rail and with a slow time increment. The

predicted event rates show that it takes over hundreds of days, during that a potential SEL may occur. Moreover, current limiters on the voltage supply could handle such effects (DN=2). Thus, resulting CN is fairly low for SELs. TID is not an issue for both LEO and GEO (TID: 170 krad(SiO_2)) and can be improved by shielding (DN=2). SHEs have never been observed and are thus not expected. SEU cross-sections (cm^2/bit) in the shared memories are fairly low but directly affect the SEFIs that are more likely and thus related with much higher probability numbers. A scrubbing mechanism of the memory could be applied to identify SEUs but may not be very efficient due to time constraints (DN=3). Watchdog devices can detect system crashes (SEFI) and reset the system to a valid state (DN=2). Single processes or threads that fail may occur similar to total system crashes but have a less SN. Such failures can be detected and partially corrected (DN=3). Assuming the individual failures and the total number and average of CN, the Zynq is acceptable for use.

5.3.2 NAND flash

The radiation test results of the desired NAND flash were set out in section 5.1.2. According to Oldham et al. [115], the 8 Gbit Micron flash showed no malfunctions and only a very few bit errors up to a total dose of 75 krad(SiO_2). No significant variations from lot-to-lot or device-to-device have been recorded. These doses are usually achieved at about 10 years in LEO (98 °, 800 km) assuming ≈2 mm aluminum shielding (see Figure 5.18) or in a 15-year GEO mission (≈6 mm aluminum shielding). SELs were never observed. However, high current spikes have been monitored during dynamic operations, especially when intensively using the write and erase functions. These high current spikes have been found to potentially cause critical damage and could lead to irreversible destructive failures.

Nevertheless, Table 5.5 on the following page which shows the predicted event rates for different errors at two reference orbits, destructive failures may occur only every eight years in LEO or every two years in GEO, respectively.

In terms of floating gate errors, the SEU cross-section is quite small, especially if ECC is enabled. It is assumed by [114] that the bit errors forming the SEU cross-section could be fully corrected by enabling ECC. However, the evaluation of static (*) and dynamic SEU-tests with an enabled ECC mechanism has not been studied so far. SEFIs on the other hand are of greater concern. It has been found that SEFIs typically occur when the control circuit and logic are affected by an incident particle. As a result, the entire memory or at least a large part of it fails, especially in the write and erase operations, but this could be generally recovered by a reset or power-cycle. Nevertheless, the event rate for SEFIs may be fair enough to handle, especially if the device is primarily being used for reading operations to load sensitive data for the boot mechanism.

TABLE 5.5: Predicted event rates for the NAND flash using OMERE [32].

SEE Type	**Orbit**	**LET threshold [MeV·cm²/mg]**	**Limit cross-section [cm²/bit;dev]**	**Events/day (nominal)**	**Events/day (worst)**
DF	GEO	$2.57 \times 10^{+1}$	1.00×10^{-4}	1.83×10^{-5}	1.38×10^{-3}
DF	LEO	$2.57 \times 10^{+1}$	1.00×10^{-4}	5.47×10^{-6}	3.58×10^{-4}
SEU	GEO	$9.98 \times 10^{+0}$	4.23×10^{-13}	1.24×10^{-18}	1.23×10^{-16}
SEU	LEO	$9.98 \times 10^{+0}$	4.23×10^{-13}	3.29×10^{-19}	3.26×10^{-17}
SEU*	GEO	$9.98 \times 10^{+0}$	2.18×10^{-12}	1.46×10^{-17}	1.45×10^{-15}
SEU*	LEO	$9.98 \times 10^{+0}$	2.18×10^{-12}	3.87×10^{-18}	3.85×10^{-16}
$SEFI_r$	GEO	1.00×10^{-3}	1.00×10^{-3}	1.53×10^{-2}	$3.27 \times 10^{+0}$
$SEFI_r$	LEO	1.00×10^{-3}	1.00×10^{-3}	8.32×10^{-3}	7.59×10^{-1}
$SEFI_{rw}$	GEO	1.00×10^{-3}	1.10×10^{-3}	2.80×10^{-2}	$5.66 \times 10^{+0}$
$SEFI_{rw}$	LEO	1.00×10^{-3}	1.10×10^{-3}	1.44×10^{-2}	$1.32 \times 10^{+0}$

*static

Criticality analysis

Table 5.6 shows the criticality determinations for worst-case conditions of the chosen NAND flash. The PN is derived from the radiation test results and predicted event rates presented in Table 5.5.

TABLE 5.6: FMECA criticality analysis on the NAND flash as static memory resources device.

ID	**Orbit**	**Failure causes**	**Failure effects**	**SN**	**PN**	**DN**	**CN**
$MEM_S.1$	LEO	SELs or high current states	permanent loss of system functionality	3	2	3	18
$MEM_S.1$	GEO			3	2	3	18
$MEM_S.2$	LEO	TIDs, long-term degradation	permanent loss of system functionality	3	1	2	6
$MEM_S.2$	GEO			3	2	2	12
$MEM_S.3$	LEO	SHEs, non-recoverable cell	permanent loss of system functionality	3	1	2	6
$MEM_S.3$	GEO			3	2	2	12
$MEM_S.4$	LEO	SEUs/MBUs recoverable state change	temporary loss of system functionality	2	2	1	4
$MEM_S.4$	GEO			2	2	1	4
$MEM_S.5$	LEO	SEFIs, recoverable functional interrupt	temporary loss of system functionality	3	4	1	12
$MEM_S.5$	GEO			3	4	1	12
MEM_S.Total			**Average CN (LEO):**				**9.2**
MEM_S.Total			**Average CN (GEO):**				**11.6**

Even if SELs were not directly observed, destructive events due to high current spikes may occur even if these events are unlikely. With proper current limiters which need to be applied carefully to avoid functional distortions, DF could be mitigated (DN=3). For TID the CN is lower on LEO missions compared to GEO due to the total dose achieved. Shielding plays an essential role and could reduce the risk for such expected failures (DN=2). Stuck-bits are not very likely and are in general not critical since the device holds enough memory for backup partitions and can be read out (DN=2). The PN differs between both types of mission since heavy-ion particles may cause such events and is more dominating in GEO. SEFIs are much more likely (PN=4) under worst-case conditions) but due to available recovery processes by continuous scrubbing of the content and the low memory allocation (DN=1). The CN reduces (Max. 18; Avg. 9.2 and 11.2) and the 8 Gbit NAND flash device is acceptable for use.

5.3.3 DDR3-SDRAM

Two potential devices from the same manufacturer (Micron 2 Gbit and 4 Gbit density) have been evaluated under radiation and the results were presented in section 5.1.3. For the 2 Gbit device, TID has been found to be not an issue since the devices showed no malfunction and only a few bit errors under biased and unbiased conditions up to dose levels of 400 krad(SiO_2). The 4 Gbit DDR3-SDRAM, however, showed an increased idle current starting at about 50 krad(SiO_2). At 90 krad(SiO_2) the first bit errors were noticed and these increased according to the idle current. It is assumed that the increased error density is caused by increased current that leads to a drop in the supply voltage that falls below the device specification [143].

TABLE 5.7: Predicted event rates for the DDR3-SDRAM using OMERE [32].

SEE Type	**Orbit**	**LET threshold [MeV·cm²/mg]**	**Limit cross-section [cm²/bit/dev]**	**Events/day (nominal)**	**Events/day (worst)**
SEU	GEO	$1.20 \times 10^{+1}$	9.01×10^{-11}	7.15×10^{-15}	7.19×10^{-13}
SEU	LEO	$1.20 \times 10^{+1}$	9.01×10^{-11}	1.90×10^{-15}	1.91×10^{-13}
$SEFI_{row}$	GEO	$1.20 \times 10^{+1}$	3.80×10^{-3}	2.06×10^{-2}	3.53×10^{-0}
$SEFI_{row}$	LEO	$1.20 \times 10^{+1}$	3.80×10^{-3}	1.05×10^{-2}	8.28×10^{-1}
$SEFI_{col}$	GEO	$1.18 \times 10^{+1}$	1.20×10^{-3}	4.57×10^{-3}	8.04×10^{-1}
$SEFI_{col}$	LEO	$1.18 \times 10^{+1}$	1.20×10^{-3}	2.57×10^{-3}	1.90×10^{-1}
$SEFI_{rw}$	GEO	$1.99 \times 10^{+0}$	9.99×10^{-6}	4.76×10^{-5}	9.16×10^{-3}
$SEFI_{rw}$	LEO	$1.99 \times 10^{+0}$	9.99×10^{-6}	3.08×10^{-5}	2.19×10^{-3}

Under particle irradiation, the devices did not shown any destructive events such as SELs or irreversible SEFIs. The most common failures that occur besides SEUs are SEFIs organized in rows and columns that cause hundreds of accumulated bit-errors. For such

SEFIs, particles affect the control circuit without a loss of the device functionality such as is classified for device SEFIs. Lot-to-lot or device-to-device variations have not not been mentioned in the test reports. Since heavy-ion test data is more reliable, the 2 Gbit device is preferred. Table 5.7 on the previous page shows the predicted event rates for the previously cited GEO and LEO reference missions.

Device SEFIs have the highest impact on the system reliability and require a reset to recover nominal functionality. According to the event rate prediction, such events are expected less than once a year for LEO missions and about every 100 days in GEO. Row and column SEFIs will occur much more often (multiple times per day) but since only a minor part of the memory resource is allocated by the application or OS it is not extremely likely to fail. Thus, lower event rates are expected. Additionally, ECC can be enabled which has not been investigated in the referenced studies. However, other mitigation strategies for DDR3-SDRAMs can be applied as discussed by [144]. The software conditioning (SC) being used has proven to reduce the SEFI cross-section significantly. Column SEFIs have been completely removed and row SEFIs' cross-section decreased by an order of two. Furthermore, device SEFIs are also improved by SC.

Criticality analysis

In table 5.8 the criticality determination for the selected 2 Gbit DDR3-SDRAM is presented for the LEO and GEO reference missions. The probability of (worst) expected events occurring is also derived from the predicted event rates presented in Table 5.7.

TABLE 5.8: FMECA criticality analysis on the DDR3-SDRAM device.

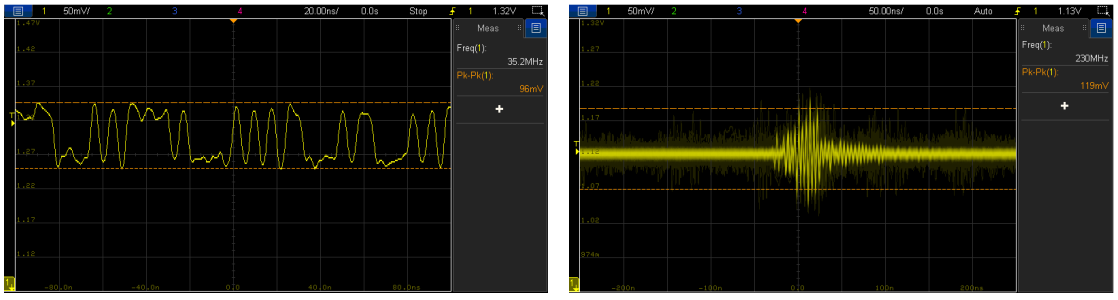
ID	Orbit	Failure causes	Failure effects	SN	PN	DN	CN
$MEM_D.1$	LEO	SELs or high current states	permanent loss of system functionality	3	0	-	0
$MEM_D.1$	GEO			3	0	-	0
$MEM_D.2$	LEO	TIDs, long-term degradation	permanent loss of system functionality	3	1	2	6
$MEM_D.2$	GEO			3	2	2	12
$MEM_D.3$	LEO	SHEs, non-recoverable cell	permanent loss of system functionality	3	0	-	0
$MEM_D.3$	GEO			3	0	-	0
$MEM_D.4$	LEO	SEUs/MBUs recoverable state change	temporary loss of system functionality	2	2	2	8
$MEM_D.4$	GEO			2	2	2	8
$MEM_D.5$	LEO	SEFIs, recoverable functional interrupt	temporary loss of system functionality	2	4	1	8
$MEM_D.5$	GEO			2	4	1	8
MEM_D.Total			**Average CN (LEO):**				**4.4**
MEM_D.Total			**Average CN (GEO):**				**5.6**

Destructive events, such as SELs or irreversible SEFIs, were not observed for any conducted and referenced radiation test, nor SHEs. Thus, the corresponding CN is zero. TID has been shown to be less critical due to the resistance of $\geq 400\,\mathrm{krad(SiO_2)}$. This value is suitable for both types of reference mission and this could be mitigated by shielding (DN=2). The SEU cross-section ($\mathrm{cm^2/bit}$) is quite low and less critical especially since only a small part of the memory is being used and ECC can be applied. The most likely failures are SEFIs in the control logic of the devices resulting in a temporary loss of system functionality. However, SC has been shown to be very efficient (DN=1) and can be used in order to reduce the CN significantly. The final determined CN (Max. 12; Avg. 4.4 and 5.6) is low and the overall useability is acceptable for the selected device.

5.3.4 AD9361

5.3.4.1 TID Effects

Section 5.2.2 gave the test procedure and test results of the AD9361 on TID effects. Two DUTs were exposed to γ-rays and another two DUTs to x-rays up to a dose level of $70\,\mathrm{Mrad(SiO_2)}$. Due to the complex structure of the AD9361 and the numerous types of functionality, a common test methodologies were not applicable, so it was necessary to develop a unique test procedure and setup. The results presented do not show any noticeable degradation effects. However, it must be mentioned that the applied test setup was not able to provide measurement accuracies that could be achieved with high-quality equipment such as signal analyzers. Nevertheless, from a qualitative perspective, the designed test setup and procedure enables robust and accurate statements to be made about. For extremely high dose levels on x-ray exposure, both DUTs have shown a loss of function at about $45\,\mathrm{Mrad(SiO_2)}$.



(a) LVDS signal prior to irradiation (b) LVDS signal after irradiation

FIGURE 5.40: Measurement in the LVDS data lines (a) prior to irradiation and, (b) after irradiation, according to [157].

Further investigation and analysis of the data resulted in failure in the digital timing calibration. This led to an error in the device calibration and a non-operable state. However, the device was partially able to configure and it is assumed that the error occurs

in the digital data interface. Measurements of the LVDS data lines verify this assumption since the signals are fully corrupted as presented in Figure 5.40 on the previous page. However, after annealing at ambient and elevated temperature, a recovery of the device functionality has been observed and a persistent degradation of the device performance was not noticed. However, dose rates of such levels are extremely high and a great deal above what is to be expected in any kind of satellite mission. Thus, TID is not an issue.

5.3.4.2 Single event effects

Even if the AD9361 has been proven to be very resistant to total dose effects, it has been shown in the test results that particle irradiation could cause several types of event. Similar to the test procedures for TID, a common test methodology is not applicable due to the complex device architecture. The design of the unique test setup and procedure for evaluating the SEE response of the DUT has been presented in section 5.2.3 and cross-section results were shown according to proton and heavy-ion irradiation. The most important remark is that neither SELs nor other destructive events have been observed that lead to a persistent loss of function of the AD9361. The following part of this section discusses the results and different observed phenomena and error-dependencies.

Ratios of classified errors

As mentioned in the error classification in Figure 5.31, several types of SEE are expected and are more or less independently monitored. However, especially SEUs in the configuration registers may have a direct impact on the function of the device and may also cause classified SEFIs. In Table 5.9, a ratio of SEUs to SEFIs is presented for DUT1.

Table 5.9: SEU to SEFI ratio on DUT1.

LET [MeV.cm^2/mg]	**Re-Cfg** [%]	**Re-Init** [%]	**IQ**$_{RX}$ [%]	**IQ**$_{TX}$ [%]	**IQ**$_{total}$ [%]
3	6.45	0	15.05	9.67	24.72
16	4.37	0.26	9.25	7.46	16.71
22.63	4.80	0.00	7.20	9.33	16.53
32.00	4.17	0.00	9.09	12.12	21.21
45.25	4.30	0.00	7.09	7.85	14.94
46.00	3.87	0.55	8.01	5.25	13.26
62.50	3.52	0.44	8.59	8.37	16.96
62.90	2.84	0.24	5.69	7.35	13.04
Average	**4.29**	**0.19**	**8.75**	**8.42**	**17.17**

Similar results are observed for DUT2. On average about 5 % of SEUs cause a SEFI that was able to be recovered by a driver-related reconfiguration. The correlation of SEUs that required re-initialization when the reconfiguration fails is less than 1 %. Nevertheless, in 95.5 % of all driver-detected SEFIs, a simple reconfiguration was successful

and in about 4.5 % of all cases a re-initialization was required and successfully attained a recovered function. In none of the test runs was a reboot of the entire setup required. Looking at the detected IQ failures one can see that there is a closer relationship. Including all types of IQ failure (hard and soft), around 17 % of them may be related to faults in the configuration registers caused by SEUs or MBUs. The relationship for IQ failures in terms of hard to soft errors and between receiver and transmitter is presented in Table 5.10.

TABLE 5.10: SEU to IQ failure ratio on DUT1.

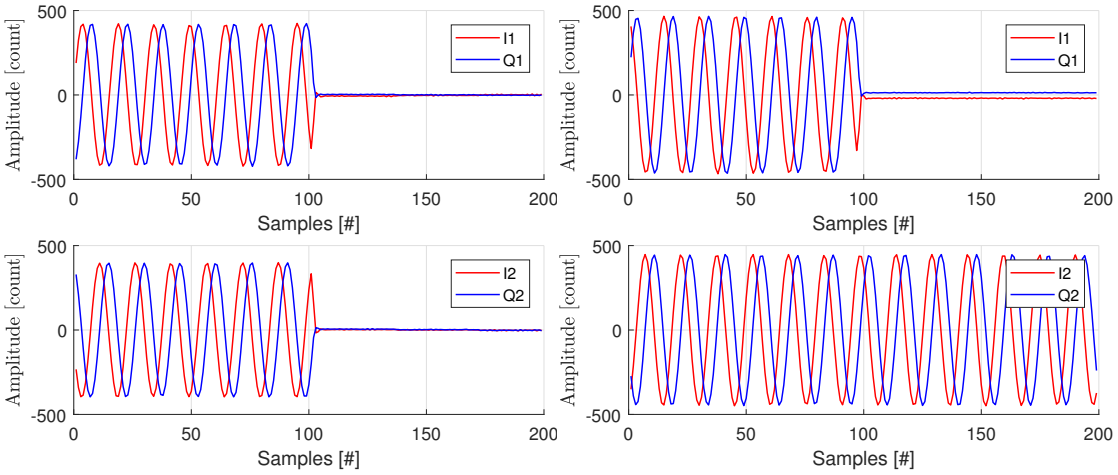
LET [MeV.cm^2/mg]	**Hard** [%]	**Soft** [%]	**Hard**$_{RX}$ [%]	**Hard**$_{TX}$ [%]	**Soft**$_{RX}$ [%]	**Soft**$_{TX}$ [%]
3	80.96	19.04	71.14	42.86	66.67	33.33
16	46.62	53.38	75.00	25.00	43.90	56.10
22.63	41.23	58.77	71.43	28.57	29.27	70.73
32.00	38.00	62.00	75.00	25.00	30.00	70.00
45.25	48.17	51.29	60.87	39.13	38.89	61.11
46.00	60.00	40.00	66.67	33.33	55.56	44.44
62.50	38.64	61.36	58.33	41.67	47.17	52.83
62.90	38.55	61.45	57.14	42.86	39.02	60.98
Average	**49.09**	**50.91**	**65.20**	**34.80**	**43.81**	**56.19**

In general, the ratio of observed IQ failures is more or less equal for hard and soft errors. This includes errors on both RX and TX. Comparing the hard and soft IQ errors on the receiver and transmitter side, a few more failures were monitored on the receiver-considered hard errors, whereas on the TX the soft errors have a slightly higher ratio. It is assumed that the ratio also follows an equal distribution if an infinite irradiation time is considered. However, the results do not clearly show that either the RX or TX part is more affected. The almost equal behavior can be an indicator that the internal control logic, specifically the synthesizer, might be affected by irradiation, a point which is analyzed and discussed in more detail in the next part.

Potential synthesizer failure

The integrated synthesizer circuit which is supported by the external (crystal) oscillator is responsible for the overall clock distribution, including the generation of the baseband frequency, to drive the ADC/DAC, the LO and other internal functions. According to the IQ data evaluation, it is feasible to observe functional interrupts on the synthesizer circuit if IQ failures are monitored. An example how IQ data will look like in case that the synthesizer may be affected by radiation is presented in Figure 5.41 (a) on the following page. In this case, the IQ data fully disappears on both channels for the receiver (I1,Q1 and I2,Q2) at the same time. Analyzing the IQ data shows that in about 31 % of all hard IQ errors, these may be caused by those types of synthesizer SEFIs. However, as can be seen in Figure 5.41 (b), it is also possible that only one of each

of the channels showed a corrupted data set. As for any kind of hard IQ failure, a re-initialization of the devices is required to recover to nominal function.



(a) Synthesizer error (b) No synthesizer error

FIGURE 5.41: IQ data set that indicates potential synthesizer errors with (a) synthesizer error and, (b) no synthesizer.

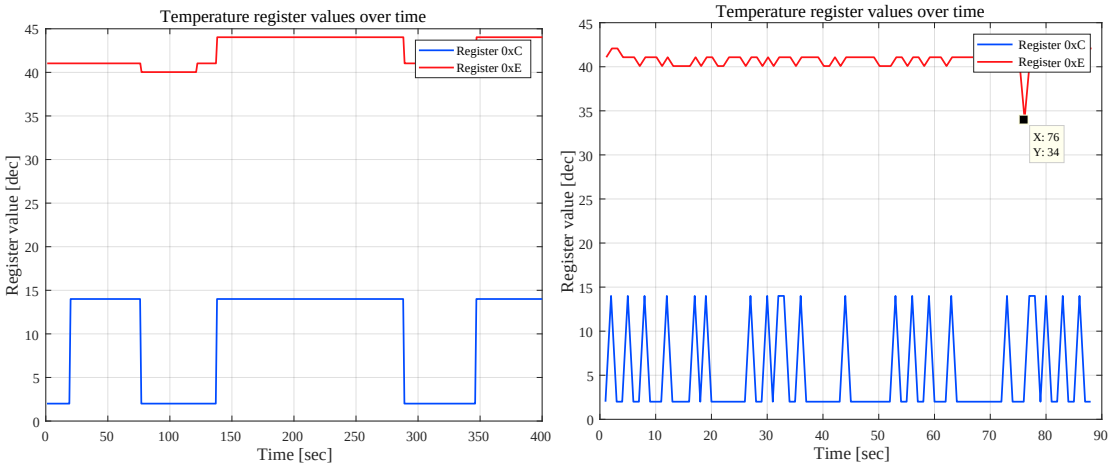
Looking more closely at the IQ failures, it has been found that about 12 % of the total number of hard IQ failures (TX and RX) can been correlated to driver-related reconfiguration processes. About 82 % of the hard IQ failures were not detected by the desired self-recovery methodology and a re-initialization was required.

IQ Data glitches, categorizes to the soft IQ failures, were observed on all channels at the same time (Figure 5.33 (b)). Thus it is very likely that these failures were also caused by the synthesizer. A possible explanation may be SETs that appear in or by the synthesizer. Another reason for the observed glitches and their quick self-recovery is that the integrated control circuit continuously performs functional checks and carries out instantaneous re-calibrations without external interaction. For soft IQ failures, about 93 % were short-termed glitches that recovered back to the intended waveform after a few samples, as shown in Figure 5.33 (b). The other 7 % of soft IQ failures are correlated SEUs in the ADC or DAC as shown in 5.33 (a).

SEU behavior and propagation

As mentioned previously, the impact of SEUs on the functional registers will cause SEFIs that are either recoverable by driver-interaction or which lead to corruption of transmitted or received data (IQ failures). For the scrubbing process of the registers to observe SEUs or MBUs, certain registers were required to mask out of the scrubbing process since they continuously change their state even without a particle interaction. Such registers are related for example to functions such as the integrated temperature sensors, the internal calibrations as well as self-checks (e.g. tuning the AGC based on the evaluated and measured RSSI).

About 6 % of the register map has been found to be taken out of the scrubbing mechanism. Nevertheless, it is also possible that those registers and the corresponding function may be affected by an incident particle and these could cause failure interruptions or false states, as shown as an example for the temperature in Figure 5.42.



(a) Nominal temperature registers

(b) SEU in temperature registers

FIGURE 5.42: SEU in masked-out registers during irradiation showing nominal behavior of the temperature registers (a) and a non-persistent SEU (b), according to [149].

Furthermore, it has been found that functional registers have dependencies on each other, meaning that if a single state in a certain register changes, further registers will alter too. This could lead to an avalanche effect resulting in multiple changes of register states but usually not causing an alternation in the functionality if the initial affected register does not affect any important function of the devices.

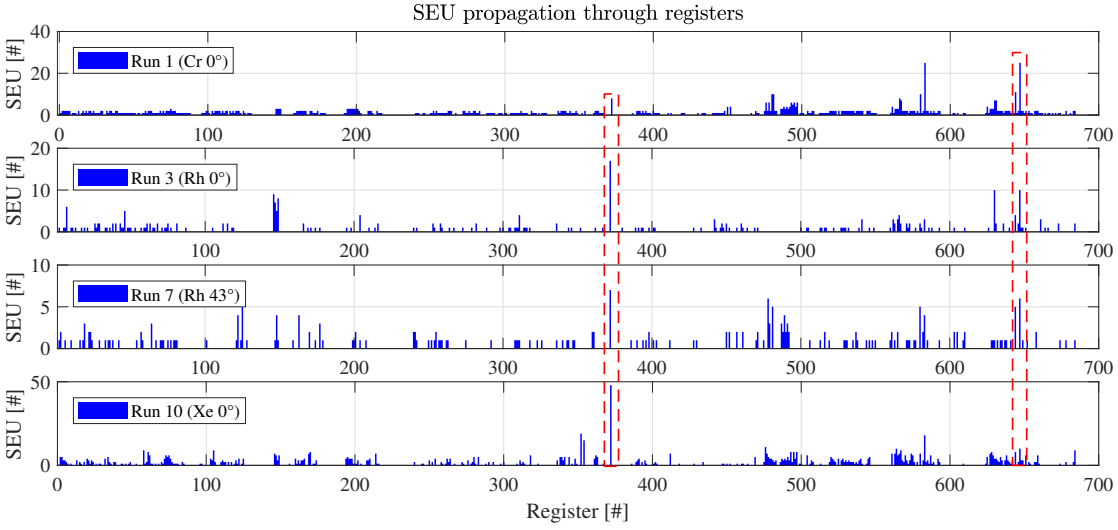
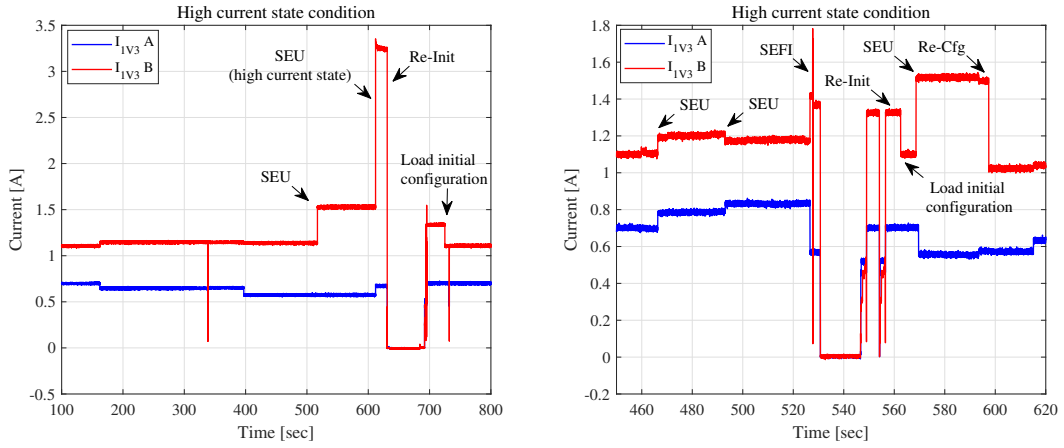


FIGURE 5.43: Register dependencies and resulting accumulated SEUs vs. monitored functional registers to illustrate SEU propagation, according to [151].

However, the effective number of counted SEUs induced by a particle is potentially lower since such register dependencies have not been taken into account during irradiation. Afterward, it was possible to analyze such conditions by either evaluating the register dependencies and matching those registers to the total number of counted SEUs to the corresponding functional register. An example is shown in Figure 5.43 on the previous page that illustrates the qualitative propagation of an SEU through the register map. In the case shown here, the highlighted register (red, dashed frame) 372_{dec} and 652_{dec}shows a extraordinary high flip-count in the accumulated numbers of SEU during three test runs under heavy-ion irradiation.

High current states

During all test conditions, neither SELs nor other destructive events occurred (up to an LET_{eff} of $125\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$). However, high current states were observed that are correlated to SEUs in functional registers. Two examples of high current states are presented in Figure 5.42. Figure 5.44 (a) depict an extremely high current state is presented that follows a re-initialization. A manual manipulation of the related registers that were found to have been flipped by an SEU during irradiation causes the same high current state as observed under conditions of heavy-ion exposure.



(a) Extremely high current state

(b) High current state

FIGURE 5.44: Observed high current states during irradiation that were caused by an SEU, according to [151].

In Figure 5.44 (b), multiple changes in the supplied current values are shown. In all cases, the current changes in steps which can all be correlated to SEUs. During the run a re-initialization was performed due to an observed SEFI. In the last section at about 570s, a high current state occurs that is recovered by a successful reconfiguration. High current states in general are of minor concern, since they are observed only rarely and are in all cases reproducible by manually changing the corresponding SEU registers that flipped during the observed high current events. Thus, it is assumed that these current

values are within the manufacturer's device specification and otherwise can easily be protected against due to the SEU detection and the use of current limitations.

Cross-section dependencies

During the heavy-ion test campaign, the tilt (pitch) angle dependency was evaluated. To do so, the DUT was irradiated with Xenon on 0 °, Rhodium on 45 ° and Krypton on 60 ° resulting in an almost common effective LET of approx. 63 MeV · cm^2/mg. The cross-section results for SEUs on both DUTs are presented in Figure 5.45.

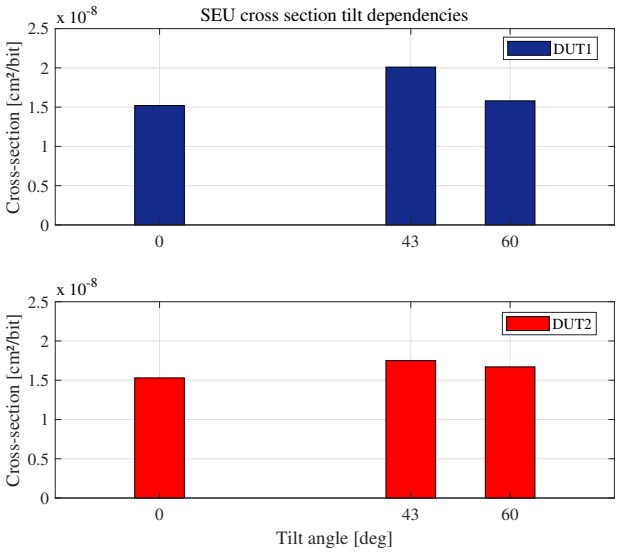
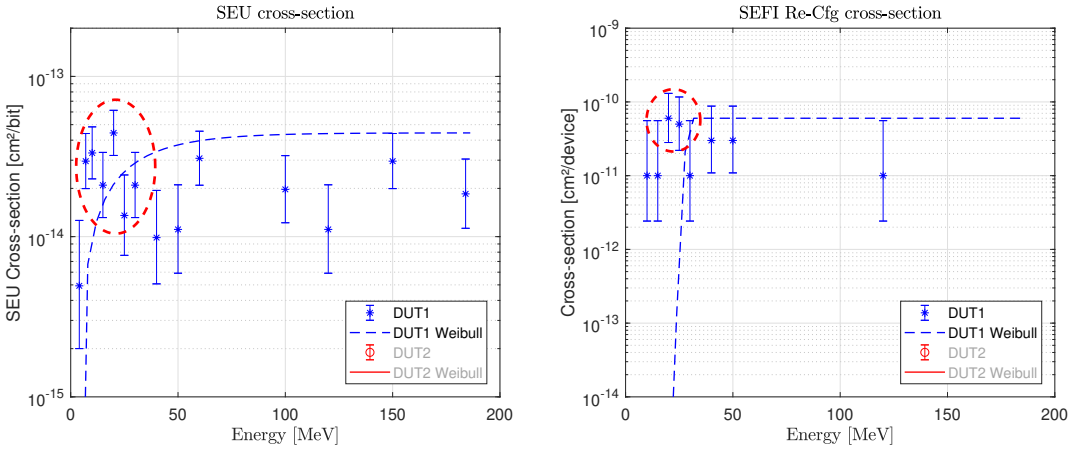


FIGURE 5.45: Tilt angle dependencies of incident heavy-ion particles (LET_{eff}≈63 MeV · cm^2/mg) to the SEU cross-section.

The results shows no major deviations in the saturated cross-section for all pitch angles. Minor differences are explained by uncertainties in the measurement and the error statistics. Similar results were observed for the SEFI cross-sections.



(a) SEU cross-section

(b) SEFI cross-section

FIGURE 5.46: Cross-section for SEU and SEFI events under proton irradiation.

For the proton cross-sections, a slight increase in the cross-section can be observed for lower energies as illustrated in Figure 5.46 for SEUs in (a) and reconfiguration SEFIs in (b). Such effects can be expected due to the 65 nm CMOS since it has been demonstrated that CMOS process below 90 nm may be sensitive to low proton energies and their capability for direct ionization [153]. However, due to the very low SEE response under proton irradiation, a clear statement regarding this phenomenon requires further investigations but is not mandatory.

Effectiveness on the LET in the sensitive region

As mentioned in the device description, the AD9361 is equipped with a large stack of metalization layers (up to seven) and an inhomogeneous distribution over the whole die area (Figure 5.17). Thus, one has to evaluate the effectiveness of such layers to the provided LET of heavy-ions to verify that penetration of the active region is given. This was confirmed by using SRIM [159] and by modeling the stack of layers and the corresponding materials. Especially for Xenon, the heaviest element in the HIF cocktail, the Bragg-peak point was observed to be still behind the active region. The effective LETs simulated by SRIM were close to the LET on the DUT's surface as presented and discussed in [151].

Event rate prediction

In Table 5.11, the predicted event rates for SEUs, MBUs and SEFIs are presented for the two desired reference orbits. As already seen in the cross-section results, the AD9361 is very sustainable to SEEs and event rates are low.

Table 5.11: Predicted event rates for the AD9361 using OMERE [32].

SEE Type	**Orbit**	**LET threshold [MeV·cm²/mg]**	**Limit cross-section [cm²/bit;dev]**	**Events/day (nominal).**	**Events/day (worst)**
SEU	GEO	1.00×10^{-3}	2.80×10^{-8}	2.23×10^{-7}	4.44×10^{-5}
SEU	LEO	1.00×10^{-3}	2.80×10^{-8}	1.39×10^{-7}	1.04×10^{-5}
MBU	GEO	1.00×10^{-3}	2.71×10^{-9}	2.76×10^{-9}	6.30×10^{-7}
MBU	LEO	1.00×10^{-3}	2.71×10^{-9}	2.01×10^{-9}	1.50×10^{-7}
SEFI_{cfg}	GEO	1.00×10^{-3}	8.01×10^{-6}	1.30×10^{-3}	2.84×10^{-1}
SEFI_{cfg}	LEO	1.00×10^{-3}	8.01×10^{-6}	6.65×10^{-4}	6.56×10^{-2}
SEFI_{init}	GEO	$4.56 \times 10^{+1}$	1.00×10^{-6}	3.92×10^{-8}	3.91×10^{-6}
SEFI_{init}	LEO	$4.56 \times 10^{+1}$	1.00×10^{-6}	1.04×10^{-8}	1.03×10^{-6}
IQ_{soft}	GEO	1.00×10^{-3}	1.95×10^{-5}	1.46×10^{-3}	3.20×10^{-1}
IQ_{soft}	LEO	1.00×10^{-3}	1.95×10^{-5}	7.68×10^{-4}	7.41×10^{-2}
IQ_{hard}	GEO	1.00×10^{-3}	1.25×10^{-5}	4.02×10^{-4}	8.70×10^{-2}
IQ_{hard}	LEO	1.00×10^{-3}	1.25×10^{-5}	2.11×10^{-4}	2.02×10^{-2}

Considering critical SEFIs such as hard IQ failures that may not be recognized by the AD9361 itself or that can be detected by driver-related SEFIs, such failures are predicted to occur only once in ≈11 days for worst-case condition (e.g. solar flare of 1 week's duration) in GEO and every ≈50 days in LEO.

Criticality analysis

The criticality determination of the AD9361 RFIC is presented in Table 5.12 below. Based on the deep investigations of radiation effects on the desired RF-Transceiver device undertaken during the work of this PhD thesis and the very good test results, the criticality numbers will be very low. In fact, SELs were not observed nor other destructive events. However, higher-current states were observed with respect to register-related changes in the configuration by an SEU or MBU. It is not expected that these states will cause thermal damage, however, as long as proper mitigation strategies (e.g. register scrubbing or current limitations) are applied (DN=1).

TABLE 5.12: FMECA criticality analysis on the RFIC functional block.

ID	Orbit	Failure causes	Failure effects	SN	PN	DN	CN
RFIC.1	LEO	SELs or high current states	permanent loss of system functionality	3	1	1	3
RFIC.1	GEO			3	1	1	3
RFIC.2	LEO	TIDs, long-term degradation	permanent loss of system functionality	3	1	2	6
RFIC.2	GEO			3	1	2	6
RFIC.3	LEO	SHEs, non-recoverable state	permanent loss of system functionality	3	0	-	0
RFIC.3	GEO			3	0	-	0
RFIC.4	LEO	SEFIs, recoverable state	temporary loss of system functionality	2	2	2	8
RFIC.4	GEO			2	4	2	16
RFIC.5	LEO	SEUs/MBUs/SEFIs, invalid data	corrupted data for transmission or reception	2	2	2	8
RFIC.5	GEO			2	2	2	8
RFIC.6	LEO	SETs, invalid data	corrupted data for transmission or reception	1	3	3	9
RFIC.6	GEO			1	4	3	12
RFIC.Total			**Average CN (LEO):**				**5.7**
RFIC.Total			**Average CN (GEO):**				**7.5**

TID is not an issue at all, since the device has shown no functional failures nor loss of performance up to 45 Mrad(SiO_2). However, shielding can be applied to further improve the TID-related criticality (DN=2). Even though the SEU's impact on functional

operation has shown to be non-critical, SEFIs occur in different ways and were evaluated during the intense radiation test campaigns. Their probability of occurrence is not negligible, but with applied mitigation strategies as discussed in section 5.3.4, the probabilities of detection are likely (DN=2) with the driver-scrubbing function ($SEFI_{cfg}$) and these would result in a moderate CN. IQ failure resulting in invalid data as defined as SET in table 5.12 are expected more often and could be potentially detected but not corrected (DN=3). However, such events are less critical since they should only lead to minor bit errors in the data transmission (which may be negligible if either ECC or another coding mechanism are applied).

Assuming all investigated effects, the general usability of this RFIC is acceptable for use either in LEO or GEO missions.

5.4 Summary

This chapter has presented and discussed the radiation effects on system-critical COTS devices of the GSDR. For the Zynq-7000 baseband processor and the memory resources, results were presented based on recent publications. These results were found valid and were adopted to identify possible failures to the entire system and their impact on the overall system reliability and performance. Based on the results, certain mitigation strategies can be applied or developed to prevent instances of destructive damage that could lead to a persistent loss of function and to improve the general system reliability and performance. The referenced test results showed sensitivities to radiation effects but are generally possible to deal with in most cases. Only the NAND flash device which is desired for non-volatile memory showed destructive failures that may occur during heavy-ion irradiation. However, these types of irreversible failure have been shown to be very rare and only occurred during extensive read/write/erase operations. Thus, the probability of failure is very low since the NAND flash will not be operated heavily under those conditions. The Zynq showed potential SELs on the auxiliary voltage supply which presents in slow steps and could be easily detected and limited by certain protection mechanisms. In any event, the presented results here and their corresponding interpretation and discussion make a persuasive argument for the use of the investigated components in the GSDR system design.

Probably the most important COTS device, the AD9361 RFIC, has been fully investigated under radiation effects in the context of this thesis. The characterization of such devices has been performed for TID and SEEs using different radiation sources such as Co60 sources (γ-rays) or an x-rays machine, as well as proton and heavy-ion particle accelerators. The device showed a very robust performance under all irradiation conditions without destructive events and a very attractive response to SEEs.

The results on the AD9361 presented here have also been published in a shortened version in [129, 149, 151, 156, 157, 160].

Chapter 6

System-level design and verification

In this chapter the final system design and its verification under radiation conditions will be presented. Section 6.1 sets out the final GSDR design on hardware and software level. A specific focus is made to the implemented mitigation mechanism that shall detect and recover from failures induced by radiation effects. The verification of such mechanism and the overall performance of the GSDR for three radiation test campaign is presented in section 6.2 and finally discussed in section 6.3.

6.1 Final system design

This section provides an overview of the final system design of the proposed highly integrated and radiation-tolerant SDR (GSDR) for the operation of multi-band RF applications in space missions. This includes the hardware design description in section 6.1.1, the software design in section 6.1.2 and the applied mitigation strategies and mechanisms (section 6.1.3) for protecting the system against radiation effects and to improve the system's reliability and performance. Finally, the system-level verification under radiation conditions is presented in section 6.2.

6.1.1 Hardware design

The final hardware design consists of the previously described novel hybrid system design approach. A 3D model of the GSDR including the exchangeable RF-daughterboard and a housing is depicted in Figure 6.1 on the following page. As already mentioned in the selection procedure for EEE parts in section 4.2.1, a series of devices was chosen on space-qualified, RadHard level while other parts are selected for COTS with

lower qualification-grade (automotive or military) but ensure a good product traceability and/or up-screening options.

(a) GSDR front view (b) GSDR back view

FIGURE 6.1: 3D model of the final GSDR system with housing and exchangeable RF-daughterboard attached.

The eventually selected devices for the GSDR system design are set out as follows for the functional blocks:

- **Baseband processor:**
  As described in the device selection procedure, there are not many alternatives to choose from for the baseband processing unit. In the end, the Zynq-7020 was selected with optional automotive/military-grade, including extended temperature ranges, non-plastic or out-gassing limited encapsulations and higher screening capabilities.

- **Data and control interfaces:**
  The GSDR supports two main digital interfaces that allow data exchange. These are an RS422 driver and receiver which is usually chosen for the UART interface but could also be used for other low data-rate protocols. The selected RS422 devices are from Renesas, including the HS-26CLV31RH line driver ([161]) and HS-26CLV32RH receiver ([162]). For higher data-rate purposes (e.g. Space-Wire), the GSDR design is also equipped with an LVDS interface. The driver (SPLVDS031RH [163]) and receiver (SPLVDS032RH [164]) used are manufactured and distributed by Space-IC.

- **Memory resources:**
  For the non-volatile memory, the NAND flash technology is preferred for providing a boot device and data storage capabilities. The desired device is the 8 Gbit automotive-grade Micron MT29F8G08AAAWP. Even though if NAND flashes have been well investigated in the context of radiation effects as presented in this thesis, a radiation-tolerant solution by 3DPLUS, the 3DFN8G08VS1706 [165]

which uses the same die of the Micron MT29F8G08AAAWP is under consideration for the design. The main difference from the latter device is that 3DPLUS performs up-screening, carries out radiation tests on the specific lots and encapsulates the die in a hermetic-sealed package.

Two DDR3-SDRAM devices of the automotive-grade (AEC-Q100) 2 Gbit of Micron (MT41J256M8HX.15E:D) were desired since the discussed radiation test results are very promising and this DRAM on the same die-revision was still available. In the meantime, the MT41J256M8HX has become obsolete but several parts are still in the own stock and can be partially purchased by distributors. Alternative solutions have lately been found such as the radiation-tolerant DDR3-SDRAM [120] that have recently been made available by 3DPLUS, namely the 3D3D16G16YB4751 [166]. This device is also a suitable structure for the Zynq-7020. This radiation-tolerant NAND is currently under consideration to be used in a further revision of the GSDR, since own investigations and up-screening activities on other DDR3-SDRAM candidates are potentially too expensive.

- **Power regulation:**
  The GSDR requires different technologies governing power regulation devices, including high-current step-down (buck) converters, low-dropout (LDO) and a specific DDR3-termination regulator. For buck converters, a highly efficient 2 A point-of-load (POL) converter from Space-IC (SPPL12420RH) has been chosen [167]. The LDOs are important for enabling the RFICs, to provide a stable power supply and to improve their phase-noise performance. For each AD9361, a dedicated LDO is used from Texas Instruments (TPS7H1101-SP, [168]). The TPS7H3301-SP ([169]) is an integrated RadHard and space-qualified sink/source DDR3 termination regulator with a built-in VTTREF buffer that is used to supply the DDR3-SDRAM employed in the GSDR system. In order to provide a low-cost evaluation and development model of the GSDR, each power regulation device has either a pin-compatible commercial alternative with the same performance and characteristics or a dual foot-print design.

- **RFIC:**
  For the RFIC, two AD9361s were selected, as previously mentioned in the device selection procedure in section 5.2 and based on the extensively investigated radiation effects characterization. The GSDR is thus equipped with four independent receiver and transmitter chains that also allows multiple input multiple output (MIMO) applications. Digital timing and RF phase calibrations are possible by synchronization procedures and an RF hard-wired cross-connection of both devices. Analog devices support a single manufacturing site and updates customers about product and process changes by a general notification service.

Hence, radiation characteristics are assumed to be valid as long as the process remains unchanged.

- **Clock generation:**
  In terms of performance, costs and stability, the general clocking sources have been chosen according to the TCXO technology. The Zynq-7020 requires a 33.33 MHz oscillator frequency for the PS and a 100 MHz clocking signal for the PL. Both TCXOs are FXO-HC54 HCMOS oscillators by Fox. The AD9361 is supplied with a 40 MHz LVCMOS clock by means of a high-precision and ultra-stable TCXO. The device selected, the M100F manufactured by Connor-Winfield, provides a stability of less than 100 ppb over industrial temperature ranges and has excellent phase-noise performance [170]. To support both RFICs, a common clock-buffer device is required and for this purpose the CDCLVC-1310 from Texas Instruments has been selected. This device has been tested by third parties for reference and is also currently under further investigation by the author of this PhD thesis.

- **Supervising circuit:**
  It is not mandatory to design the supervising circuit with RadHard devices, as discussed in section 4.2.8. However, since specific parts are important for establishing a self-recovery from system functional interrupts, the watchdog device (ISL705ARH), the timer (SE555-SP) and the power switches (IRHNJ597034 + JANSR2N222AUB) are chosen RadHard. Other devices that are included in the supervising circuit are non-critical parts to radiation (e.g. Zynq-7020 internal ADC, low-power switching transistors (NPN) or current-sensing amplifier). A further description of the supervising circuit and its design is presented in the hardware mitigation section 6.1.3. Similar to the other RadHard devices in the previously presented functional blocks, a commercial alternative is foreseen for the manufacturing of a low-cost evaluation and development model.

6.1.2 Software design

The GSDR software design basically consists of sets of functional data that are required to support a fully functional operation. These data sets are configured to **boot images** and **filesystem images**. The software architecture is based on an embedded Linux OS which is specifically tailored to reduce size and complexity. Beside the *Linux filesystem* a *kernel* is developed to interact with certain devices of the GSDR (e.g. AD9361) over corresponding drivers. The architectural interconnection between the filesystem, kernel and the GSDR devices is defined in a *devicetree* file. Kernel, Linux filesystem and the devicetree are parts of the filesystem image. Due to the combination of PS and PL of the Zynq, a *bitstream* is mandatory. The boot mechanism is carried out in four stages as shown in Figure 6.2.

In order to boot and load the essential files from the NAND flash and bring up the system to nominal operation, a boot image is required. A boot image contains the *BootROM header*, *first-stage boot loader (FSBL)*, *second-stage boot loader (SSBL)* and an initial bitstream which is necessary to physically interconnect the GSDR devices with the Zynq and hence with the Linux OS.

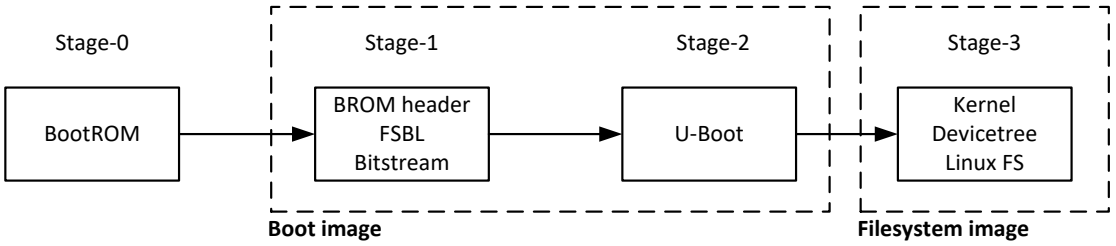


FIGURE 6.2: Boot procedure of the GSDR.

In the first stage (*stage-0*), the internal BootROM which stores the boot code is executed firstly on one of the central processing unit (CPU) cores after a hardware-reset or the initial start-up. The BootROM is hard-coded in a non-accessible read-only memory. It initializes the clocks and configures one of the CPU cores along with necessary peripherals to fetch the boot images located in the NAND flash boot device. Once the initialization and self-checks have been performed and confirmed, it searches for the BootROM header and then starts the transition to *stage-1* by copying the FSBL code to the OCM of the Zynq PS and then starting its execution. The FSBL is responsible for initializing the PS configuration data (MIO, Clock, DDR etc.), flashing the PL with the initial bitstream, searching for the SSBL within the boot image, then loading it to the DDR3-SDRAM and finally executing a hand-off to the SSBL (*stage-2*). In case of the GSDR, the SSBL is a u-boot bootloader that furthermore can load and execute additional data such as devicetree, kernel and Linux filesystem that are combined within the filesystem image (*stage-3*).

Since it is feasible that SEUs in the NAND flash might corrupt either the boot or filesystem image, a multi-boot mechanism with fallback options at different stages is established as described in [171]. Such a mechanism is depicted in Figure 6.3 on the following page. For the BootROM code neither a fallback option nor a secure mechanism is possible since it is hard-coded. However, it has not been found in the referenced radiation results that such code has been damaged during irradiation. Before the hand-off from *stage-0* to *stage-1* takes place, the BootROM code searches for a BootROM header in the boot image and performs validity checks (image identification parameter check and the calculation and verification of the headers' checksum) before loading the FSBL to the OCM. Thus, errors in the BootROM header can be detected and the BootROM searches for the next valid header in the NAND flash boot device or safely locks down the system and reports an error code. The second case happens if the search process fails for all boot images and the process goes out of range (128 MB for NAND

flashes [171]). Usually, if a BootROM header is invalid, BootROM increments the search address by 32 KB and repeats the validity checks until a valid header is found and the FSBL is loaded to the OCM and executed.

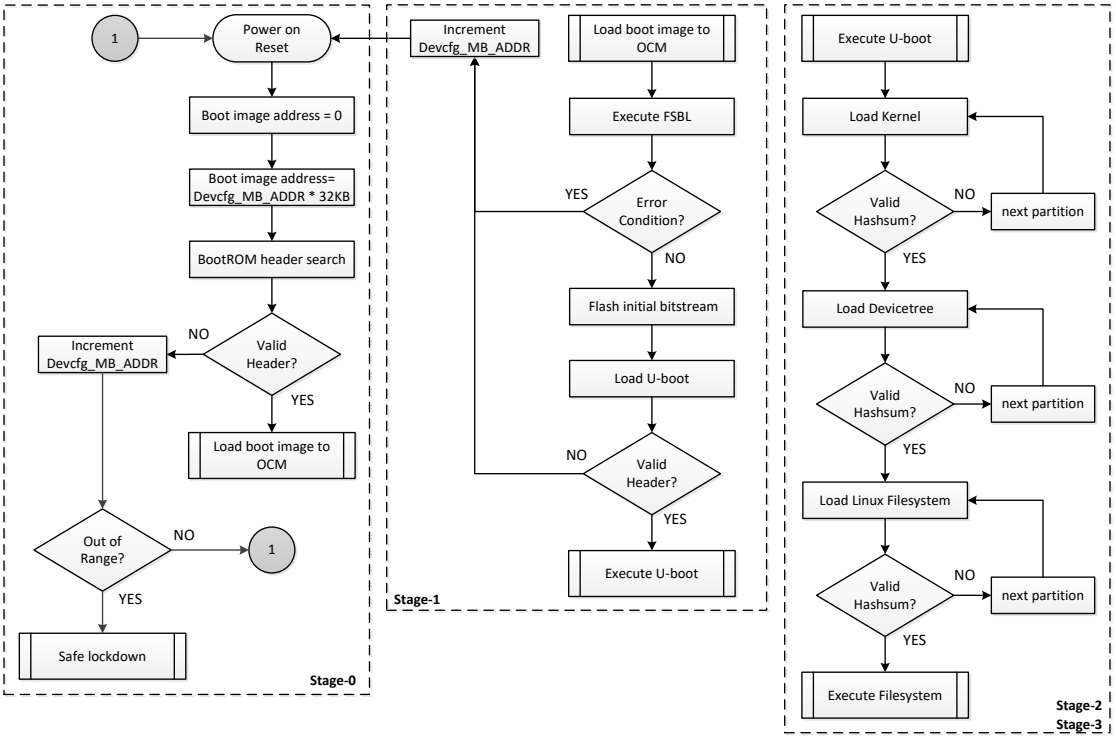


FIGURE 6.3: Boot procedure of the GSDR with fallback mechanism.

In order to establish a secure fallback mechanism for the other stages, BootROM has access to a configurable multiboot address parameter (Devcfg_MB_ADDR) that can be controlled by the FSBL. Once the execution of the FSBL has been initiated, it can report error conditions, increments the MB_ADDR and then performs a soft-reset that leads the processor to clear the configurations and execute the BootROM again (*stage-0*). Due to the incremented MB_ADDR, BootROM is then searching for the BootROM header within the next boot image that can be located in a different region of the NAND flash.

Before the FSBL hand-off to the SSBL (u-boot), it validates its header. If the validation fails, the MB_ADDR is incremented and a soft-reset is performed to load the next boot image. If the u-boot header is valid, the SSBL is executed and takes control for the further boot procedure (*stage-2*). At this stage, the boot image has fully loaded and u-boot is able to load the filesystem image partitions one by one (kernel, devicetree and Linux filesystem). Each image part has multiple redundancies in dedicated partitions (addresses) of the NAND flash boot device. Each partition is verified by a hashsum before loading to the DDR3-SDRAM. If all parts are loaded, the execution of the filesystem takes place and the final *stage-3* is reached. Once the filesystem is executed,

several tasks are started that monitor the system conditions and perform application-specific signal processing. The monitoring tasks especially are described in more detail in the following section 6.1.3.

Due to the fact that only the headers of the BootROM and u-boot are verified, there is no guarantee that any further code may be corrupted which lead to a deadlock of the boot process and system. As will be described in section 6.1.3, it is therefore important to cross-check the boot and filesystem images when the system is running. Thus, possible scenario for reaching a deadlock is when a critical upset occurs during the boot process before the FSBL and SSBL are loaded and executed. To identify the sensitivity of corrupted codes of the bootloaders, multiple bits (and bytes) are re-written with random data at the addresses of the NAND flash where the bootloaders are stored. The results showed that for both bootloaders it is mandatory to corrupt a relatively large amount of data (up to 10 %) to force a deadlock situation. Thus, and especially due to the short time period when a radiation-induced corruption is possible in space, it is very unlikely that a deadlock will occur.

6.1.3 Radiation effect mitigation methods and strategies

In order to detect functional interrupts and prevent catastrophic damages to the system from radiation effects, the GSDR system supports several mitigation mechanisms on hardware and software level to autonomously recover to a nominal and safe state.

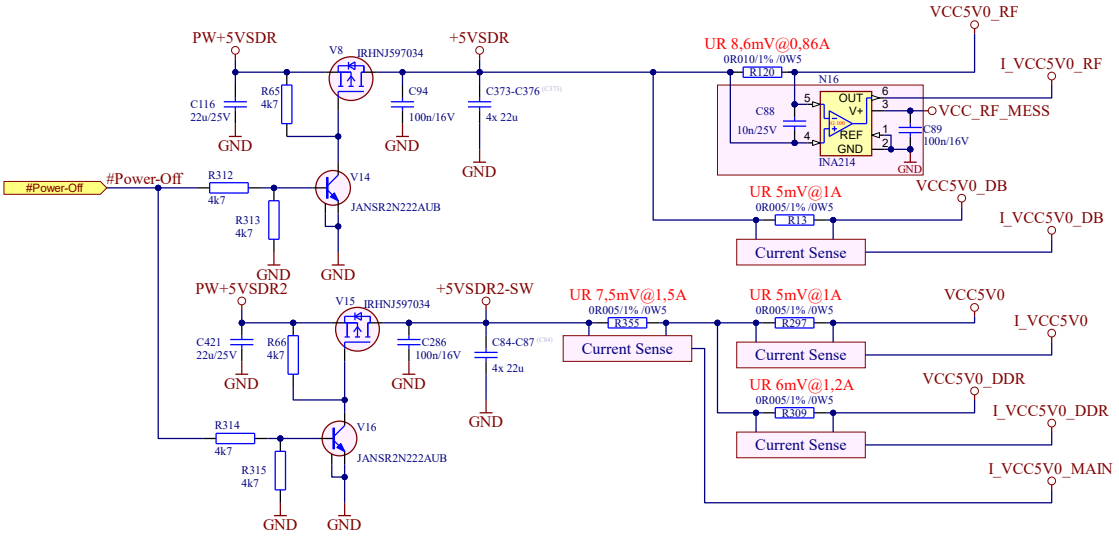


FIGURE 6.4: Power-input stage schematic of the GSDR with current-sensing nodes and the power-switch unit to internally reset the system.

In principle, the mitigation strategies implemented are a combination of soft and hardware mechanisms. As mentioned previously in the supervising functional block design, the GSDR is equipped with certain devices that are capable of detecting functional interrupts and to force a self-triggered reset. The essential power-input stage that is designed

with a power-switch circuit is presented in Figure 6.4 on the previous page. The GSDR is designed with two primary power inputs to allow for use also on space missions where current limitations on the spacecraft's power distribution and conditioning unit could be an issue. Thus, each primary power-input line has a dedicated power-switch circuit that is triggered simultaneously in any case. The power switches are a combination of a MOSFET device and a driving bipolar transistor (BJT). The BJT is controlled by a centralized *#Power-Off* signal that is distributed by the supervising circuit presented in Figure 6.5.

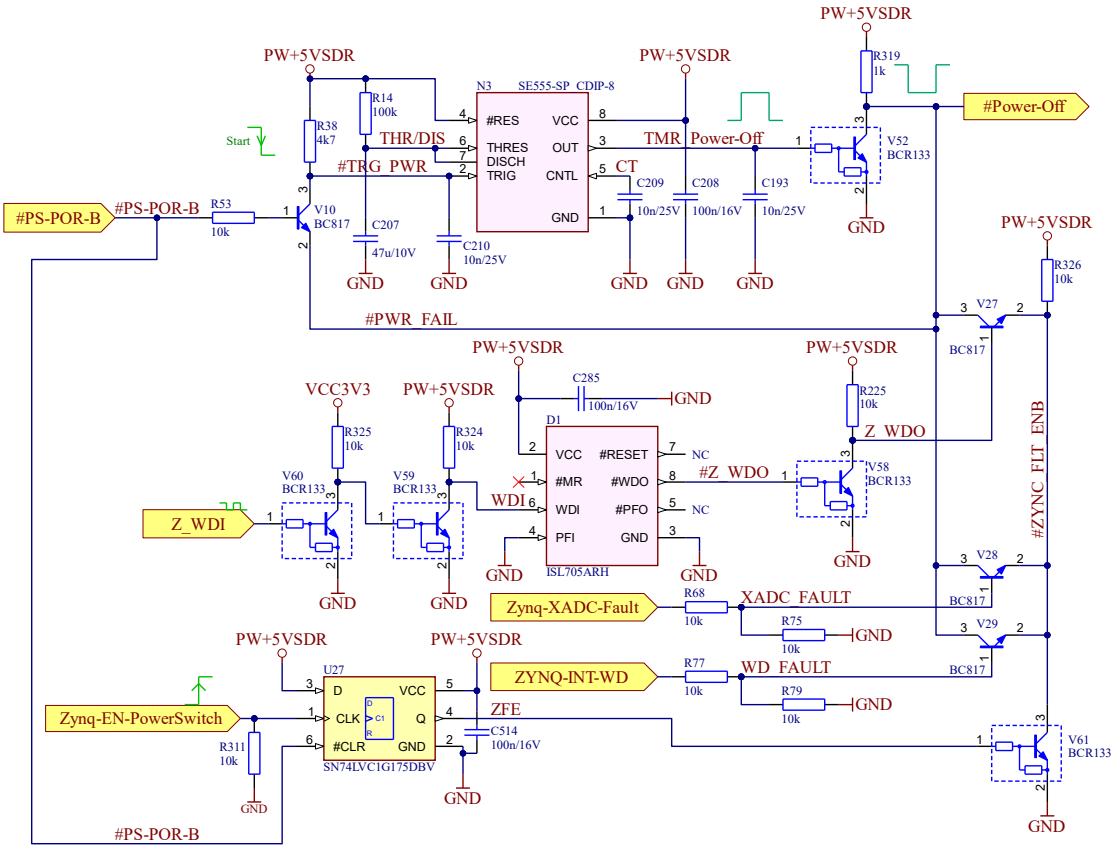


FIGURE 6.5: Essential part of the supervising circuit schematics.

The system is able to monitor internal voltage and current conditions on each of the sub-voltage power lines. To do so, a shunt resistor is integrated in series for each power line whereby voltage drop-off is magnified by a current-sensing amplifier (INA21X). The resulting amplified voltages are provided to the system-integrated XADC of the Zynq-7020 BBP and evaluated by a software module to detect sub-voltage high-current state (SELs) and abnormal voltage conditions. The supervising circuit, as schematically presented in Figure 6.5, primarily consists of the watchdog, timer and a set of BJTs to provide the discrete trigger for the *#Power-Off* signal from multiple sources.

Three different sources have been determined that can force a reset:

1. *Zynq-XADC-Fault*: If a non-nominal voltage or current condition is detected by the Zynq-XADC, a fault state is released to trigger a reset.
2. *ZYNQ-INT-WD*: If a software issue is detected that cannot be recovered (e.g. a process stuck and cannot be restarted), the system can trigger a reset.
3. *Z_WDO*: If the watchdog is failing to detect the heart-beat signal from the processor (description see below) it will enable the active low WDO output and force a reset.

Especially since the watchdog requests a heart-beat signal directly whenever power is supplied ($\leq$1.6 s) and the boot sequence takes longer than the power-on sequence of the board, it would immediately trigger the *#Power-Off* signal and continuously interrupt the boot process. Thus, the supervisory circuit needs to be enabled after the boot sequence has been completed and the software is fully operational. Therefore, the *Zynq-EN-PowerSwitch* signal is implemented which prevents such interruptions and unwanted reset events.

As soon as the OS is booted, the system starts several tasks to detect and recover failures that may be induced by radiation effects but also generally supervises the system's health conditions:

- **RFIC supervising:**
  To detect functional interrupts on the AD9361 RFIC, a dedicated software-task monitors changes in the register configuration and continuously reads the driver parameters, as described in the device characterization in section 5.2. IQ data validation is possible by means of the RF feedback option that is usually designed to perform RF phase calibrations between both RFICs for MIMO application purposes.
- **Temperature, voltage and current validation:**
  One of the *#Power-Off* trigger events is the detection of abnormal current and voltage conditions that are captured by the Zynq-7020 XADC. Furthermore, several device temperatures are monitored that can also force a reset of the system. The software implementation for this validation process reads out all relevant information and verifies whether the levels are within the tolerances that are user-defined. If one or multiple values exceed the hard-threshold in a certain period (warning thresholds are also implemented that are reported in the housekeeping data set but do not force a reset), the software process triggers the *Zynq-XADC-Fault* output and thus forces a reset.
- **Software watchdog:**
  For more minor problems, such as frozen software processes that need to be fixed,

a software watchdog is implemented. This watchdog monitors all processes at regular intervals and can trigger the kernel watchdog. The software watchdog starts as a daemon and monitors certain processes and system resources. In the event of an error, a repair script is started that will recover the erroneous process. If errors are not fixed or the software watchdog itself crashes, the kernel watchdog performs a reboot (not a reset) of the system.

- **Hardware watchdog:**
  To trigger the external hardware watchdog (ISL705ARH) of the GSDR, a process sends heart-beat pulses every 200 ms to the watchdog device input. If the whole software architecture or OS is not working properly anymore and if neither the software watchdog nor the kernel watchdog are capable of resolving this issue, it is assumed also that the heart-beat signal will disappear and will lead the hardware watchdog to force a reset.

- **Boot configuration validation:**
  With a dedicated process, specified files/partitions are cross-checked with a hash-sum. This is usually intended for boot files/images such as the kernel, ramdisk image and BOOT.bin. For these files and their duplicates, there is a single hash file with the hashes of the respective files. At regular intervals, these files are checked and in the event of an error, a redundant file with a correct hashsum is used to overwrite the corrupted partition/file.

6.2 System-level testing and verification

Even though critical COTS devices have been carefully selected, radiation test results on component-level are available and presented with their criticality to the system design, some COTS components have not been investigated with regard to radiation effects which have been found to be less critical based on the FMECA performed. Furthermore, different radiation effect mitigation strategies were implemented to improve the system performance under radiation conditions and to increase the reliability. In order to validate such mechanisms and to verify the selection of less critical COTS devices, system-level radiation testing is now considered.

RHA through system-level testing is currently not very common but becomes more and more popular, in particular relevant for NewSpace applications where development time is critical and does not foresee component-level testing. However, risk acceptance is a critical key element for system-level testing approaches and needs to be considered. Recent guidelines were developed and published during this work, in which the here presented development and verification of the GSDR was used for contribution [172, 173].

System-level radiation tests were performed in three test campaigns including proton irradiation and the use of a mixed-field irradiation facility at European organization for nuclear research (CERN), namely CERN high energy accelerator mixed-field facility (CHARM). The following sections will outline the test definition, the test setup and test results.

6.2.1 Test definition

Similar to the previously presented radiation tests on the AD9361, system-level testing was conducted according to reference mission requirements. Since large areas of the GSDR need to be irradiated, only proton irradiation at KVI has been carried out. Heavy-ion testing was not possible since the test facilities used in this study do not support large field beams nor energies that are capable of passing trough plastic encapsulations.

In addition to proton testing, a unique mixed-field irradiation test facility has been used that allows irradiation of very large systems. The system is exposed to radiation during operational conditions, meaning reception and transmission of RF data as well as the control of the GSDR to execute certain commands and to verify the protection mechanism as described previously in the mitigation strategy section.

The first radiation test campaign was carried out at CHARM using a prototype version of the GSDR (see 3D illustration in Figure 6.6) which has the same architecture but which has been equipped with a back-plane connector and a different power regulation design (the prototype was fully based on COTS devices). The same prototype was used in the second test campaign which was held at KVI.

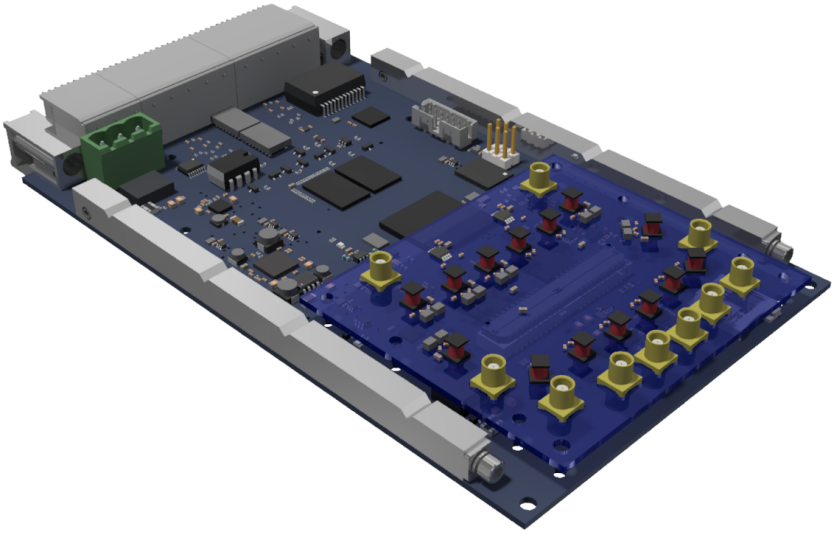


FIGURE 6.6: 3D model of the GSDR prototype that was used for the CHARM test campaign and the first proton irradiation test at KVI.

The final design of the GSDR (illustration in Figure 6.1) has been recently tested under proton irradiation at KVI. The specific test conditions for both test sites are described in more detail in the following sub-sections.

6.2.1.1 CHARM

CHARM provides a mixed-field radiation environment by using the 24 GeV proton beam of the CERN proton synchrotron (CPS) complex that is extracted and directed to selected metal targets (e.g. copper). Protons of the CPS arrive at the metal targets in spills lasting about 350 ms. The repetition period of spills is about 10 s. Irradiation can be considered as quasi-continuous since the pulse is orders of magnitude larger that the SEE-characteristic time scale (typically in ns, see Figure 2.11). A layout of CHARM is presented in Figure 6.7 with the initial position (PC0, green box) of the GSDR as system under test (SUT).

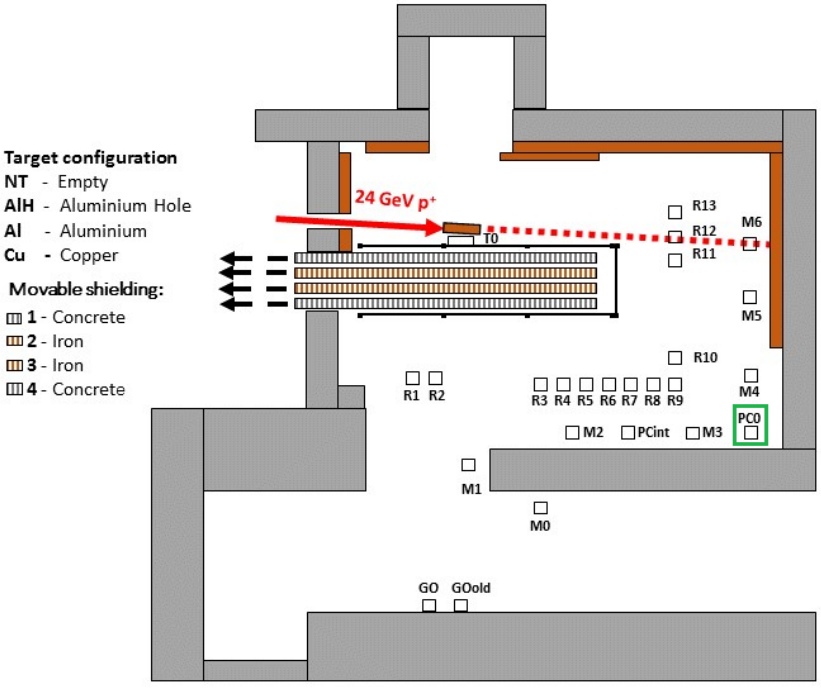
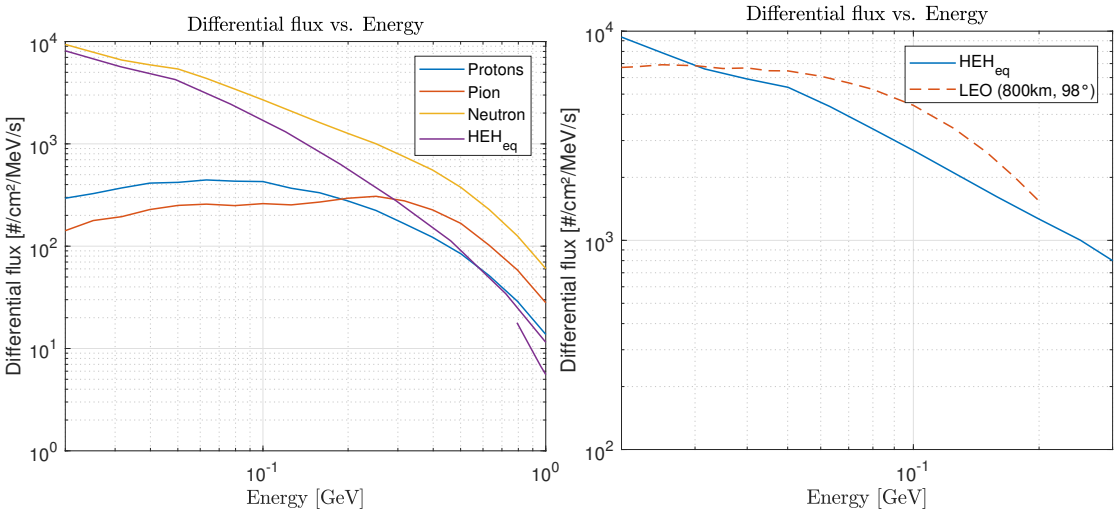


FIGURE 6.7: Layout of the mixed-field radiation facility CHARM, according to [174].

Multiple particle species are present at CHARM over a broad energy range as described in [175]. However, hadrons are mainly responsible for the generation of SEEs since these can generate nuclear interactions leading to localized energy deposition. First approximations showed that all hadrons above 20 MeV, mainly consisting of neutrons, protons and pions, are considered as equally efficient in inducing SEEs. The expected differential flux as illustrated in Figure 6.8 on the following page is simulated by using the FLUktuierende KAskade (FLUKA) Monte Carlo simulation tool.

For energies below 20 MeV, charged hadrons are almost disregarded due to their loss of energy when they encounter packaging materials. Coulomb repulsion with the nuclei and neutrons are weighted with a response function in an energy range of 0.2–20 MeV. This range was evaluated according to experimental SEU data for a given reference SRAM memory. The sum of the hadron fluence above 20 MeV plus the intermediate energy (0.2–20 MeV) neutron contribution is defined as the equivalent high-energy hadron fluence (HEH_{eq}) and used to calculate corresponding cross-sections in the mixed-field environment.



(a) Differential particle flux

(b) Differential flux on HEH_{eq} and reference mission

FIGURE 6.8: Differential flux of particle composition in (a) and comparison of HEH_{eq} flux vs. proton flux of a LEO reference mission in (b).

A nominal spill contains about $4.5 \times 10^{+11}$ protons which results in a high-energy hadron (HEH) equivalent flux of $1.02 \times 10^{+7}\,\mathrm{HEH_{eq}/cm^2/spill}$ and a TID of 0.44 rad(Si)/spill at the desired position of the GSDR within CHARM. The irradiation test campaigns lasted for five days and an HEH_{eq} fluence of $2.17 \times 10^{+11}\,\#/\mathrm{cm}^2$ was achieved as well as a total dose of ≈10 krad(Si).

Test setup and procedure

The measurement and test equipment is located in the control room during the irradiation phase. The irradiation room is connected via patch panels providing several digital, analog and RF cable connections to the control room as illustrated in Figure 6.9 on the following page. For better error statistics and backup purposes, two samples were tested in parallel. Due to the limited number of RF cables, an RF multiplexing circuit was implemented in order to evaluate all RF-specific configurations and possibilities of the GSDR. The RF multiplexing circuit is a customized, RadHard design, as featured in [176]. Each SUT has a corresponding reference transceiver where RF data are exchanged (received and transmitted). A commonly used computer (as seen in a spacecraft OBC) is responsible for commanding and controlling each SUT (via UART) and for managing

the allocation of the RF multiplexing circuit. The second UART interface is used to dump the log data of the SUT software which is then stored by the OBC in an (error) log file.

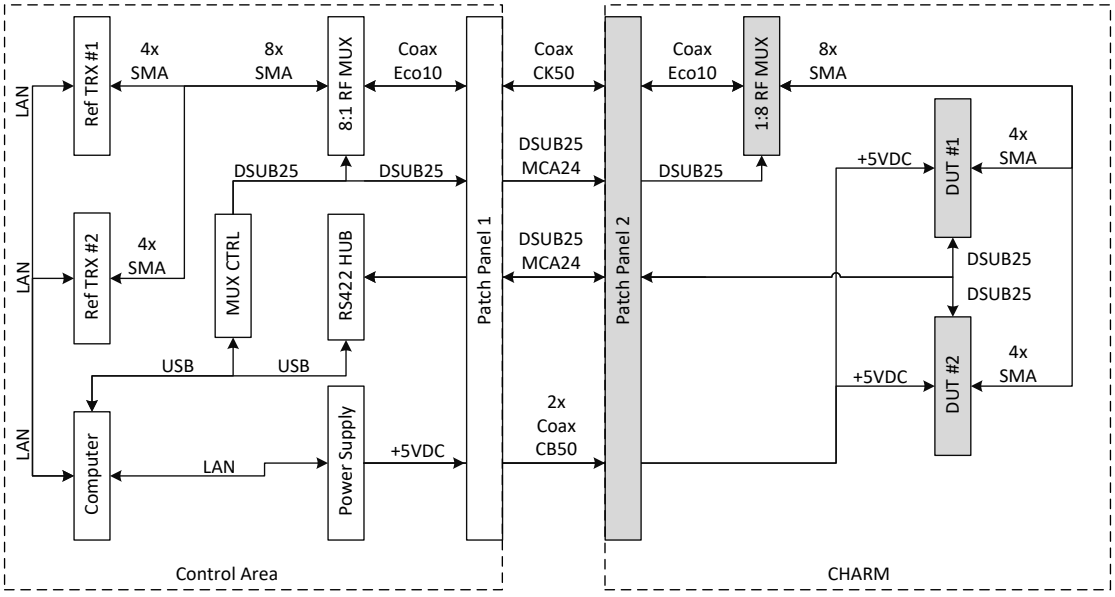


FIGURE 6.9: Schematic of the test setup of two GSDRs in the CHARM facility, according to [174].

In order to establish a reliable and automatic test procedure, a significant amount of software logic is required, specifically implemented in the OBC control computer software. The basic control and data flow is presented in Figure 6.10 below.

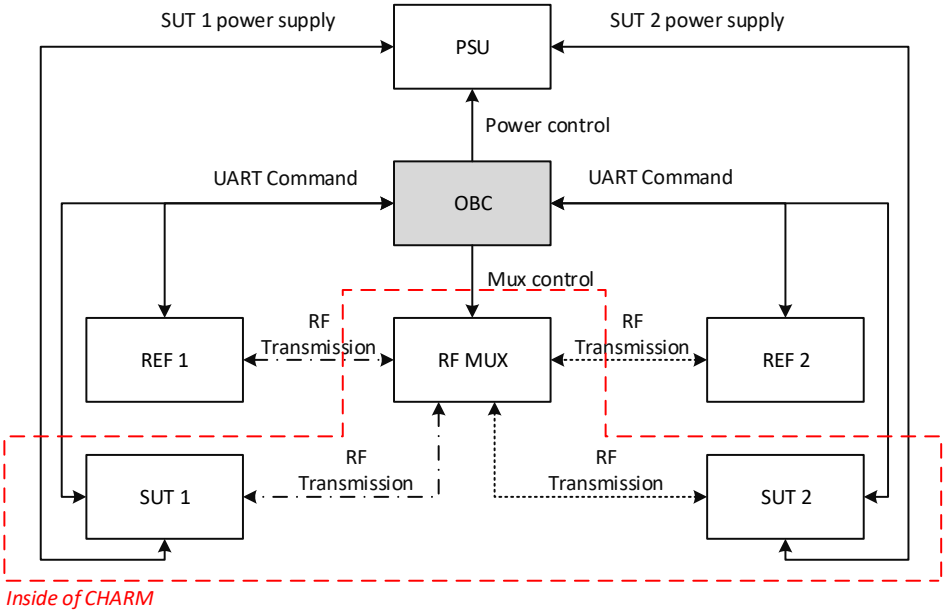


FIGURE 6.10: Data and control flow process for the GSDR system-level test at CHARM.

The OBC, located in the control area, commands the SUTs with a repeating procedure and captures and stores the replied data. These commands include the processing of RF data by execution of programs to further process the captured baseband data (spectrogram, waterfall fast-fourier transformation (FFT) of RF data) and providing housekeeping data to evaluate the health condition of the SUT.

The GSDR receives the request or commands from the OBC, executes the corresponding request and replies with the telemetry data. For the prototypes being tested, the generated data was temporarily stored on an SD-Card which was later removed from the design since it caused serious issues during the test (see section 6.2.2). The OBC also controls the power supply unit (PSU) to allow a power-cycle of the SUT and to prevent critical damage such as in the case of a high-current event or major SEL.

Due to the fact that only one RF cable is available between CHARM and the control area, the RF multiplex circuit needs to be used to share the capabilities of RF transmission for both SUTs and all receiver and transmitter options of the GSDR.

In general, the OBC follows its procedure list, requests actions of a SUT and controls the allocation of the RF multiplexer. Once the SUT has responded successfully, the OBC releases the RF multiplexer and follows the next procedure step and the next SUT can request the multiplexer allocation if required. In cases where an SUT is still not responding after the third repeated command, the OBC assumes that a functional system interrupt has occurred and triggers the PSU to power-cycle and reboot the SUT. During the reboot process, the OBC skips the non-replied request and continues with the next procedure step. In principle, the procedure follows a hopping between both SUTs to avoid long time gaps during the reboot process. Thus, even if a permanent loss of operation of one SUT appears, the procedure can be continued.

Each SUT is in general capable of handling a series of malfunctions on its own, as detailed in the radiation effect mitigation methods section 6.1.3. Therefore, two major SEFIs can be classified: (1) self-recovered SEFIs and, (2) power-cycles SEFIs by the OBC due to non-responding issues. Further investigations are made on the processed baseband data, the internal generated housekeeping reports and the soft mitigation strategies (e.g. memory scrubbing or fault detection on the RFIC settings).

6.2.1.2 Proton irradiation

As mentioned, two test campaigns were performed on the GSDR under proton irradiation at KVI. The first one was in addition to the test that had been carried out at CHARM and aimed to verify the achieved results using the prototype of the GSDR. The second test was conducted on the final design as presented in section 6.1. For both test campaigns a primary proton beam energy of 184 MeV was chosen and degraders

were used to scale the desired beam energies. In total five energies were used: 184, 150, 120, 100 and 70 MeV. Due to time constraints, the total fluence for all energies was limited to $5 \times 10^{+8}$ protons/cm^2 for the first test. For the second test campaign the target fluence was magnified by a factor of five to $2.5 \times 10^{+9}$ protons/cm^2 to improve the error statistics. Although for the second test campaign the final GSDR design was used, changes are not expected to be seen in the cross-section results since the principal architecture and components of interest (see below) have not been modified.

Test setup and procedure

In both campaigns, one SUT of the GSDR was evaluated. Due to the selected collimator at KVI, different areas of interest can be irradiated. Three particular areas were of interest:

1. Zynq (only for the first test campaign)
2. Zynq+DDR3+NAND
3. DDR3
4. Zynq+NAND+DDR3+AD9361 (only for the second test campaign)

Similar to the methodology of the CHARM test campaign, the SUT is controlled by the OBC which repeatedly commands the GSDR and waits for its reply. In case of a non-response (three consecutive commands), the SUT is power-cycled and the last request/command of the OBC is repeated. An important modification in the data generation work-flow was made in order to avoid the issue that was observed at the CHARM test with the SD-Card as temporary data storage before transmission of request data to the OBC. In this case, the data were generated on-the-fly in the non-volatile DDR3-SDRAM and directly transmitted. Furthermore, the generated data are later stored in the NAND flash devices instead of using the SD-Card. Further modifications to the basic software architecture were not made. The RF data transmission in this test was performed directly by individual cabling to the reference transceiver device since the RF multiplexer was not mandatory. The characterization follows the same categorization as for the CHARM test, including the major SEFI behavior and the system mitigation mechanisms. Due to the specific focus on non-RadHard devices listed above (critical COTS component, see section 5) of the final system design, the commercial-grade version of the GSDR (evaluation/development model) was chosen for the second test campaign at KVI.

6.2.2 Test results

This section focuses on the test results under the mixed-field irradiation environment in CHARM and the proton-induced radiation effects on system-level. These results are discussed in section 6.3.

6.2.2.1 CHARM

Due to the nature of CERN's proton synchrotron where particles come in spills with a high concentration of protons, SEFIs of the system were observed during the first spills resulting in a reboot or power-cycle of the SUTs. In most cases, the system-integrated hardware watchdog triggered a reboot due to the missing heart-beat generated by the software running on the ARM processor. In minor cases, the system needed to be power-cycled due to non-responded commands from the OBC. The number of events and the resulting cross-sections for both types of SEFI are presented in Table 6.1.

Table 6.1: Cross-section results for the CHARM test campaign.

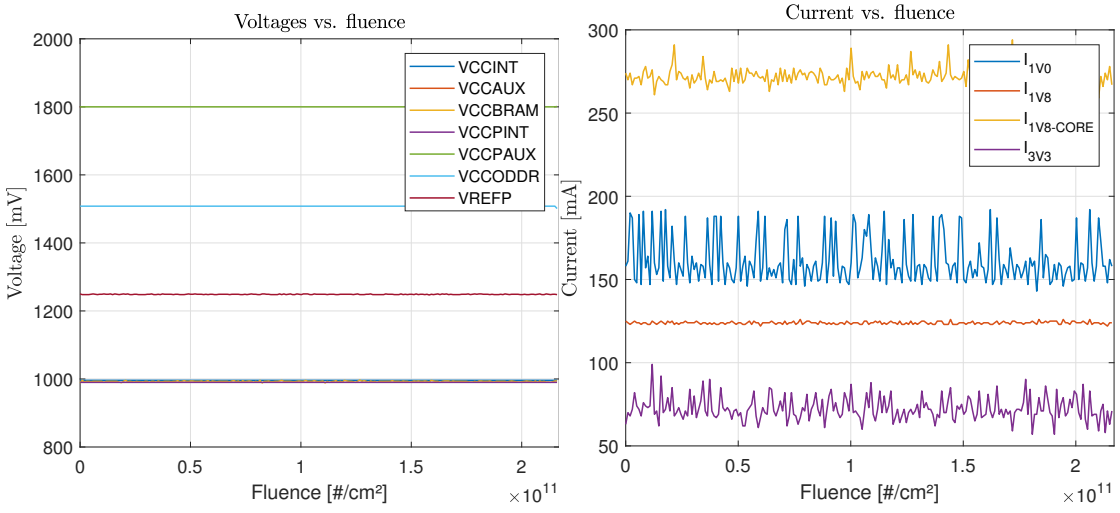
SUT	**SEE**	**#Spills**	**#Events**	**HEH$_{eq}$ fluence [#/cm^2]**	**Cross-section [device/cm^2]**	**TID [krad(Si)]**
1	Self-recover	21236	5320	$2.17 \times 10^{+11}$	2.45×10^{-8}	10
1	Power-cycle	21236	75	$2.17 \times 10^{+11}$	3.46×10^{-10}	10
1	AD9361 SEU	21236	355	$2.17 \times 10^{+11}$	1.64×10^{-9}	10
1	AD9361 SEFI	21236	8+5	$2.17 \times 10^{+11}$	6.00×10^{-11}	10
2	Self-recover	15364	3840	$1.57 \times 10^{+11}$	2.44×10^{-8}	7.2
2	Power-cycle	15364	53	$1.57 \times 10^{+11}$	3.38×10^{-10}	7.2
2	AD9361 SEU	15364	255	$1.57 \times 10^{+11}$	1.62×10^{-9}	7.2
2	AD9361 SEFI	15364	5+3	$1.57 \times 10^{+11}$	5.09×10^{-11}	7.2

Furthermore, the observed average numbers of SEUs and SEFIs of the AD9361 RFIC are presented with their corresponding cross-sections. As mentioned in the section for the CHARM test definition (section 6.2.1.1), an SD-Card was used as intermediate storage for the requested data by the OBC and for long-term data storage (e.g. for the offline housekeeping data or payload data). Unfortunately, it has been found that these SD-Cards were quite sensitive to the radiation at CHARM resulting in a partial loss of read and write operations. For SUT-1 this issue was able to be fixed during the test campaign

since it was at least able to write. For SUT-2, the full operation of the SD-Card was lost for about 71 % of the test time. Thus, the test plan and procedure only continued with SUT-1, and SUT-2 was disabled at this point. The achieved total dose for SUT-1 is about 10 krad(Si), and 7.2 krad(Si) for the SUT-2, respectively.

For any functional interrupt of the system that required either a self-triggered (*self-recover*) reboot or external *power-cycle*, an interrupted boot process has not been observed. Additionally, the scrubbing and verification process of the boot device partitions holding the kernel, ramdisk image and BOOT.bin never detected any corruption of those data. Thus, the system was always able to get into a safe and nominal operation-mode after a reboot or power-cycle.

The internal temperature, voltage and current monitoring process never triggered a reboot due to out-of-limit conditions, e.g. by sub-voltage SELs. As an example, the captured voltage and current values for SUT-1 are shown in Figure 6.11 over HEH_{eq} fluence, representing the full duration of the test campaign.



(a) Voltages (b) Currents

FIGURE 6.11: System-internal (SUT-1) measured voltages (a) and a set of system currents (b) during irradiation at CHARM, according to [174].

The voltage conditions in 6.11 (a) clearly remain constant without any degradations, e.g. due to TID effects. Similar behavior can be observed for the current values presented in Figure 6.11 (b). The dynamic current values (specifically caused by the DDR3-SDRAM and the Zynq) are to be expected due to the repeated operations and commanded execution of applications/programs by the OBC (e.g. capturing of IQ data and performing post-processing).

The mentioned processing of IQ data either includes the simple capture and storage of these or the execution of FFT operations over a series of data sets resulting in a spectrogram of the received RF data. These data are then converted to an image and

transmitted to the OBC on request. The accumulation of these spectrogram pictures for the full test span is presented in Figure 6.12 for SUT-1.

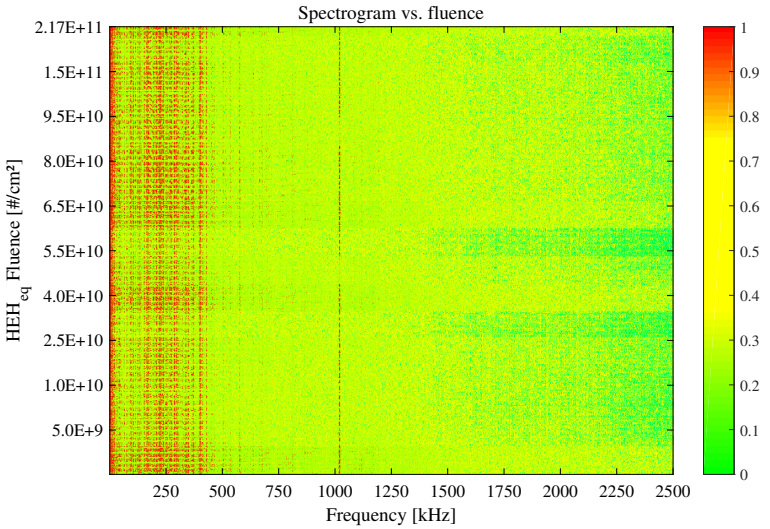


FIGURE 6.12: Spectrogram of the received RF data from the SUT-1 during irradiation at CHARM.

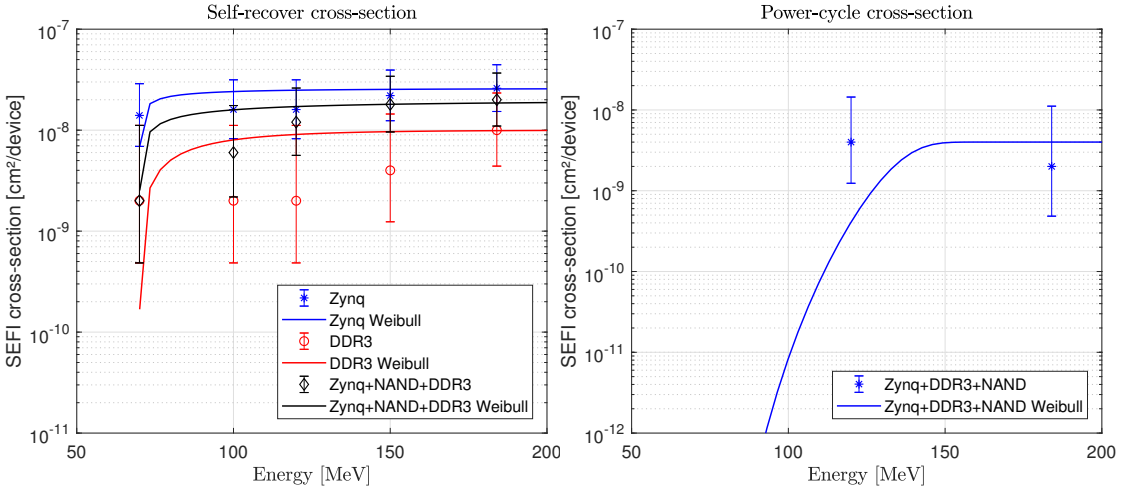
The signal that is transmitted by the corresponding reference transceiver to the SUT is a repeatedly pulsed signal (ADS-B). The carrier frequency on which the data are transmitted is set to 2.4 GHz. A set of 100 messages is transmitted within one frame. Since the messages come in bursts, a sine-wave tone of about 1 MHz is transmitted in between the messages (dotted line in the spectrogram). The later decoding of the messages that were received by the OBC showed no errors. However, it has been observed that some files and pictures were not stored correctly that was caused by system crashed during the storage operation.

6.2.2.2 Proton irradiation

The first test under proton irradiation was primarily intended to verify the results of the CHARM test with its unique mixed-field irradiation environment. Since the composition of particles and energies is very broad at CHARM, a comparison can only be made with the cross-section saturation of both results.

To further investigate the response of radiation effects on system-level, and since it has been observed at CHARM that mostly the operating system or part of it crashed, the proton beam was focused on the desired areas as described in the proton irradiation test setup and procedure. The cross-section results are presented in Figure 6.13 for self-recovered SEFIs in (a) and power-cycle events in (b) on the following page.

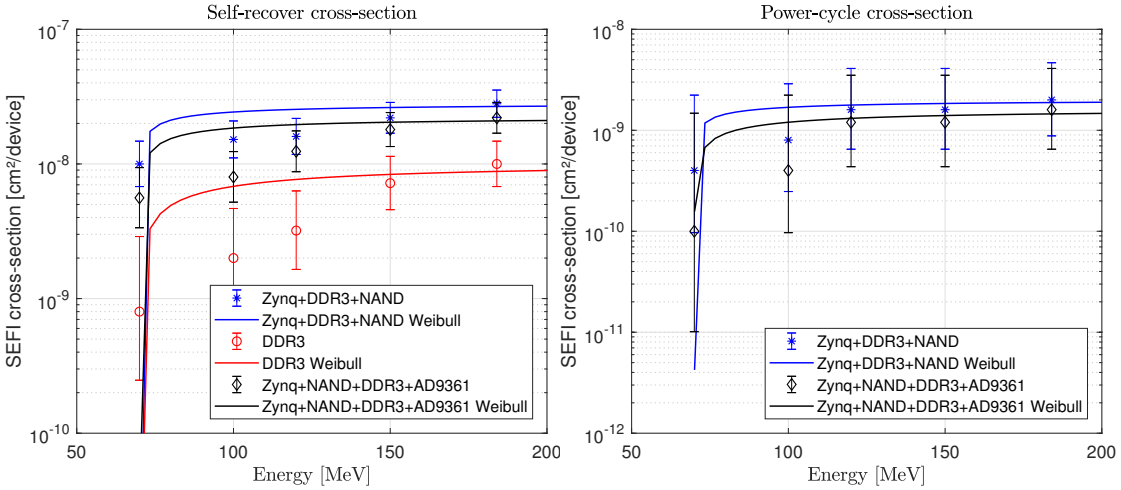
The second test campaign was performed at the final system design, without using RadHard devices with a focus on similar areas of interest as for the first proton irradiation test.



(a) Self-recovered (b) Power-cycle

FIGURE 6.13: Cross-sections for the first GSDR system-level proton test for (a) self-recovered and, (b) power-cycled SEFI.

In this test the AD9361 RFICs have also been irradiated and the Zynq-only beam configuration has been skipped. The test result cross-sections are presented in Figure 6.14. For both test campaigns neither abnormalities in the housekeeping data have been found (including temperature, voltage and current levels) nor significant SEFIs on the AD9361, which was expected due to the very low response under proton irradiation and the relatively low target fluence (see section 5.2.3).



(a) Self-recovered (b) Power-cycle

FIGURE 6.14: Cross-sections for the second GSDR system-level proton test 2 for (a) self-recovered and, (b) power-cycled SEFI.

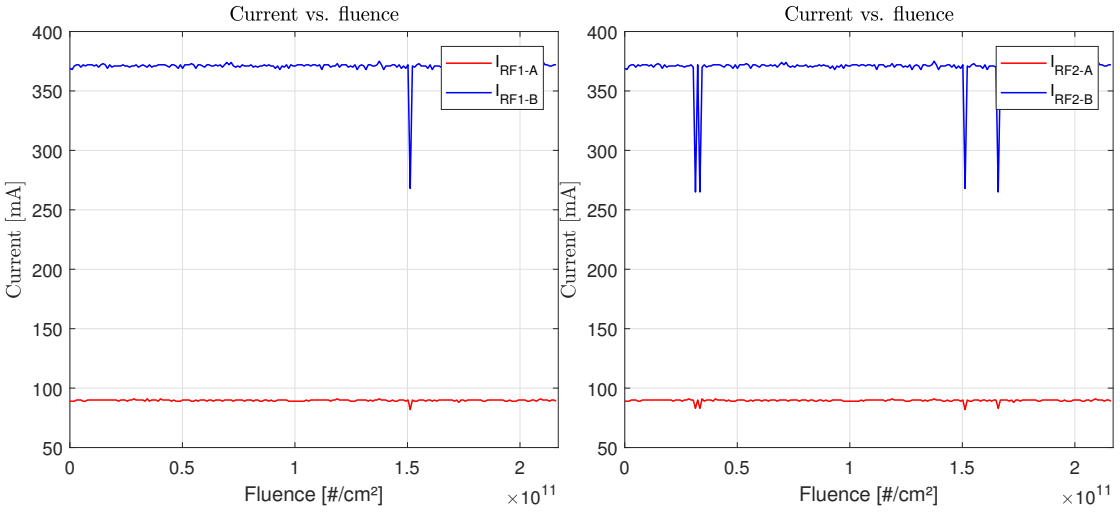
Only very few SEUs were counted but no SEFIs were observed nor corrupted data that had been captured, stored and post-processed. In the beam configuration where the NAND flash was also irradiated, upsets in the region where sensitive boot data are stored were observed but could be recovered/restored at any time by the responsible validation process. The total number of events counted for upsets in the corresponding NAND flash partitions was three in the first test campaign and seven for the second test, respectively.

The test results are further discussed in section 6.3 and later compared with each other.

6.3 Discussion

In this section the previously presented test results of the GSDR system at CHARM and KVI are discussed.

In general, all tests have shown that the GSDR system is capable of handling about 98 % of system SEFIs on its own and can recover to a nominal operation without external interaction. The system never ended up in a deadlock mode where it was not able to load boot images and start certain program executions. Even for the SUT-2 at CHARM, where the SD-Card issue led to persistent non-response to the OBC's commands and thus a continuous power-cycle, the boot sequence was successful. As expected, the failures driven by the AD9361 and therefore the direct processing of the RF data are negligible. For all test campaigns, only a few SEFIs were found that were detected and recovered by the device driver. Such SEFIs were also observed in the system-internal monitored current values, written in the housekeeping data as illustrated in Figure 6.15.



(a) RFIC-1 (b) RFIC-2

FIGURE 6.15: Current conditions of RFIC-1 (a) and RFIC-2 (b) during irradiation at CHARM.

However, such device SEFIs have not been found during the specific RF data processing that was requested by the OBC such as for the spectrogram application. Surprisingly, the validation of the sensitive boot data stored in dedicated partitions of the NAND flash device never showed a corruption of data (not even a single bit flip) at CHARM. Such results can be explained by the fairly low allocation of available data (just about 5 %) and the wide distribution of the partition in the memory. Furthermore, it is assumed that the control logic of the NAND flash is not being affected which is a reasonable assumption due to the low LET of available particles at CHARM. Nevertheless, the NAND flash has shown errors in the partition with the sensitive boot data during irradiation by proton at KVI. The number of errors found by the validation process was very low and these could always be restored (cross-section: $\approx 1.5 \times 10^{-9}\,\mathrm{cm}^2$/device). An abstract of the provided log file is presented in listing 6.1, showing the detected corruption in the NAND flash partition and the recovery process.

```
1  sha256sum: WARNING: 1 computed checksum did NOT match
2  Error: FlipProtection:Crc:  /dev/mtd2
3  Erasing 128 Kibyte @ 0x0 -
4  0% complete Erasing 128 Kibyte @ 20000 --
5  3% complete Erasing 128 Kibyte @ 40000 --
6  # --- SNIP --- #
7  96% complete Erasing 128 Kibyte @ 3e0000 --
8  100% complete
9  ECC failed: 0
10 ECC corrected: 0
11 Number of bad blocks: 0
12 Number of bbt blocks: 0
13 Block size 131072, page size 2048, OOB size 64
14 Dumping data starting at 0x00000000 and ending at 0x00400000...
15 Writing data to block 0 at offset 0x0
16 Writing data to block 1 at offset 0x20000
17 # --- SNIP --- #
18 Writing data to block 31 at offset 0x3e0000
19 ECC failed: 0
20 ECC corrected: 0
21 Number of bad blocks: 0
22 Number of bbt blocks: 0
23 Block size 131072, page size 2048, OOB size 64
```

Listing 6.1: Abstract of the error-log file for a NAND flash SEU.

As seen in line 1, the corruption within the NAND flash partition was detected by the sha256sum process which recognized that the checksum did not match. The corresponding error in line 2 was printed out and the recovery process started by erasing the content of partition mtd2. After the erase operation was successful, the backup partitions were firstly checked before copying the right data to the previously erased NAND flash partition (line 10-18). It has not been observed that two partitions were affected at the same time so that a voting could fail. After the write operation is done, the partition is again validated. The majority of SEFIs clearly resulted in filesystem crashes that

could be further investigated by the error-log that is provided by the kernel and which was recorded during irradiation. Therefore, an abstract of the error log is provided in listing 6.2. From the listing 6.2 the initial start-up is presented from line 1-2 (reading the primary application (payload) from flash and starting its execution).

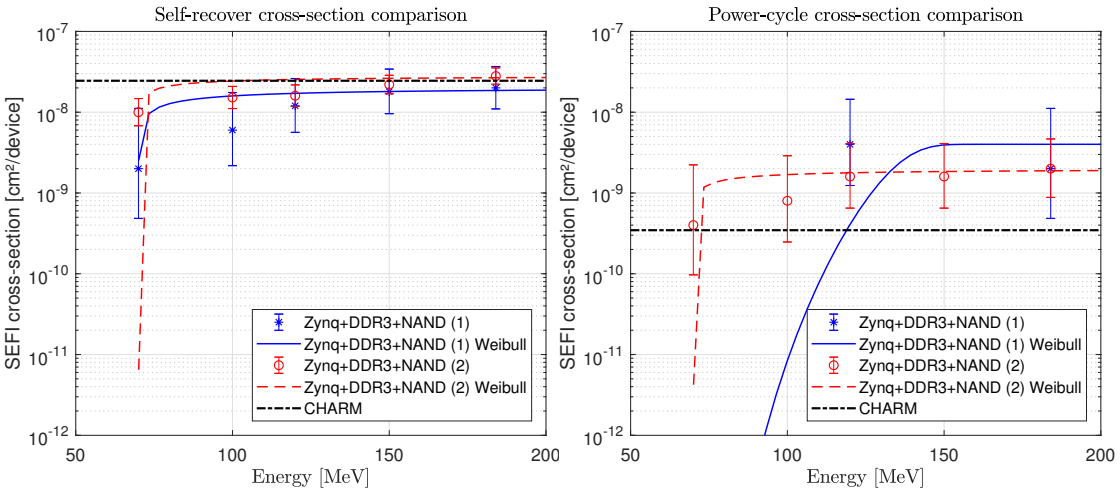
```
1  S2TEP Payload
2  Reading payload from nandflash partition 12
3  Toggle: 0
4  # --- SNIP --- #
5  ECC failed: 0
6  ECC corrected: 0
7  Number of bad blocks: 0
8  Number of bbt blocks: 0
9  Block size 131072, page size 2048, OOB size 64
10 Dumping data starting at 0x00000000 and ending at 0x00100000...
11 Toggle: 3
12 # --- SNIP --- #
13 Toggle: 20
14 Unhandled fault: imprecise external abort (0x1406) at 0xb3f0298c
15 pgd = df858000
16 [b3f0298c] *pgd=2f1b4831, *pte=3514075f, *ppte=35140c7f
17 Internal error: : 1406 [#1] PREEMPT SMP ARM
18 Modules linked in:
19 CPU: 0 PID: 981 Comm:  gsdr-payload.elf Not tainted 4.9.0 #1
20 task:  ef218640 task.stack:  ef144000
21 PC is at kernfs_path_from_node_locked+0x1e0/0x344
22 LR is at lookup_fast+0x268/0x2dc
23 pc :  [<c014bd34>] lr :  [<c00f7f74>] psr:  20030013
24 sp :  ef145d98 ip :  70672f73 fp :  49bc604e
25 r10:  d0d0d0d0 r9 :  ef2443d0 r8 :  ef145dc8
26 r7 :  eed42000 r6 :  ef145dd0 r5 :  eed4b330 r4 :  ef145ed0
27 r3 :  c014bd34 r2 :  00000000 r1 :  00000011 r0 :  eed4b330
28 Flags:  nzCv IRQs on FIQs on Mode SVC_32 ISA ARM Segment none
29 Control:  18c5387d Table:  1f85804a DAC: 00000051
30 Process gsdr-payload.elf (pid:  981, stack limit = 0xef144210)
31 Stack:  (0xef145d98 to 0xef146000)
32 # --- SNIP --- #
33 Backtrace:
34 [<c04577a8>] (_netif_receive_skb_core) from [<c04595e0>]
35 (netif_receive_skb+0x80/0x8c)
36 r10: 1f724f40 r9: df52a000 r8:00000000 r7:0880 c042
37 r6:00000001 r5: c09048e4 r4: df61ed80
38 [<c0459560>] (netif_receive_skb) from [<c045c2f8>]
39 (netif_receive_skb_internal+0x120/0x12c)
40 r5: c09048e4 r4: df61ed80
41 [<c045c1d8>] (netif_receive_skb_internal) from [<c045c314>]
42 (netif_receive_skb+0x10/0x14)
43 # --- SNIP --- #
44 [<c01cfe48>] (Sys_write) from [<c0107580 >]
45 (ret_fast_sys_call+0x0/0x48 )
46 r7: 00000004 r6: 00000001 r5: be818910 r4: be818560
47 Code: 0 a00005b e3590000 13 a08000 1 a000013 (00000000)
48 end trace 12950dc5f8bbaad0
```

Listing 6.2: Abstract of the error-log file provided by the kernel.

In line 4-9 the log-output of the validation process of the sensitive boot data within the NAND flash partition is shown (ECC-enabled and no error found). The Toggle ID is an internal counter that is displayed in the log file that verifies execution of the primary payload application.

From line 13, the output of the log-file shows the system failure interruption that is in this case caused in the primary gsdr-payload.elf application. The following output identifies which process ID is correlated to the application and that it was executed by the CPU Core 0. *Not tainted* in line 19 specifies that the error did not originate from the kernel itself. The backtrace from line 33 allows for an evaluation of what the corresponding program (gsdr-payload.elf) tried at last before (or a reason why) the system crashed. In this example the gsdr-application failed to execute a *sys_write* function.

Based on the error-log and the documentation of the ARM processor it is possible to evaluate the specific address that is responsible for the SEFI and the corresponding cache(s). As mentioned in section 5.1.1, it has been found that specific caches are responsible for most software crashes but, due to the time-critical application running during the test, all caches were enabled. However, the analysis of the error-log files has shown that also for the radiation test on the GSDR, in most cases the caches have been affected by radiation and have caused the system-functional interrupts. This is in correlation to what has been observed by [106, 135].



(a) Self-recovered (b) Power-cycled

FIGURE 6.16: Comparison of the cross-sections for self-recovered SEFIs (a) and power-cycles (b) at KVI and CHARM.

In order to compare the test results the cross-sections for both test campaigns that focused on the Zynq, NAND and DDR3-SDRAM, the cross-sections are presented in Figure 6.16. As reference, the cross-section for the CHARM tests is presented as a constant value, since an energy relationship cannot be determined due to the nature of

CHARM's radiation environment. Anyhow, for the most common system SEFI (self-recovery) presented in Figure 6.16 (a), the cross-sections for all three test are almost equal.

For SEFI cross-sections that required an external power-cycle, the results vary strongly due to the relatively low number of counted events as shown in Figure 6.16 (b). To predict the potential event rates, the maximum cross-section saturations were taken out of all three test campaigns and the results are listed in Table 6.2 for two reference missions (LEO: 800km, 98° and GEO).

TABLE 6.2: Predicted event rates (on protons) for the GSDR system.

SEE Type	**Orbit**	**Energy threshold [MeV]**	**Limit cross-section [device/cm^2]**	**Events/day (nominal)**	**Events/day (worst)**	**Ref.**
$SEFI_{Self}$	GEO	$7.00 \times 10^{+1}$	2.18×10^{-8}	1.95×10^{-2}	$1.12 \times 10^{+0}$	[32]
$SEFI_{PC}$	GEO	$7.00 \times 10^{+1}$	1.57×10^{-9}	1.32×10^{-3}	6.97×10^{-2}	[32]
$SEFI_{Self}$	LEO	$7.00 \times 10^{+1}$	2.18×10^{-8}	8.62×10^{-2}	3.50×10^{-1}	[32]
$SEFI_{PC}$	LEO	$7.00 \times 10^{+1}$	1.57×10^{-9}	5.71×10^{-3}	2.22×10^{-2}	[32]

The presented event rate predictions are only based on in-flare and out-flare proton rates using the OMERE software [32]. Thus, one can assume to have about 1 self-recovered SEFI per day in GEO under worst-case conditions and about every 8.5 days in LEO. For nominal conditions, those rates are decreased to 51.3 days for failure in GEO and about 11.6 days for LEO. Considering heavy-ions that have not been tested, the event rate is expected to be higher, especially in GEO.

6.4 Summary

This chapter has presented the system-level design and its verification under particle irradiation. In total three test campaigns have been carried out on two revisions on the GSDR. The first test was performed at CHARM, a unique mixed-field irradiation test facility run by CERN in Geneva, Switzerland. Due to its nature, the full system was irradiated with a cocktail of different particles and energies which do not allow a clear determination of radiation effects with respect to specific particles and their energy. Nevertheless, for comparison purposes to the later performed proton irradiation test an approximation to a HEH_{eq} cross-section (saturation) can be used. Two samples were tested at CHARM and besides some design issues with the data processing on-board over the SD-Card which broke on one SUT, the test was fully successful since it was always able to recover from a failure and came back to a nominal operation. It has been found that almost all failures detected were driven by Zynq and DDR3-SDRAM which

were running the OS and certain applications. Thus, a second radiation test campaign on the same hardware/prototype was performed at KVI using the proton accelerator in order to evaluate and verify the cross-section results gained in the mixed-field radiation test. Due to time constraints, only a lower target fluences were set for five energies being used. However, the cross-section saturations were almost equal, especially for the self-recovered SEFIs. SEFIs that required an external power-cycle of the SUTs were found rarely under proton irradiation. Thus, different cross-section saturations were observed. The results of CHARM and the validation of the proton-induced radiation effects characterization have been published in [174] in an abbreviated version.

The final design of the GSDR, which for the most part is a redesign in the power regulation unit, has been lastly tested again under proton irradiation at KVI with the same focus on the critical system components that have already been investigated on the previous hardware revision (Zynq, DDR3-SDRAM, NAND and AD9361). The target fluence was increased in order to improve error statistics. The test software being used was not significantly modified to ensure a further comparison to the test results that were achieved in the previous campaign at KVI and CHARM. Especially for the self-recovered SEFI events, a close match has been evaluated which verifies the previous test results and also the HEH_{eq} assumption of CHARM. For power-cycle events, not enough data was collected so that the error statistic does not allow a clear comparison.

The experience gained on the verification process of the GSDR contributed to recently published guideline for system-level RHA [172, 173].

Chapter 7

Conclusion

This thesis is devoted to the design and development of a highly integrated SDR that allows the operation of multi-band RF applications in the harsh radiation environment of space, here named GSDR. Even if SDR technologies are already well established in the space community there were big differences found between them. On one hand they were designed for highly reliable missions known for commercial space applications resulting into a stringent design of space-qualified, RadHard components with low flexibility and performance, and extremely high costs. On the other hand, they were being rapidly developed and manufactured for CubeSat missions with a low-cost driven approach using only COTS devices. Therefore, such systems are potentially more powerful and efficient due to the use of cutting edge technologies, but there is no guarantee that they will be reliable for safe operation in the harsh environment of space. These circumstances either lead to high risk acceptance or to extreme mission costs. The gap between both approaches is huge and the focus of the presented PhD thesis was to develop a design methodology that allows a analytical judgment for the use of COTS EEE components in space applications. The proposed FMECA-based risk assessment focuses primarily on radiation effects and provides a guidance for selecting EEE parts aiming to reduce the costs, decrease the risk and improve the system performance. This balance is essential for the design and development of the proposed GSDR, since the required technologies for multi-band applications are not designed for space.

The result is a unique system design that is based on RadHard and evaluated COTS EEE devices. Specifically for the mandatory RFIC that is the key-technology for achieving multi-band RF operations, own investigations for RHA were required, since it has never been tested before. Due to its high integrity and complexity, the development of a dedicated test methodology was required, which was peerless since testing such devices that combines analog, digital and RF technologies were not undertaken so far. Outstanding and detailed results were achieved by several performed TID and SEE test campaigns.

The investigated RFIC and other critical COTS parts have been successfully evaluated for their use, followed the proposed risk assessment approach in this PhD thesis.

Even though the design methodology outlined here represents a novel risk assessment approach and points to the recommended use of several COTS EEE devices, it is still crucial to verify this assumption by means of rigorous system-level radiation testing. Furthermore, such tests are also vital for verifying the functional implementation of mitigation strategies that ought to improve system reliability, such as the capability of and capacity for functional recovery. For this reason, the developed GSDR has been tested in three radiation test campaigns. The first test was carried out at a unique mixed-field radiation test facility, CHARM at CERN. Since the mixed-field approach differs from the actual radiation environment in space, such as the presence of mainly protons in a LEO mission, two proton test campaigns were conducted afterward at KVI. Due to the limited beam size, only groups of EEE parts were irradiated that have been found to be responsible for most system failures during the test at CHARM. The results were presented and compared to the cross-sections determined at the mixed-field radiation environment at CHARM. The comparison verifies the test approach of CHARM's HEH_{eq}, specifically if the error statistics are satisfied.

The GSDR showed a very good response to radiation, including a TID of greater than 10 krad(Si) and a moderate self-recovered SEFI rate occurring about every 9 days in a LEO mission under worst-case conditions (for instance, as a result of a solar flare). In any test scenario, no destructive event was observed and the system was always capable of recovering to its initial state.

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List of own publication

The following works have been carried out in the framework of the presented thesis and have been published in scientific and engineering journals as well as on international conferences:

"Design of a Highly Integrated and Reliable SDR Platform for Multiple RF Applications on Spacecrafts," J. Budroweit, *GLOBECOM 2017 - 2017 IEEE Global Communications Conference, Singapore, 2017, pp. 1-6.*

Abstract:
The utilization of Software-Defined Radios (SDR) has already become state-of-the-art for terrestrial Radio Frequency (RF) and wireless applications. The almost conservative space industry also identified the benefits of reconfigurable radio systems and uses SDRs on satellites and space vehicles. The traditional definition of a software-defined radio thereby is the digital implementation of applications in Field Programmable Gate Arrays (FPGA) or Digital Signal Processors (DSP). The analog parts (e.g. RF components) of the radio are generally tailored to the application specification and are not, or only partly, configurable. With the release of programmable and reconfigurable Radio Frequency Integrated Circuits (RFIC), a new era of SDRs was declared, which allows more flexibility and higher performance into smaller dimension. Thus, making these benefits available for applications on spacecraft has been identified as a big challenge, since those technologies are not designed for the harsh environmental conditions in space. This paper presents an approach for a highly integrated and reliable Generic Software Defined-Radio (GSDR) platform design and the results of a pre-evaluation test under radiation conditions on a prototype, to investigate certain mitigation techniques and a preconceived selection of system components. Focus of this platform is the integration into a satellite system, in order to operate multiple RF and wireless communication applications, where typically specific units for each application are used.

"Design challenges of a highly integrated SDR platform for multiband spacecraft applications in radiation enviroments," J. Budroweit and A. Koelpin, *2018 IEEE Topical Workshop on Internet of Space (TWIOS), Anaheim, CA, 2018, pp. 9-12.*

Abstract:
Software-Defined Radios (SDR) are already widely-used and often implemented in terrestrial Radio Frequency (RF) and wireless applications. Even the very conservative and slow changing space industry has identified the benefits of reconfigurable radio systems and uses SDRs on satellites and space vehicles. Nevertheless, those systems are mostly inapplicable for lower- and mid-class mission, or are often limited in performance, reliability and are only available for a specific frequency band. This paper presents the approach for a reliable and highly integrated Generic Software Defined-Radio (GSDR) platform design, using state-of-the-art RF transceiver devices to provide multi-band applications on spacecraft. Design challenges under radiation environments for this GSDR platform are discussed and results of a pre-evolution test under selected radiation condition on a prototype are presented.

"Total Ionizing Dose Effects on a Highly Integrated RF Transceiver for Small Satellite Radio Applications in Low Earth Orbit," J. Budroweit and M. Sznajder, *2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 2018, pp. 1-6*

Abstract:
Software-Defined Radios (SDR) are commonly used in state-of-the-art radio systems and are already well established in the space industry. A SDR usually describes the signal processing of a radio application in software and is often implemented into Field Programmable Gate Arrays (FPGA) or Digital Signal Processors (DSP). Most RF front-ends are strictly specified and realized for an executed application and are thus not re-configurable. With the release of new Radio Frequency Integrated Circuit (RFIC) devices, a significant portion of RF front end specifications have become programmable and alterable. This paper presents the use case and selected radiation test results of such RFIC technologies for small satellite radio applications, primary designed for low earth orbit (LEO) missions.

"In-Situ TID Testing and Characterization of a Highly Integrated RF Agile Transceiver for Multi-Band Radio Applications in a Radiation Environment," J. Budroweit and M. P. Jaksch, *2019 IEEE International Conference on Wireless for Space and Extreme Environments (WiSEE), Ottawa, ON, Canada, 2019, pp. 1-6*

Abstract:
In this paper, the in-situ testing and characterization of an highly integrated radio frequency (RF) agile transceiver in an radiation environment is presented. The device under test (DUT) is exposed by γ-rays to evaluate the total ionizing dose effects. The

advance in-situ test setup allows detailed analysis of the DUT's RF performance. The test procedures and methods are described and particular test results are shown. The DUT has been irradiated to a total ionizing dose of ≈190 krad and has not shown any conspicuous degradation effects or malfunctions.

"Proton Induced Single Event Effect Characterization on a Highly Integrated RF-Transceiver," J. Budroweit, Jaksch and M. Sznajder, *Electronics. 2019; 8(5):519.*

Abstract:
Radio frequency (RF) systems in space applications are usually designed for a single task and its requirements. Flexibility is mostly limited to software-defined adaption of the signal processing in digital signal processors (DSP) or field-programmable gate arrays (FPGA). RF specifications, such as frequency band selection or RF filter bandwidth are thereby restricted to the specific application requirements. New radio frequency integrated circuit (RFIC) devices also allow the software-based reconfiguration of various RF specifications. A transfer of this RFIC technology to space systems would have a massive impact to future radio systems for space applications. The benefit of this RFIC technology allows a selection of different RF radio applications, independent of their RF parameters, to be executed on a single unit and, thus, reduces the size and weight of the whole system. Since most RF application sin space system require a high level of reliability and the RFIC is not designed for the harsh environment in space, a characterization under these special environmental conditions is mandatory. In this paper, we present the single event effect (SEE) characterization of a selected RFIC device under proton irradiation. The RFIC being tested is immune to proton induced single event latch-up and other destructive events and shows a very low response to single failure interrupts. Thus, the device is defined as a good candidate for future, highly integrated radio system in space applications.

"In-Situ Testing of a Multi-Band Software-Defined Radio Platform in a Mixed-Field Irradiation Environment," J. Budroweit, S. Mueller, M. Jaksch, R.G. Alia, A. Coronetti and A. Koelpin, *Aerospace. 2019; 6(10):106.*

Abstract:
This paper presents an in-situ test concept for a multi-band software-defined radio (SDR) platform in a mixed-field radiation environment. Special focus is given to the complex automated test setup with respect to the requirements of the irradiation facility. Additionally, selected test results of a system-level evaluation are presented and discussed. For the verification of the mixed-field radiation environment, the software-defined radio (SDR) was also tested under proton irradiation. The cross-sections for the observed single event effects are compared and show similar results.

"Heavy Ion Induced Single Event Effects Characterization on an RF-Agile Transceiver for Flexible Multi-Band Radio Systems in NewSpace Avionics," J. Budroweit, M. Jaksch, R.G. Alia, A. Coronetti and A. Koelpin, *Aerospace. 2020; 7(2):14.*

Abstract:
Nowadays, technologies have a massive impact on the design of avionic systems, even for the conservative space industry. In this paper, the single event effect (SEE) characterization of a highly integrated and radio frequency (RF) agile transceiver is being presented which is an outstanding candidate for future radio systems in NewSpace applications and space avionics. The device being investigated allows programmable reconfiguration of RF specifications, where classical software-defined radios (SDR) only define an on-demand re-configuration of the signal processing. RF related configurations are untouched for common SDR and developed discretely by the specific application requirements. Due to the high integrity and complexity of the device under test (DUT), state-of-the-art radiation test procedures are not applicable and customized testing procedures need to be developed. The DUT shows a very robust response to linear energy transfer (LET) values up to $62.5\,\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, without any destructives events and a moderate soft error rate.

"Design of a fully-integrated Telemetry and Telecommand Unit for CCSDS Spacecraft Communication on a Generic Software-defined Radio Platform," J. Budroweit, T. Gaertner and F. Greif, *2020 IEEE Space Hardware and Radio Conference (SHaRC), San Antonio, TX, USA, 2020, pp. 13-15*

Abstract:
This paper presents the design of a fully-integrated Telemetry and Telecommand unit for spacecraft communication on a generic software-defined radio platform. The implementation is compliant to the CCSDS standard and allows high flexibility in reconfiguration of the physical layer and data link layer. A state-of-the-art TMTC architecture is presented and is compared to the proposed design approach.

"Design of a multi-channel ADS-B receiver for small satellite-based aircraft surveillance," J. Budroweit, M. P. Jaksch and T. Delovski, *2019 IEEE Radio and Wireless Symposium (RWS), Orlando, FL, USA, 2019, pp. 1-4*

Abstract:
In this paper we discuss the design and implementation of a multi-channel ADS-B receiver as an approach to solving the known issues for satellite-based aircraft surveillance. The presented approach is designed to be implemented and tested on an already developed highly integrated generic software-defined radio platform for spacecraft application. The multi-channel ADSB receiver implementation is presented and first test results are given.

"Implementation of a HDL-Coder based telecommand receiver application for microsatellite communication," J. Budroweit, F. Stehle, C. Willuweit and D. Wuebben, *2018 IEEE Global Conference on Signal and Information Processing (GlobalSIP), Anaheim, CA, USA, 2018, pp. 1063-1067*

Abstract:
In this paper the development and implementation of a Telecommand (TC) receiver application for microsatellite communication is presented. The TC receiver application is executed and operated by a highly integrated Generic Software-Defined Radio (GSDR) platform. This platform architecture is designed for the reliable operation of multiple radio frequency applications on spacecraft. For the development and implementation process of the TC receiver application, a new model-based development workflow by Matlab/Simulink is used and evaluated.

"Software-defined radio with flexible RF front end for satellite maritime radio applications," J. Budroweit, *CEAS Space Journal 8, pp. 201-213 (2016)*

Abstract:
This paper presents the concept of a software-defined radio with a flexible RF front end. The design and architecture of this system, as well as possible application examples will be explained. One specific scenario is the operation in maritime frequency bands. A well-known service is the Automatic Identification System (AIS), which has been captured by the DLR mission AISat, and will be chosen as a maritime application example. The results of an embedded solution for AIS on the SDR platform are presented in this paper. Since there is an increasing request for more performance on maritime radio bands, services like AIS will be enhanced by the International Association of Marine Aids to Navigation and Lighthouse Authorities (IALA). The new VHF Data Exchange Service (VDES) shall implement a dedicated satellite link. This paper describes that the SDR with a flexible RF front end can be used as a technology demonstration platform for this upcoming data exchange service.

"Ultra-High Total Ionizing Dose Effects in a Highly-Integrated and RF-Agile Transceiver," J. Budroweit, M. Jaksch and G. Borghello *2020 IEEE Radiation Effects Data Workshop (in conjunction with 2020 NSREC), Santa Fe, NM, USA, 2020, pp. 1-4*

Abstract:
This paper presents the characterization of total ionizing dose (TID) effects on an highly-integrated radio frequency (RF) agile transceiver to ultra-high dose levels. The DUT shows no RF-specific degradation up to 40 Mrad(SiO_2). Malfunctions on the digital interfaces are assessed at ≈45 Mrad(SiO_2) which results into a non-functional operation of the DUT. Additional TID testing to 80 Mrad(SiO_2) has been performed to investigate further behavior. Rebound effects during 100 °C tempered post-test annealing to almost nominal operations are observed.

"RHA Through System Level Testing: Risk Acceptance, Facility Requirements, Test Methodology and Applications," A. Coronetti, R. Garcia Alia, R. Ferraro, S. Danzeca, CERN, Switzerland, J. Budroweit, German Aerospace Center (DLR), Germany, T. Rajkowski, P. Wang, 3D-Plus, France, I. da Costa Lopes, K. Niskanen, V. Pouget, F. Saigné, A. Touboul, University of Montpellier 2, France, D. Soderstrom, A. Javanainen, H. Kettunen, University of Jyväskylä, Finland, C. Cazzaniga, STFC, United Kingdom, J. Mekki, F. Manni, D. Dangla, CNES, France, A. Koelpin, BTU, Germany, R. Germanicus, University of Caen Normandie, France *IEEE Transaction on Nuclear Science, 2021*

Abstract:
Functional verification schemes at a level different than component-level testing are emerging as a cost-effective tool for those space systems for which the risk associated to the lower level of assurance can be accepted. Despite the promising potential, system-level radiation testing can be applied to the functional verification of systems under restricting intrinsic boundaries. Most of them are related to the use of hadrons as opposed to heavy ions. Hadrons are preferred for the irradiation of any bulky system in general because of their deeper penetration capabilities. General guidelines about the test preparation and procedure for a high-level radiation test are provided to allow understanding which are the information that can be extracted from this kind of functional verification schemes in order to compare them with the reliability and availability requirements. The use of a general scaling factor for the observed high-level cross-sections allows converting test cross-sections into orbit rates.

"Risk Assessment for the Use of COTS Devices in Space Systems under Consideration of Radiation Effects," J. Budroweit and H. Patscheider, *Electronics (ISSN 2079-9292)*, 2021

Abstract:
In this paper, a new approach is presented to assess the risk of using commercial off-the-shelf (COTS) devices in space systems under consideration of radiation effects that can dramatically affect reliability and performance. In the NewSpace era, the use of COTS has become mandatory, since typical space-qualified (class-1) electrical, electronic and electromechanical (EEE) components for space missions are no longer attractive due to their extremely high costs, long lead times and low performance. This paper sets out the usual constraints for COTS devices and proposes a guideline on how to select non-space-qualified components and when class-1 EEE devices are recommended for use.

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