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COMPARISON OF SINGLE ENDED AND DIFFERENTIAL SIGNALLING FOR WIRED BIOMEDICAL IMPLANTS USING SPI COMMUNICATION WITH REED SOLOMON ERROR CORRECTION CODES

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ABSTRACT
For an implantable system for the recording of brain signals from neonatal mice the design specifications for the weight and the size of a implantable system are very tough. The animals are very small and light weight (1-3 cm, 2-3 g) and the recording data rate is very high (3,5 Mbit/s). Thus, the system has to be extremely small. With state of the art technique it is not possible to set up a wireless implantable system that is suitable for a neonatal mouse. Thus a wired system is developed. For the wired system the connector is a size limiting factor. In wired transmission systems single ended and differential signalling are available. Differential signalling is more robust against noise disturbances, single ended transmission is beneficial with respect to a minimum number of wires and chip area. A detailed comparison of the suitability of both transmission types for wired implantable systems has been performed. A Serial Peripheral Interface connection with Reed Solomon Encoder connection has been implemented. Reed Solomon Error Correction is used to correct the errors occurring on the wired transmission line. Measurements of data rate and error rate for single ended and differential signalling have been performed for long cables (up to 1.8 m). It could be shown that single ended transmission is favourable for the desired application. For the detection and correction of errors occurring on high speed Serial Peripheral Interface Reed Solomon decoding on FPGA was used. This particular decoder design has capability of correcting up to 2 symbol errors on a packet of data composed of 9 symbols where each symbol is 4 bits long. Complete error correction takes about 65 clock cycles on a speed up to 100 MHz.

KEY WORDS
Data and Signal Acquisition, Biomedical Devices, Single Ended Signalling, Wired Biomedical Implants, SPI Communication, Reed Solomon Error Correction Codes

1 Introduction

In the research of diseases like certain forms of epilepsy and the research of the development of the brain genetic mouse disease models are used [1], [2]. Of special interest is the neonatal period [3]. In this period the mice are very small (1 - 3 cm) and have a very low weight (2 - 3 gramms). With state of the art recording technique a long-term recording is not possible [7], [5], [4]. Thus, a custom designed integrated circuit has been developed [6] that can fit into an implantable system.

For a wired implantable system the size of the connector is often critical and a size limiting factor. The smaller the connector the smaller is the stress on the subject and the less is the influence on the experiments. The size of the connector is mainly affected by the number of wires that have to be connected.

Additionally, behavioural experiments are conducted in neuroscience research, where the subject has to perform experiments and runs around in a cage. During these tasks signals from the brain are recorded with high data rate. Communication over long wires (up to 2 m) is therefore necessary. The recording systems are connected through wires to a computer. The size and the weight of the cable limits the movements of the subjects. Therefore, the wire dimensions mus be kept to a minimum.

In wired transmission systems single ended and differential signalling are distinguished. Differential signalling is more robust against transmission errors, while single ended transmission uses only half the number of wires. The two types of transmission are compared by using a SPI Interface on different types of wires. To correct errors that might occur on the wired transmission line Reed Solomon Error Correction Coding has been implemented.

The two transmission methods are compared, the number of errors are analysed and the suitability for wired biomedical implants is analysed in detail.

1.1 Error Types in Wired Communication

In digital communication, information between two ports is transmitted through a transmission channel. As the receiver receives the incoming signal, it compares it to an internal threshold voltage level and interprets that as either logic 1 or logic 0. However, the signal can be corrupted and this creates error on the communicated data.

Theses errors are caused e.g. by external electromag-

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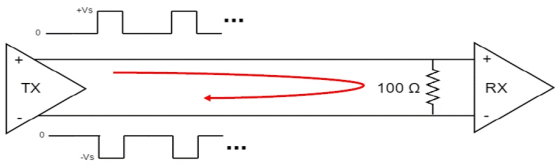

Figure 1. Low Voltage Differential Signalling Structure

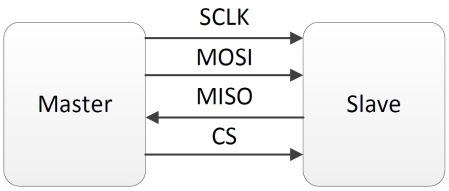

Figure 2. SPI Communication Block Diagramm

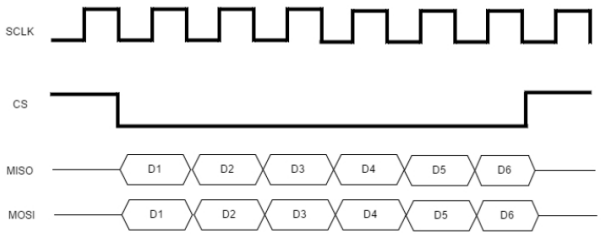

Figure 3. SPI Communication Timing Diagram

netic interference, propagation delays and reflections on the transmission line. They can be classified into two main categories:

1.1.1 Single Bit Errors

A single bit error is an isolated error condition, which alters one bit and does not change nearby bits. This can occur in the presence of white noise. Single bit errors are the least likely type of errors in serial data transmission [8].

1.1.2 Burst Errors

Burst errors on the other hand have more than two bits corrupted. They are more common and more difficult to deal with. Burst errors can be caused e.g. by an impulse noise from an external source or crosstalk between the channels of a transmission line [8].

1.2 Single Ended and Low Voltage Differential Signalling

In wired data transmission systems two types of the wiring are differentiated: single ended and differential signalling. In single ended transmission every signal has a dedicated transmission line. In differential signalling, the single line becomes two current carrying conductors routed together (usually twisted to improve cancelling), with the current in one conductor always equal in magnitude but opposite in direction to the other conductor. This causes electromagnetic fields cancelling each other [7].

Fig. 1 shows the Low Voltage Differential Signalling (LVDS) structure with both ends of the transmission line. A constant current of typically I = 3.5 mA is injected from the transmitter side. The direction of the current flowing through the termination resistor determines the logic level while receiver senses the differential voltage across the termination resistor. Typical values for the transmission are a 350 mV swing voltage with 1.4V offset voltage (3.3V or 2.5V supply voltage to drivers).

The main advantages of differential signalling are a higher robustness against common mode noise and a lower voltage swing. Single ended signalling has the advantage that it needs only half the number of wires. This significantly reduces the size of the connector that is needed for a wired implantable system. The reduced number of wires results also in advantages for the design on chip level: the number of Input/Output (I/O) pads for the digital communication is halved, this reduces the chip area.

LVDS can also improve signal integrity concerns at higher speeds. Higher frequencies and wider bit widths can cause transmission line reflections and crosstalk. As the system loading increases, the characteristic impedance of a system can change and cause impedance mismatches, which will, in turn, send reflective signals across the transmission line. These reflections can cause bit errors or increase settling times making timing budgets more difficult when speed increases.

1.3 SPI Communication

The communication protocol for data transmission was chosen to be Serial Peripheral Interface (SPI) communication. It utilizes the four signals:

- Serial Clock (SCLK)
- Master Out Slave In (MOSI)
- Master In Slave Out (MISO)
- Chip Select (CS)

It is a synchronous communication with a Master-Slave communication. A block diagram and a timing diagram of the communication are shown in Fig. 2 and Fig. 3.

2 Reed Solomon Error Correction

The decoder is designed for overcoming the errors occurring at high speed transmission. The ability of Reed

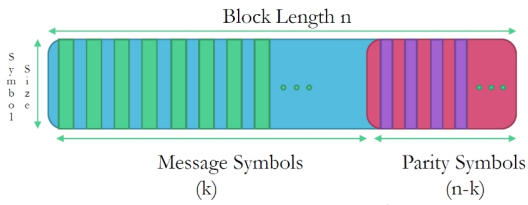

Figure 4. Data package: 20 data bits and 16 error correction bits.

Solomon (RS) codes to correct symbol errors comes from the fact that it uses univariate polynomials over finite fields. Since it uses symbols rather than binary coding, it works best against burst error type. Amount of correctable burst error depends on the designer by increasing the overhead which is attached to end of data symbols. It is a systematic code, this means that the construction of the overhead symbols (parity bits) does not alter the message symbols. In this work, 2 symbol error correction on a data packet composed of 9 symbols is selected which generally described as (9,5) RS code.

The data package consists out of 36 bit. A block structure is given in Fig. 4. Reed Solomon encoder work on symbols. With a symbol size of 4 bits, the data package of 20 bits can be represented with 5 symbols. Additionally 4 symbols for error correction are added.

RS Codes work on finite fields or Galois field (GF) [9], [12]. The elements of the GF are constructed with a specific polynomial called primitive polynomial. This is selected as:

$$p(x) = 1 + x + x^4. \tag{1}$$

The root of the primitive polynomial is α. The different powers of α are the elements of the Galois Field. In this case, since the symbol size is 4 bits, the field size is 16.

2.1 REED SOLOMON ENCODER

The purpose of the Reed Solomon (RS) encoder is to calculate and attach the parity symbols at the end of a message packet. By adding this redundancy information, error correction is possible. The generator polynomial is defined by the error correction capability. It is selected to be

$$g(x) = x^4 + 13x^3 + 12x^2 + 8x + 7. \tag{2}$$

The remainder of this division is attached to the end of message symbols. Hence at the decoder side, the received data package will be divisible by the generator polynomial. If there is any change in the code, i.e. error occurred, then the message will not be divisible by the same generator polynomial any more.

Fig. 5 shows the hardware implementation of RS encoder.

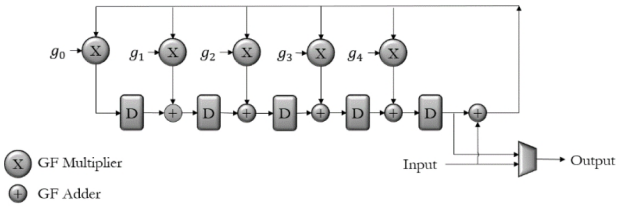

Figure 5. Hardware implementation of RS Encoder: The factors g_0 to g_4 are the constants of the generator polynomial. Multiplication and addition operations are done in Galois field. After all the bits are cycled through the loop, the register tabs will hold the remainder. These data are attached to the end of the message symbol train.

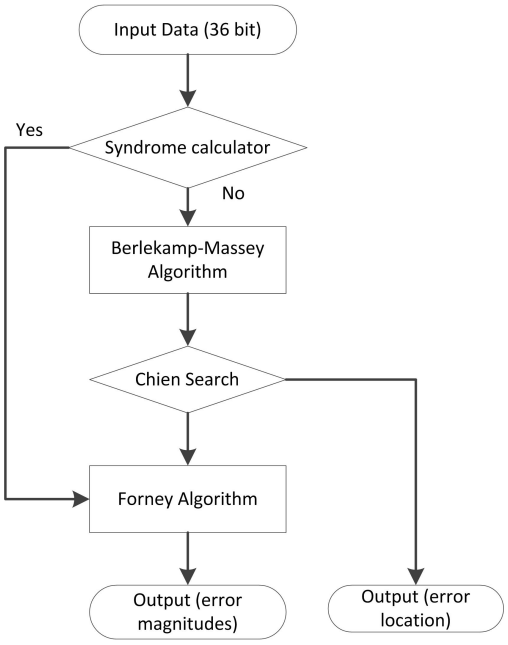

Figure 6. Reed Solomon Decoder Block Diagram

2.2 REED SOLOMON DECODER

There are different ways of decoding the RS codes presented in literature. In this paper syndrome based decoding with Berlekamp-Massey (B-M) algorithm is used [10]. The decoder is composed out of four individual components. Fig. 6 shows a block diagram of the decoder.

2.2.1 Syndrome Calculator

The syndrome calculator module takes the data packet (36 bits) and calculates four unique numbers called syndromes. The syndromes indicate whether the data is corrupt or not. If all four of the syndromes are zero, the received data packet is without errors.

2.2.2 Berlekamp-Massey Algoritm

After the syndromes are calculated the next step is to find the error locator polynomial. This step can be realized e.g. with the B-M Algorithm. A realisation is described in [11]

2.2.3 Chien Search

The roots of the error locator algorithm show the error location in terms of powers of α. The Chien Search algorithm scans the entire GF elements and puts it inside the error locator polynomial. If the result is 0, this shows that this particular element is the root. Since the encoder corrects up to 2 errors, there can be only 2 roots of the error locator polynomial.

2.2.4 Forney Algorithm

Next step is to find how far these error diverted from the original message. In other words, the magnitude of the error is calculated. The Forney algorithm is used to calculate these distances [11].

2.2.5 Error Corrector

After Forney Algorithm module, the last step is to correct the data packet since now locations and magnitudes of the errors are known.

3 MEASURMENT SETUP

A block diagram of the experimental set-up is shown in Fig. 7. The design was implemented on a Xilinx Spartan 6 Field Programmable Gate Array (FPGA) on Opal Kelly XEM6010 development board. The set-up consists of the development board, a wired connection from Master to Slave and an USB connection to a computer. The master and slave for the SPI communication are implemented on the FPGA. The wired channel can be changed to test the transfer over different wire types and lengths. The master also controls all other modules using 1-bit long ready and go flags. A micro controller handles the USB connection and streams the data to a computer.

3.1 SPI communication

Observability and accessibility of the communication and the states were required for the experiment. For the implementation of the SPI communication a state machine has been implemented. The state machine is depicted in Fig. 8. It starts with idle state and waits for a start flag. In the sending state the slave sends bits through wired channel and master receives it. The master checks for errors using the syndrome calculator. If errors are detected, the decoder gets activated. The state machine enables a continuous transmission until the transmission is terminated.

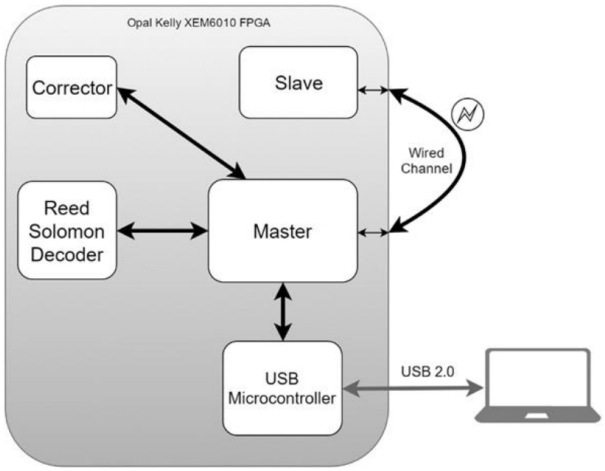

Figure 7. Experimental Setup Block Diagramm

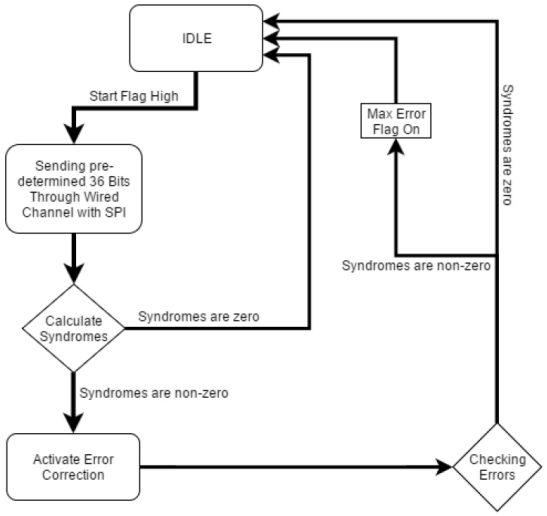

Figure 8. State machine SPI communication

A user interface (UI) has been developed to see the error locations and magnitudes in real-time.

3.2 Experimental Method

In the experiments the system was used with different clock frequencies, cable lengths and transmission types. For the experiments a special very light and flexible SPI cable from the company Intan was used. It has a length of l = 1.80 m and it is optimized for experiments with moving subjects [15]. For comparison, the experiments where also performed with a cable of cable of l = 0.20 m (26 AWG jumper cable). During the transmission the channel where observed for errors while monitoring the User Interface.

Two different signalling techniques where used and compared: Single Ended Signalling and LVDS.

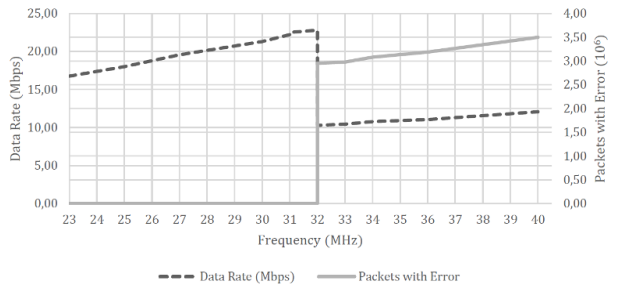

Figure 9. Measurement results for single ended transmission using a cable with a length of l = 0.2 m showing a critical frequency of above 31 MHz.

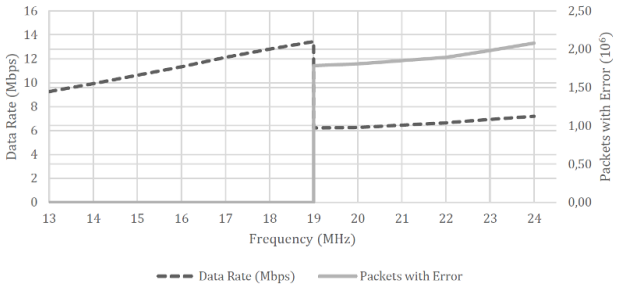

Figure 10. Measurement results for single ended transmission using a SPI cable with a length of l = 1.8 m showing a critical frequency of above 17 MHz.

For a measurement time of Δt the number of transmitted data packets and errors where recorded. The data rate was calculated according to:

$$DataRate = \frac{Number\ of\ Packets\ Sent\ *\ 36bits}{\Delta t} \tag{3}$$

For each experimental set-up measurements with varying clock frequency have been performed.

4 RESULTS

4.1 Single Ended Transmission

The measurements showed that there are critical frequencies for both type of wires where they fail to deliver error free communication. These critical frequencies depend on the wire type and the type of signalling. Below the critical frequency the system runs almost without any errors. Above the critical frequency the symbols start to show errors and an additional delay appears between two data packets.

Measurement results for single ended transmission on a short cable with a length of l = 0.20 m (26 AWG) and a long cable with a length of l = 1.80 m (SPI cable) are shown in Fig. 9 and Fig. 10. In both type of wires, after a critical

Table 1. Maximum frequency and effective data rate for single ended signalling for different wire length.

Wire Length	Maximum Frequency	Maximum Data Rate
0.20 m	32.32 (MHz)	22.78 (Mbit/s)
1.80 m	17.20 (MHz)	12.16 (Mbit/s)

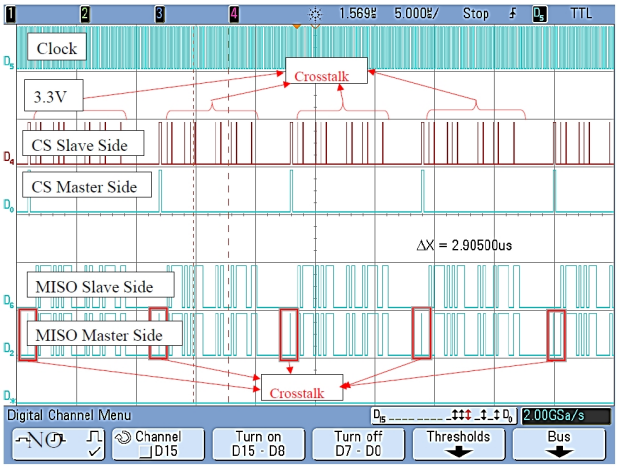

Figure 11. Single Ended Transmission using a SPI cable with a length of l = 1.8 m operating at 12.10 MHz showing crosstalk

frequency, the number of packets with errors jumps from zero to 100 %. At that point, the decoder attempts to correct the errors. However, since there are more than two symbol errors, the decoder fails to correct the errors. By using the single ended signalling method, maximum frequencies for operation as well as data rate without any errors are given in Tab 1.

Below the critical frequency the main reason for signal distortion was found to be crosstalk between the inner channels of the cable. This crosstalk creates disturbance on one channel. Below the critical frequency these signal distortions did not lead to bit errors in the data transmission in the performed measurements.

In Fig. 11 the CS line on the slave side as well as on MISO line at master side show short burst changes occurring with a specific pattern. Specifically, the CS Slave is affected. It can be seen that changes on the CS slave matches with the negative edge of the MISO line. This indicates that these signal disturbances are not coming from external sources. The crosstalk however, does not produce an error on the line because the changes are too transient for the I/O port from the receiver to sample these interferences on the lines. However, as the frequency increases, the bit time window for an error gets smaller. Therefore, after a critical frequency, all the changes start to accumulate and appear as bits on an I/O port and the communication fails.

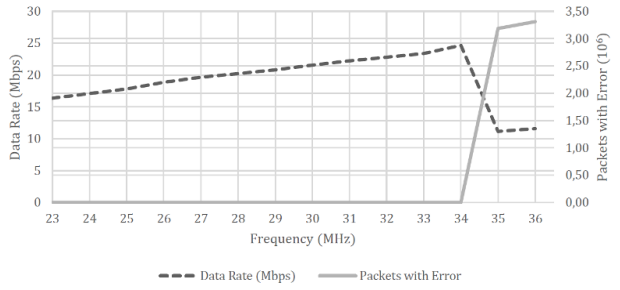

Figure 12. LVDS measurement results using a cable with a length of l = 0.2 m showing a critical frequency of above 34 MHz.

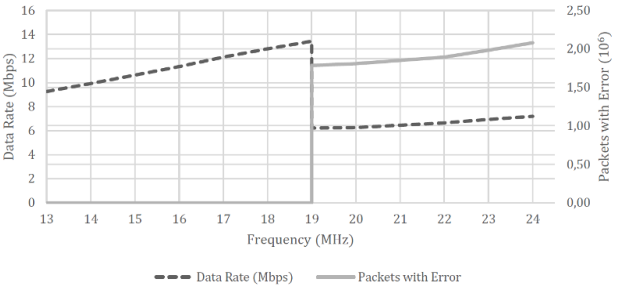

Figure 13. LVDS measurement results using a SPI cable with a length of l = 1.8 m showing a data rate of above 13 Mbit/s.

4.2 LVDS Results

The results for the LVDS measurements are shown in Fig. 12 and Fig. 13. The LVDS transmission shows a characteristic similar to the single ended transmission but with a slightly higher critical frequency.

In Tab. 2 it can be seen that for the short cables the maximum frequency that works without error has increased by 2.58 MHz while the data rate increased by 1.87 Mbit/s. On the other hand, the long cable showed a 1.80 MHz increase in the maximum frequency and a corresponding 1.27 Mbit/s increase in data rate.

Similar crosstalk issues that were discovered on single ended transmission was observed with the LVDS measurements.

As can be seen from Fig. 14, there are small burst changes on the CS Negative and MISO Positive lines. The CS negative line and MISO negative line show changes at MISO positive lines falling edge. Lines that are affected by crosstalk do not depend on the arrangement inside the cable. Since the SPI cable has 12 inner channels the same experiments were tested through different channels and crosstalk was observed on different channels as well.

The analogue measurement of the line with crosstalk is shown in Fig. 15. The crosstalk, the sudden voltage drops on the line, are indicated with red arrows.

Table 2. Maximum Frequency and Data Rate Values for LVDS transmission for different wire length.

Wire Length	Maximum Frequency	Maximum Data Rate
0.20 m	34.90 (MHz) (+8%)	24.65 (Mbit/s) (+8%)
1.80 m	19.00 (MHz) (+10%)	13.43 (Mbit/s) (+10%)

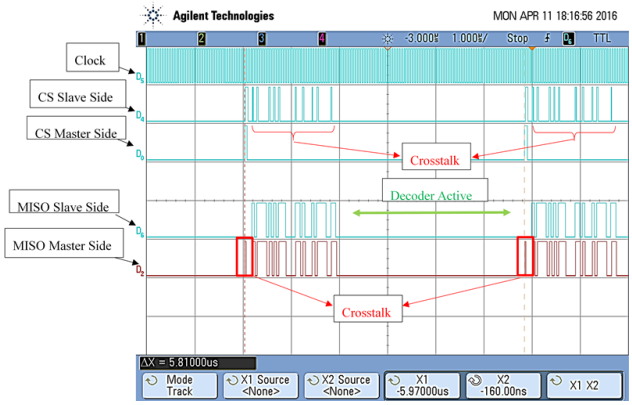

Figure 14. LVDS transmission using a SPI cable with a length of l = 1.8 m operating at 18.39 MHz showing crosstalk.

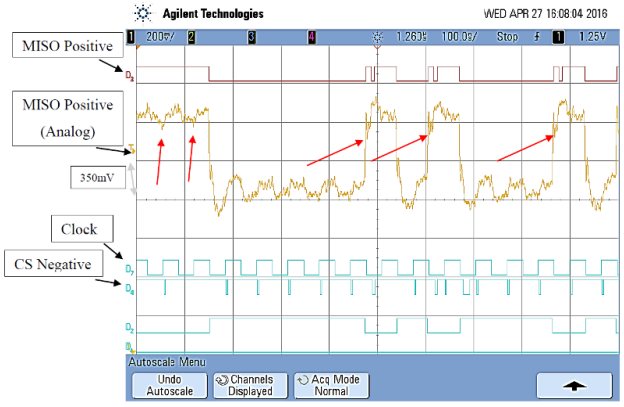

Figure 15. Analogue recording of a LVDS transmission using a SPI cable with a length of l = 1.8 m operating at 18.39 MHz showing crosstalk.

It was found that LVDS method gives improved performance over the single ended method of communication over longer distance communication. Performance showed approximately a 9 percent improvement.

5 Conclusion

A detailed comparison of errors and data rates on single ended and LVDS transmission lines has been performed. A SPI protocol with variable frequency was analysed, Reed Solomon coding was implemented into the system for error detection and correction. The results showed an improvement of less than ten percent in differential signalling compared to single ended signalling. These results show that for a wired implantable biomedical system a detailed requirement analysis is necessary.

As long as the data rate is low compared to the critical frequency of the transmission system it can be recommended to use single ended transmission. Single ended transmission is beneficial compared to differential signalling in terms of number of wirings and connector area.

Acknowledgment

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