Bidirectional System on Chip for Intracorporeal Pressure Measurement

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Abstract

A multichannel pressure sensing integrated circuit utilizing wireless power and wireless data transmission for long term monitoring of patients following endovascular stent implantation has been developed in partial fulfillment of the degree of Doctor of Engineering. Each of the 8 capacitance to digital converter signal conditioning chains is a fully differential architecture from signal input to the digital output sampled at 4ksps with 3μW power consumption per channel. Power is supplied to the device using wireless radio frequency power transmission, and the signal conversion is performed using a single stage operational transconductance amplifier and a 10 bit fully differential charge redistribution ADC. The pressure sensing IC has integrated energy harvesting, power regulation, and wireless data interface electronics.

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To my loving wife, Stefanie, and my two wonderful daughters,
Charlotte and Louisa.

Acknowledgements

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Glossary

η_{gm}	$\eta_{\mathrm{gm}} = \frac{gm}{I_d}$ MOSFET transconductance efficiency
ω	Frequency in radians per second $\omega = 2\pi f$
ω_o	Variable indicating center frequency or resonant frequency in radians per second
σ	Standard Deviation
σ^2	Variance
τ	Exponential decay time constant
f	Frequency in Hertz
f_{t}	MOSFET intrinsic gain bandwidth product $f_{\mathrm{t}} = gm/C_{gs}$
f_{v}	VCO frequency
f_o	Variable indicating center frequency or resonant frequency in Hertz
gd	$gd = \frac{\partial Id}{\partial V_{\mathrm{ds}}}$ MOSFET output conductance
gm	$gm = \frac{\partial Id}{\partial V_{\mathrm{gs}}}$ MOSFET transconductance
k'	$\frac{\mu_o C_{\mathrm{ox}}}{2n}\frac{W}{L}$ the MOSFET manufacturing constants
k_{e}	The ratio of the RX electronics envelope detector cutoff frequency to the AM carrier
k_{m}	The ratio of the AM message frequency to the AM carrier
n	The number of inductor wire loop turns per unit length
r_o	$r_o = \frac{1}{gd}$ MOSFET output resistance
s	$s = j\omega$ Laplace transform variable
A_{cl}	$A_{\mathrm{cl}} = \frac{V_{out}}{V_{in}}$ The closed loop gain
A_o	The open loop gain of an amplifier
C_{dg}	MOSFET drain gate capacitance
C_{ds}	MOSFET drain source capacitance
C_{oss}	$C_{\mathrm{oss}} \approx C_{\mathrm{ds}} + C_{\mathrm{dg}}$ MOSFET output capacitance
C_{v}	VCO total capacitance
F	The feedback factor, the amount of output signal fed back to the gate inputs
K_{v}	VCO transfer function in $\frac{Hz}{V}$
R_r	Antenna Radiation Resistance
R_{on}	The MOSFET on resistance
T_o	$V_{\mathrm{out}} = V_{x_{ab}} T_o$ The amplifier loop transfer function
V_{dsat}	This is the V_{ds} voltage where the MOSFET transitions from linear to saturation
V_{ds}	MOSFET drain to source voltage
V_{gs}	MOSFET gate to source voltage
V_{pp}	Voltage Peak to Peak
V_{rms}	$V_{\mathrm{rms}} = \frac{1}{\sqrt{2}}\left(\frac{V_{\mathrm{pp}}}{2}\right)$ This is the RMS signal voltage
V_{v}	VCO control voltage
V_{os}	The OTA input referred offset voltage
$\boldsymbol{nf}$	OTA noise amplification factor
ADC	Analog to Digital Converter
ADC	Analog to Digital Converter
atm	Atmospheric pressure at sea level
CAD	Computer Aided Design

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CDC	Capacitance to Digital Converter
CDC	Capacitance to Digital Converter
CDS	Correlated Double Sampling
CML	Common Mode Logic
CMP	Chemical Mechanical Polishing
CRC	Cyclic redundancy check
D	Duty Cycle of Switched Circuits
dbuf	The RX data receive buffer
DFF	D Flip-Flop
DNL	Differential Non-Linearity
DR	$DR = 10^{\frac{6.02*N+1.76}{10}}$ For an N bit ADC, this is the maximum signal energy versus the minimum step size energy
EM	Electromagnetic
ENOB	$ENOB = \frac{SNR_{dB}-1.76}{6.02}$ The effective number of bits
ENOB	Effective number of bits
ESR	Electrostatic Resistance
FOM	Figure of Merit
FS	Full Scale is the maximum or minimum representative range of the ADC
GBW	The gain bandwidth product
INL	Integral Non-Linearity
KCL	Kirchoff's Current Law, the sum of all currents into a node is equal to zero
KVL	Kirchoff's Voltage Law the sum of all voltages around a loop is equal to zero
LSB	Least Significant Bit
Mbps	Megabits per second
MOMcap	Metal Oxide Metal capacitor
MOSFET	Metal Oxide Silicon Field Effect Transistor
N	Number of inductor wire loop turns
NEB	Noise Equivalent Bandwidth, for 1st order decay, NEB = BW/4 in rad/sec
OTA	Operational Transconductance Amplifier
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
Pa	Pascal - Unit of pressure measurement, 1 atm = 101.325kPa
PDK	Process Design Kit
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PLL	Phase Locked Loop
PSD	Power Spectral Density
PSK	Phase Shift Keying
PSpice	Simulation Program with Integrated Circuit Emphasis
Q	Quality factor, the ratio of reactive energy to resistive energy
RX	data reception
S/H	Sample and Hold capacitor
SAR	Successive Approximation Register ADC
SC	Switched Capacitor
SEPIC	Single Ended Primary Inductor Converter
SNR	$SNR = \frac{S^2_{\text{ignal}_{rms}}}{V^2_{\text{noise}}}$ Signal to noise ratio
SNR$_{\text{dB}}$	$SNR_{\text{dB}} = 10\ \text{Log}_{10}(\text{SNR})$
sps	samples per second
SSB	Single Sideband
TX	data transmission
Variance	σ is the rms squared value of the AC part of a signal (signal - average)$^2_{\text{rms}}$
VNA	Vector Network Analyzer
WPT	Wireless Power Transmission
ZVS	Zero Voltage Switching

1

Introduction

Patients suffering from various types of cardiovascular disease will often undergo endovascular stent implantation. Afterwards, patients are generally required to have periodic checkups for the rest of their lives to verify that the stent implant is still functioning as expected. Today, these checkups require the patient to make a trip to the hospital to undergo computer imaging, sonography, MRI, or X-Ray computed tomography. These scans are then reviewed by a physician to verify the functionality of the stent implant.

1.1 Project Motivation

The goal of this research work was to develop a system that not only improves the accuracy of the stent implant verification process by collecting direct real time pressure measurements at the location of the stent implant, but to allow these checkups to be performed from the comfort of the patient's home. With this new system, the patient would be able to take pressure measurements from the stent implant at any time of their choosing, and they could then send the data files to their physician for clinical evaluation.

The methods for determining stent implant efficacy are dependent on the purpose for which the stent was implanted. One major use for stent implants is the treatment of aortic aneurysms. The treatment of aneurysms requires the stent to fully prevent blood from leaking into the aneurysm sac. For this purpose, an array of sensors placed around the outside of the stent could be used to detect localized pressure gradients indicating blood leakage around the stent. Another common use for endovascular stents is to help

dilate arteries to improve blood flow. To determine if the artery is still being held open and allowing adequate blood flow, an array of sensors with good time and pressure resolution will be used to measure the blood flow through the stent to give warning if the artery once more starts to become blocked.

The device requirements set forth by the expected operating conditions are that the system needs to be able to measure absolute pressure from an array of sensors with a pressure resolution better than 1mmHg, and the system needs to sample fast enough to capture the leading edge of a wave travelling at roughly 1m/sec using sensors which are spaced only 1cm apart from each other. Also, because the device is intended for permanent implantation without the option of battery replacement, the whole system must consume a minimum of power to meet the energy supply constraints associated with wireless power transmission.

1.2 Preliminary Project Work

During the first half of this doctoral work, a proof of concept demonstrator was built and tested by way of in vivo animal testing at the University Clinic Hamburg-Eppendorf. The proof of concept demonstrator was constructed using commercially available electronics. The main controller was a 16 bit microcontroller with 4 ADC channels, and the sensors were micromachined piezoresistive pressure sensors. In December 2011, a successful round of animal testing was concluded giving proof of concept that the wireless power transmission and wireless data transmission design was valid.

Even though the demonstrator was able to show proof of concept, there were many qualities of the demonstrator which needed improvement. First and foremost was the active power consumption. When the demonstrator was active, and the piezoresistive pressure sensors were energized for pressure measurement, the system had an active power consumption of about 15mW, which is a tremendous amount of energy for only four pressure sensors. In addition to the power consumption, the resolution of the pressure sensors was only about 12 mmHg per least significant bit.

The design, construction, and testing of the proof of concept demonstrator will not be covered in this paper. Instead, this paper will cover the design of a new pressure measuring device capable of much greater pressure and time resolution at much lower energy requirements.

1.3 Proposed Monitoring System

This paper will present a system which is being designed to meet these requirements. The system uses an external RF energy sender which serves as the energy source for the pressure sensing implant. The pressure sensing implant has an array of capacitive pressure sensors which are measured with an application specific integrated circuit (ASIC). The ASIC has integrated wireless energy harvesting electronics, 4 capacitance to digital converter channels, and a wireless bi-directional communications interface. The system can simultaneously measure 4 different pressure sensors at 4ksps with a pressure resolution of 0.75mmHg, and transmit those pressure samples to an external monitoring device for display and data logging.

2

System Overview

In February of 2012, design work began on a completely integrated system on chip which could combine all of the discrete elements of the demonstrator system into one silicon package. In November of 2012, the first design was completed and sent for fabrication, and in October of 2013, a second version of the chip was submitted for manufacture. It is the design of this fully integrated system on chip which will be presented in the paper.

The pressure monitoring system is a complete mixed signal system on chip with RF energy collection, capacitance to digital conversion, bidirectional data communication, and a digital control logic block, Figs. 2.1. The implant has been designed to be permanently implanted inside the affected artery as an integrated part of the endovascular stent implant, and to receive its energy and transmit its pressure samples wirelessly to an external reader device.

2.1 The RF Receive Block

The RF receive block of the implant is made up of the energy harvester and clock recovery blocks, voltage regulation and power distribution, and receive data demodulation blocks. The energy harvester rectifies the RF energy and extracts the system clock. The voltage regulation and power distribution blocks generate the 1.2 VDC and the analog system bias reference currents. The receive data demodulation blocks extract the analog data envelope from the AM modulated RF energy carrier.

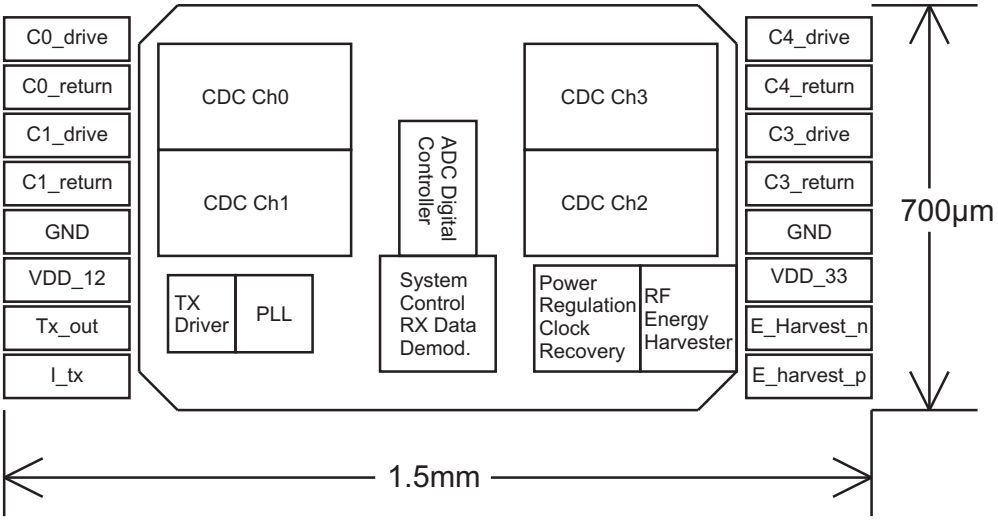


Figure 2.1: The block diagram of the TIPS pressure measurement IC.

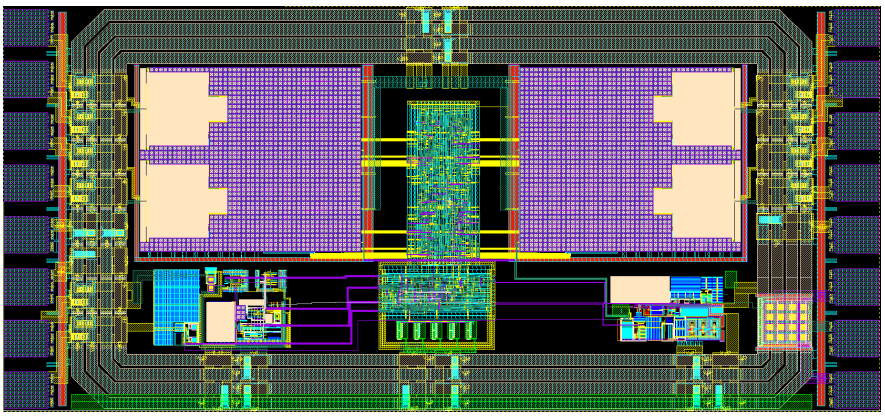


Figure 2.2: The layout of the TIP pressure measurement IC in 130nm UMC technology.

2.2 Capacitance to Digital Converter

The implant has 4 integrated capacitance to digital conversion (CDC) channels. Each channel uses a capacitive bridge architecture to generate the signal, and an operational transconductance amplifier (OTA) to amplify the small signal from the capacitive bridge to the full scale signal for the digital conversion. The digital conversion is accomplished using a fully differential analog to digital converter (ADC) .

2.3 Data Transmission

Using the extracted clock as a reference, a phased locked loop (PLL) is used to generate a high frequency RF data carrier which is an integer multiple of the RF energy carrier. The PLL is a highly configurable self biasing design which can be operated over a wide range of oscillation frequencies. This gives it the ability to transmit its data using any of the various RF spectrum energies which are available for medical devices [1, 2].

2.4 Wireless Power Transmission

To enable permanent implantation without the capability of changing batteries at a later date, the implant uses RF energy harvesting as its energy source. The RF power sender is a class E tuned amplifier, and it serves both as the implant's energy source and clock source. The power sender and the implant are coupled together through resonant magnetic coupling.

The various chapters in this dissertation will be dedicated to giving an in depth description of the method and performance of each of these system design blocks.

3

The Pressure to Voltage Converter

The ASIC design developed during this research work is, first and foremost, a pressure sensing IC. There are 4 pressure sensing channels working in parallel to simultaneously measure blood pressure at a combined rate of 16,000 samples per second (sps). The implant's IC design has been built in a 130nm CMOS technology process, and it has been custom designed to measure a commercially available capacitive pressure sensor, the E1.3N from Protron Mikrotechnik [3]. Starting with the pressure sensitive capacitor, the pressure sensing channel in Fig. 3.1 measures the signal voltage from the capacitive bridge, amplifies the signal using a gain boosted operational transconductance amplifier (OTA), and converts the analog signal to a digital value with the 10 bit analog to digital converter.

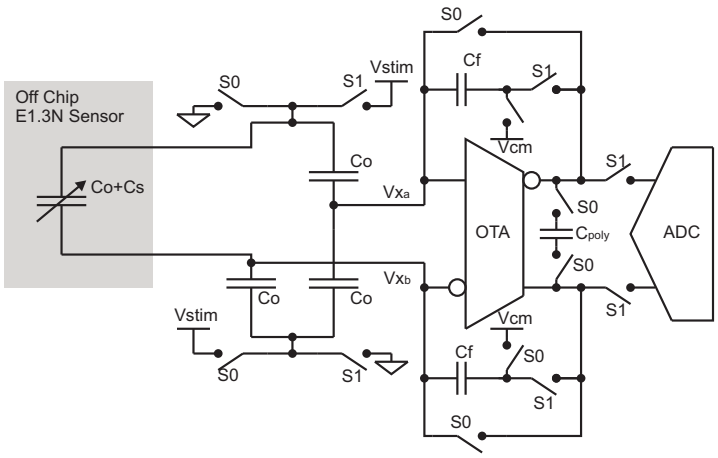


Figure 3.1: The pressure sensing capacitance to digital conversion channel.

To accurately measure the sensor's capacitance, a complete signal conditioning chain for converting the sensor capacitance to an analog signal for the analog to digital converter (ADC) has been developed. The signal conditioning electronics have been designed with a special emphasis on meeting the ADC signal to noise (SNR) requirements while consuming the minimum amount of power possible.

3.1 Capacitance to Analog Conversion

This chapter will describe a circuit architecture which measures the capacitor using correlated double sample techniques (CDS) [4, 5]. The correlated double sampling signal conditioning chain is used to generate a signal voltage from the pressure sensitive capacitor, and apply gain to that signal for analog to digital conversion. There are as many different switched capacitor (SC) gain stage structures as there are different ways to use them, but they all essentially behave the same way. Operating with two non-overlapping clock phases, S0 and S1, the OTA resets itself during phase S0, and it samples the input voltage during phase S1. Figure 3.1 shows the basic structure of the capacitance to digital converter chain which was used for this design.

3.1.1 Correlated Double Sampling with Input and Output Offset Correction

The signal amplifier is a fully differential SC amplifier with input and output offset compensation (Fig. 3.1) [6]. The SC amplifier takes two input signal samples to generate one output voltage. During SC switch phase S0, the amplifier resets itself by placing itself in a unity gain configuration. While in unity gain, any input referred offset voltage $V_{\rm os}$ shows up across the OTA's output and is inverted and fed directly back to the input because of the unity gain feedback. This action is called input offset cancellation.

During the S0 reset phase, a voltage equal but opposite to the OTA's input referred offset gets sampled across $V_{\rm ab}$, and when the system switches to phase S1 the OTA behaves as if it were a perfect OTA with no input offset voltage. However, there is now an offset voltage which would be present at the OTA output if it is not taken care of. To cancel out the output offset voltage, during S0 when the input offset is being canceled, the right side plates of the feedback capacitors C_f (Figure 3.1) are set to the common mode voltage V_{cm}. This means that the offset voltage which gets stored across

the output also gets stored across the feedback capacitors. Because the output offset has been stored across the feedback capacitors, when the right side plates are switched from ground to the output node, then the output nodes, which were previously at V_{os}, must swing to V_{cm} for V_{os} to be maintained across $V_{x_{ab}}$.

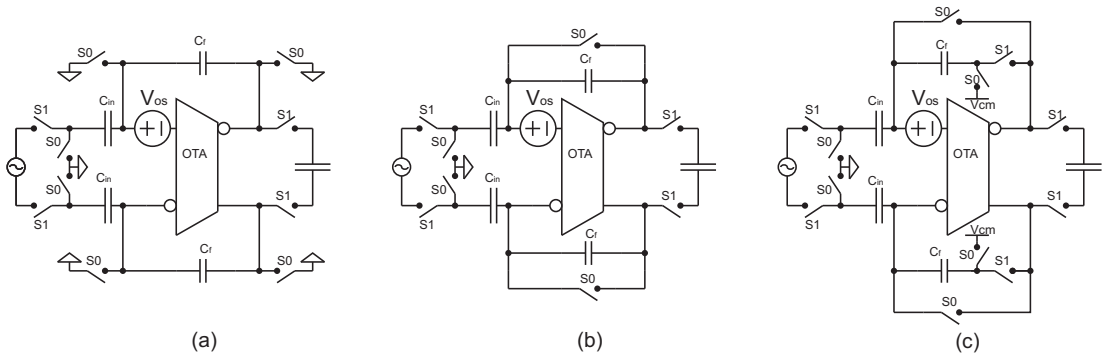
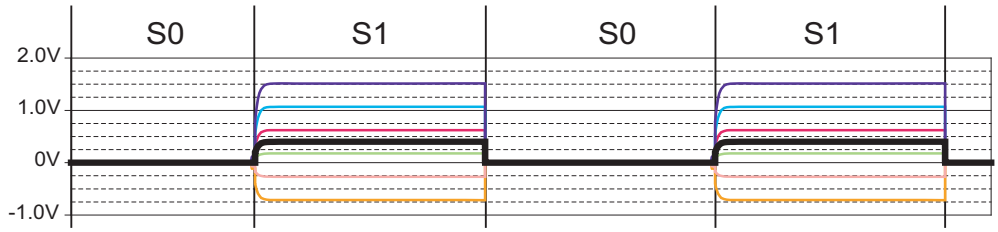


Figure 3.2: Three different switched capacitor gain stage offset cancellation topologies
a) A CDS structure with no offset cancellation.
b) A CDS structure with only input offset cancellation.
c) A CDS structure with input and output offset cancellation.

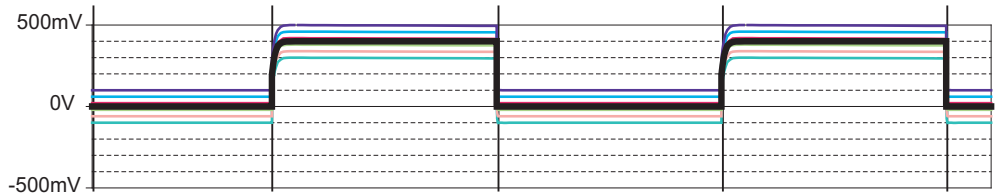
Fig. 3.3 shows three simulation runs, one simulation for each of the three circuits from Fig. 3.2. Each of the three simulations has an input signal voltage of $V_{\text{in}} = 40\text{mV}$ with a closed loop gain A_{cl} =10 V/V, and the simulated input offset voltage is stepped from -100mv to +100mV in 40mV increments. Fig. 3.3a shows how the output voltage is the input signal plus the static DC offset multiplied by the closed loop gain. Fig. 3.3b shows how the output voltage has a constant offset equal to the input referred offset voltage. Fig. 3.3c shows that during the reset phase S0 there is an offset voltage at the output (this is the offset which is zeroing out the input offset), but during the sample phase S1 the output offset voltage is zeroed out, and the final output voltage is $V_{\text{out}} = V_{\text{in}} A_{\text{cl}} = 400\text{mV}$

3.1.2 Switched Capacitor Charge Injection

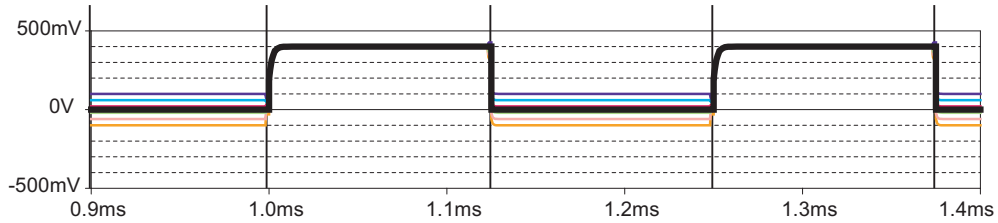
The CDC gain stage is a switched capacitor gain stage, and each of these switches are MOSFET switches. A MOSFET is great as an off switch with an off resistance on the order of several tens of gigaohms, but the transition from on to off has a deleterious side effect called charge injection.



(a) No Offset Cancellation



(b) Input Offset Cancellation



(c) Input and Output Offset Cancellation

Figure 3.3: Waveforms from simulations of the circuits given in Fig. 3.2. The desired output voltage is the bold trace $V_{\text{out}_0} = V_{\text{in}} A_{\text{cl}}$, and it is plotted against three different switched capacitor structures where the input offset voltage is stepped from -100mV to +100mV.
a) With no input or output offset cancellation: $V_{\text{out}} = A_{\text{cl}}(V_{\text{in}} + V_{\text{os}})$
b) With only input offset cancellation: $V_{\text{out}} = A_{\text{cl}} V_{\text{in}} + V_{\text{os}}$
c) With input and output offset cancellation: $V_{\text{out}} = A_{\text{cl}} V_{\text{in}}$

Figs. 3.4a and 3.4b shows the MOSFET as it switches from on to off. Charge injection into the low impedance voltage source causes no change in its voltage, but the effect of charge being injected onto the capacitor causes a voltage jump across C equal to (3.1).

$$dV = \frac{dQ}{C} \tag{3.1}$$

Charge injection is caused by the physical process of turning a MOSFET off, and as long as MOSFETs are used as the switches, there will be some charge injection. This project work did not attempt to develop a new way of building the switches. Instead,

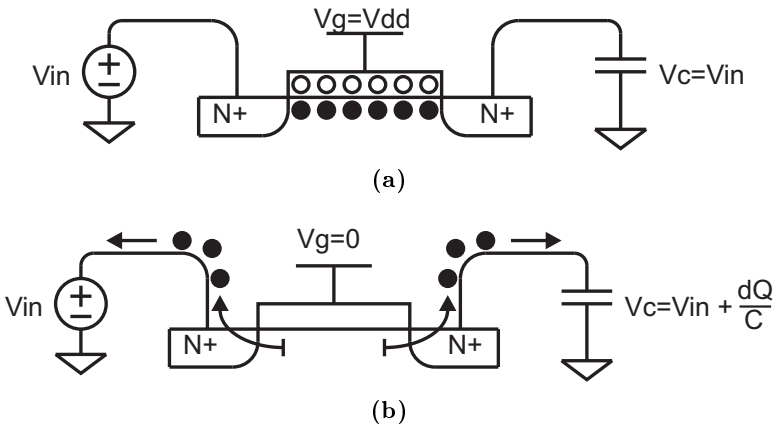


Figure 3.4: MOSFET charge injection

this project work exploits the differential nature of the gain stage to minimize the effects of the charge injection.

The nodes which experience charge injection are nodes $V_{x_{a,b}}$ and the right hand side plates of the feedback capacitor. During reset phase S0, the OTA inputs V_{x_a} and V_{x_b}, the right hand side feedback capacitor plates (Fig. 3.1), and the OTA output nodes are all reset to Vcm (this is accurate if $V_{\text{cm}} + V_{os} \approx V_{\text{cm}}$). Because all of these nodes are at a known potential as the device switches from S0 to S1, then it is assumed that the amount of charge injected onto V_{x_a} and V_{x_b} are equal to each other and remain the same from sample to sample. This type of deterministic behavior lends itself well to the use of a fully differential architecture. If the amount of charge injected onto the two differential nodes is equal, then the differential voltage change will be negligible. Also, if the amount of charge injected onto the differential nodes is not equal, but is always the same from sample to sample, then this manifests itself into a constant offset voltage which can be calibrated out. The two switches on the C_f right hand side plate, S0 and S1, have been sized with equal width and length, so that the charge carriers which are injected onto the feedback capacitor plate by the S0 switch channel destruction, are then removed from the plate by the S1 switch channel creation.

Because each and every one of the nodes starts at a pre-determined S0 reset voltage, the most effective method for ensuring that the charge injection from the switches is common mode is to ensure that the complimentary switches on the top and bottom of the circuit are as closely matched to each other as possible when layed out on the IC.

Fig. 3.5 shows the layout used for the two feedback capacitors, C_f in Fig. 3.1, and their S0 and S1 switches.

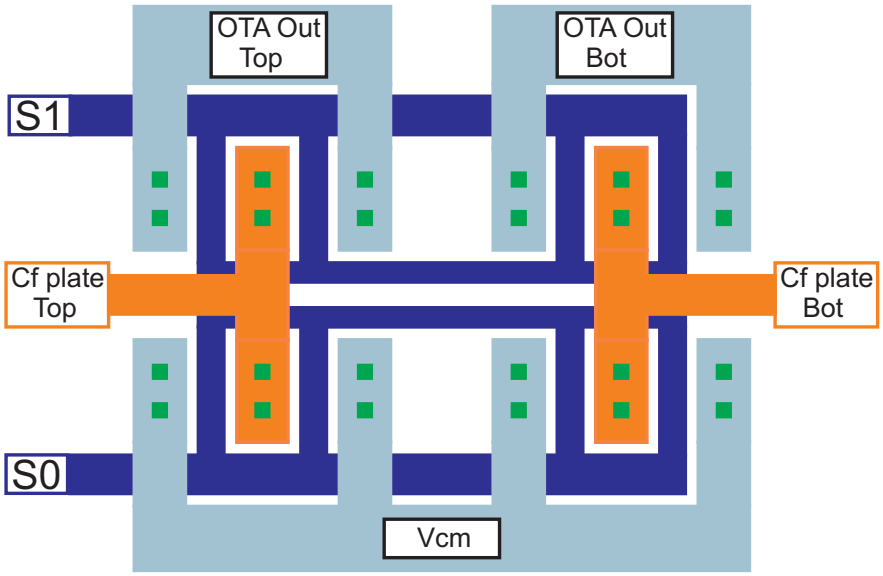


Figure 3.5: The layout design for minimizing mismatch between the complimentary switches of the SC amplifier.

Each of the switches are dual gate MOSFETS which helps to reduce the parasitic drain capacitance and to ensure that the current flows in both directions through each devices. The switches are layed out so that their spatial orientations are as closely matched as possible to try to accomplish as effective charge injection cancellation and matching as possible. The switches and capacitors are close to each other, and the capacitor and switch groupings are mirror images of each other.

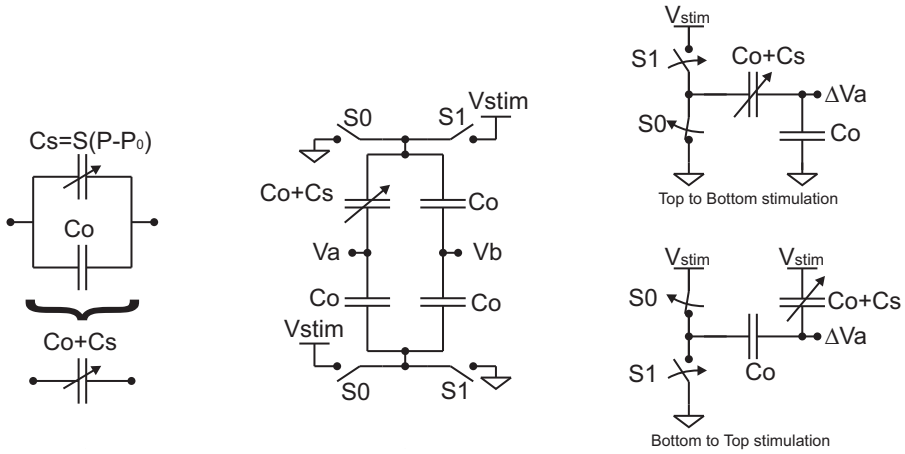
The system has a relatively slow sample rate, which makes it fairly easy to size the switch transistors so that their on resistance R_{on} is small enough to not slow down the system response. The maximum output swing of the OTA is $V_{\mathrm{dd}}/2V_{\mathrm{dsat}}$, which is a little bit less than the NMOS threshold voltage. This has the effect of decreasing the NMOS R_{on} as the output nodes potential starts to put the MOSFET device into the linear region. But, because the required bandwidth of the system is relatively low, the result of increasing R_{on} does not have a significant impact on the switches response time. However, the switches which drive the capacitive bridge input signal generator are transmission gates to ensure good rail to rail voltage stimulation.

3.1.3 Calculating C_f

The first step in designing the signal conditioning electronics is to derive a formula which gives the measurement device's signal voltage generation as a function of its pressure sensitivity and the stimulation voltage. Fig. 3.6a gives a simplified model of the capacitive pressure sensor (the parasitic resistances have been omitted), showing that the sensor can be modeled as a nominal capacitance and a pressure sensitive capacitor in parallel resulting in a total sensor capacitance of

$$C_{\text{sensor}} = C_0 + S(P - P_0),$$

where C_0 is the nominal capacitance at the nominal pressure P_0, S is the sensitivity of the sensor given in Farads/atmosphere, and P is the absolute pressure being applied to the sensor.



(a) **(b)** **(c)**

Figure 3.6: The circuit diagrams used for calculating the signal voltage as a function of the stimulation voltage and sense capacitance.
a) The pressure sensitive capacitor equivalent circuit.
b) The capacitive bridge circuit for generating the signal voltage.
c) The circuits used for calculating the net change at node V_a using superposition.

To calculate the the signal voltage response to the device's pressure sensitive capacitance, each branch of the capacitive bridge is being stimulated by 2 voltages, a positive going V_{stim} and a negative going V_{stim}. To find the total voltage change at each branch node, superposition can be applied to the bridge circuit, Fig. 3.6b. Using the equivalent

circuits in Fig. 3.6c and calculating the positive (3.2) and negative (3.3) going voltages, and then the summing the voltages (3.4) gives the V_a node transfer function.

$$\uparrow Va_{\mathrm{S0}\to\mathrm{S1}} = V_{\mathrm{stim}}\frac{C_0 + C_s}{2C_0 + C_s} \tag{3.2}$$

$$\downarrow Va_{\mathrm{S0}\to\mathrm{S1}} = V_{\mathrm{stim}}\frac{C_0}{2C_0 + C_s} \tag{3.3}$$

$$\Delta Va_{\mathrm{S0}\to\mathrm{S1}} = V_{\mathrm{stim}}\frac{C_0 + C_s - C_0}{2C_0 + C_s} \tag{3.4}$$

$$\Delta Va_{\mathrm{S0}\to\mathrm{S1}} = V_{\mathrm{stim}}\frac{C_s}{2C_0 + C_s} \tag{3.5}$$

The transfer function for V_b is can be derived in exactly the same way, but because $C_0 - C_0 = 0$, then

$$\Delta Vb_{\mathrm{S0}\to\mathrm{S1}} = 0,$$

resulting in a function which describes the input signal voltage as a product of the stimulation voltage and the sense capacitance of the pressure sensitive capacitor (3.6), and a capacitance to signal voltage transfer function $H_{(C_s)}$ of (3.7).

$$\begin{aligned} V_{\mathrm{signal}} &= \Delta Va_{\mathrm{S0}\to\mathrm{S1}} - \Delta Vb_{\mathrm{S0}\to\mathrm{S1}} \\ V_{\mathrm{signal}} &= \Delta Va - \Delta Vb \\ V_{\mathrm{signal}} &= V_{\mathrm{stim}}\left(\frac{C_s}{2C_0 + C_s}\right) \end{aligned} \tag{3.6}$$

$$H(C_s) = \frac{C_s}{2C_0 + C_s} \tag{3.7}$$

In order for the CDC to be able to make full use of the ADC's dynamic range (DR), the signal which is generated by stimulating the capacitive bridge needs to be given an appropriate amount of closed loop gain, A_{cl}, so that when a full scale pressure is applied to the sensor, there will be a corresponding full scale output voltage.

It should be pointed out that the system is a fully differential system, meaning that the full scale fully differential output voltage is

$$V_{\mathrm{out_{FS}}} = \pm V_{\mathrm{dd}} = 2V_{\mathrm{dd}}.$$

If the pressure sensing capacitive bridge is stimulated with the stimulation voltage V_{stim}, then, across the full scale peak-peak range of the pressure sensing capacitance $C_{s_{\text{pp}}}$, the full scale input voltage is

$$V_{\text{in}_{\text{FS}}} = V_{\text{stim}} H(C_{s_{\text{pp}}}) = V_{\text{stim}} \left(H(C_{s_{\text{max}}}) - H(C_{s_{\text{min}}}) \right), \tag{3.8}$$

For this design, the stimulation voltage for the capacitive bridge is the supply voltage, $V_{\text{stim}} = V_{\text{dd}}$, and the system closed loop gain is therefore (3.10).

$$A_{\text{cl}} = \frac{V_{\text{out}_{\text{FS}}}}{V_{\text{in}_{\text{FS}}}}$$

$$2V_{\text{dd}} = A_{\text{cl}} V_{\text{dd}} H(C_{s_{\text{pp}}}) \tag{3.9}$$

$$A_{\text{cl}} = \frac{2}{H(C_{s_{\text{pp}}})} \tag{3.10}$$

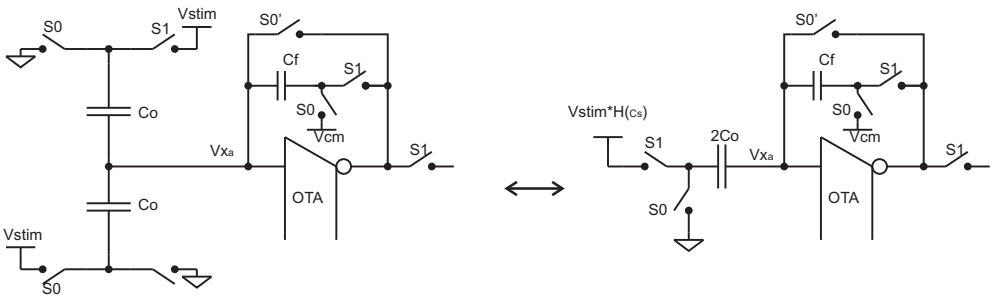


Figure 3.7: The CDS half circuit for finding the closed loop gain.

The closed loop gain of an inverting amplifier is the feedback impedance divided by the input impedance Z_f/Z_{in}. The top half circuit of the amplifier from Fig. 3.1 is shown again in Fig. 3.7, with the capacitor bridge transformed to show how the input impedance of the CDS system is simply the two branch capacitors in parallel. The feedback impedance from C_f is $1/sC_f$, and the input impedance is $1/s(2C_0)$, resulting in (3.11).

$$A_{\text{cl}} = \frac{2C_0}{C_f} \tag{3.11}$$

Combining (3.10) and (3.11) will solve for the value of C_f as a function of the sensor's nominal capacitance and maximum capacitance $H_{(C_{s_{\text{pp}}})}$(3.12).

$$C_f = C_0 H_{(C_{s_{\text{pp}}})} \tag{3.12}$$

In the case where $C_0 \gg C_s$, which is the case for the E1.3N capacitive pressure sensor, then (3.7) can reduce to

$$H_{(C_s)} \approx \frac{C_s}{2C_0}, \tag{3.13}$$

and the feedback capacitance C_f would be

$$\begin{aligned} H_{(C_s=C_{s_{\text{pp}}})} &\approx \frac{C_{s_{\text{pp}}}}{2C_0} \\ C_f &\approx \frac{C_{s_{\text{pp}}}}{2} \end{aligned} \tag{3.14}$$

3.1.4 The Final CDS Network Design

At this stage of the design process, because the system supply voltage of V_{dd} was chosen for the stimulation voltage, the value for C_f can be calculated based entirely on the desired pressure read range and physical constants intrinsic to the capacitive pressure sensor. The E1.3N pressure sensor has sensitivity $S \approx 1.6\text{pF/atmosphere}$, and a nominal capacitance of $C_0 \approx 6.0\text{pF}$. For this project, the desired dynamic pressure read range is 1 atm, so $C_{s_{\text{pp}}} = 1.6\text{pF}$, and C_f is 804 fF from (3.12) (and $C_f = 800fF$ when using (3.14)).

At this point, the structure for the pressure sensor's gain stage has been finalized (Fig. 3.1), and the required closed loop gain, and therefore also the value for C_f, has been calculated based on the desired pressure read range and the amplifier output voltage swing. The next two design requirements concern designing an OTA that can meet the desired sample rate and pressure resolution.

4

The Capacitance to Digital Converter Noise Analysis

The capacitance to digital conversion process isn't simply the act of taking the pressure to voltage conversion, amplifying it, and then resolving it to an arbitrary ADC resolution. There will always be some system noise from the amplification stage which will be summed with the pressure sensor sample, and the amount of system noise will determine the maximum usable ADC resolution. Higher resolution ADCs require lower amounts of system noise, and in general, keeping the system noise low requires more power. The ADC and the ADC driver are designed to work with each other. There is no real benefit for over designing the amplification stage if the ADC resolution is low. For example, if the ADC is a 1 bit ADC, then as long as the noise from the amplifier is less than Vdd/2, then the ADC will have no difficulty deciding if the sensor reading is a 1 or a 0. On the other hand, if the power consumption of the circuit must be kept to a minimum, then there is no need to design a 12 bit ADC when the amplifier has a very small signal to noise ratio. To be able to match the OTA performance to a desired pressure resolution it is necessary to define exactly how much noise the CDC system will inject into the noise sample.

Section 4.1 will describe some of the fundamental behaviors of the MOSFET device such as the derivation of the circuit voltage gain and the bandwidth as a function of the device transconductance and load impedance. Section 4.2 will perform a rigorous noise analysis of the switched capacitor capacitance to analog voltage conditioning circuit. The noise analysis will result in a single design equation which describes the total system

noise as an inverse function of the OTA noise factor, nf, and the ADC sample and hold input capacitance. This section will also derive the required OTA bandwidth and open loop gain, A_0, based on the sample rate and ADC resolution accuracy requirements. Section 4.3.1 will cover the derivation of a single general design equation which will return the OTA's maximum allowed noise amplification factor (nf). The nf will be given as a function of the transconductance efficiency ratios, η_{gm}, of each of the OTA's MOSFET devices, and their associated thermal noise coefficient, γ, when operating at that particular level of gm efficiency. And finally, Section 4.4 will discuss the method used to size all of the various transistors to meet the noise factor and the settle time requirements.

4.1 General Transconductance Device Behavior

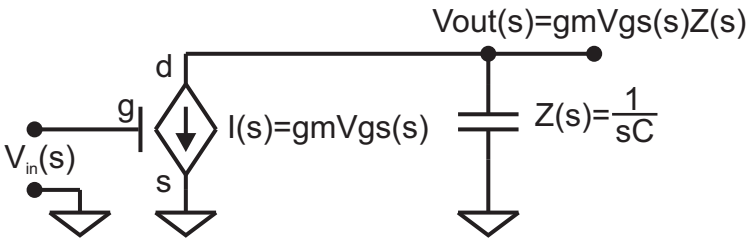


Figure 4.1: The MOSFET small signal model.

The small signal model of a MOSFET driving a capacitance is given in Fig. 4.1. It has an output impedance $Z = 1/sC$, and an output current to input voltage ratio of gm. Because the current and voltage are inversely related to each other by the factor gm, gm is sometimes modeled as an inverse resistance, $gm = 1/R_{eff}$. The output voltage is the output current times the output load which gives the input to output voltage transfer function (4.1).

$$\begin{aligned} V_{\text{out}}(s) &= I(s)Z(s) \\ V_{\text{out}}(s) &= gmV_{\text{in}}(s)Z(s) \\ H(s) &= \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = gmZ(s) \end{aligned} \tag{4.1}$$

Substituting $Z(s) = 1/sC$ into (4.1), results in the frequency dependent transfer function (4.2), and the frequency where the voltage gain drops to 1 V/V, also known

as the gain bandwidth product (GBW), occurs at $\omega = gm/C$, (4.3).

$$H(s) = \frac{gm}{sC} \tag{4.2}$$

$$\omega_{\text{GBW}} = \frac{gm}{C} \tag{4.3}$$

A perfect current source driving a perfect capacitor as in in Fig. 4.1 would have infinite DC voltage gain, but in real life there are no perfect MOSFETs or capacitors. In reality there will be leakage current through the MOSFET (and also a little through the capacitor) as voltage is applied to the drain of the MOSFET, and the current through the MOSFET will will no longer be exactly $Id = gmV_{\text{gs}}$. The ratio of the change in drain current to change in drain voltage is called the device output conductance gd, and its reciprocal is the output resistance $1/gd = r_0$. Fig. 4.2 shows the complete small signal model for the MOSFET driving a load capacitance C.

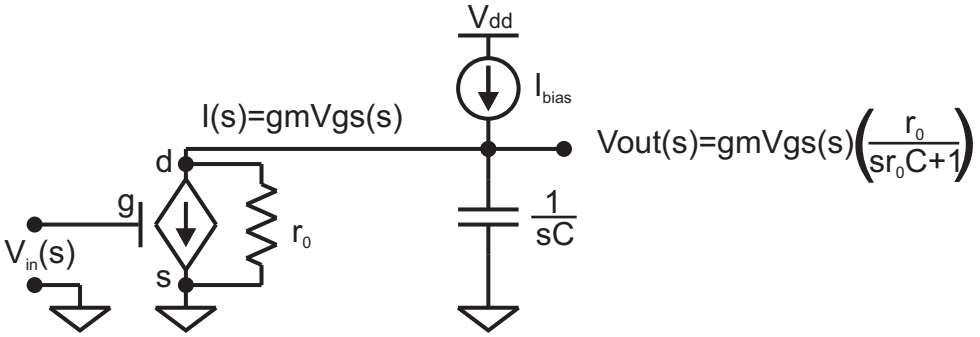


Figure 4.2: An equivalent circuit of a transconductance device with the included device transresistance and reference bias generator.

The output impedance of the circuit from Fig. 4.2 is (4.4), and the small signal transfer function is (4.5). The DC gain of the amplifier is (4.6), and the 3 dB cutoff bandwidth occurs when the denominator magnitude is $1/\sqrt{2}$ (4.7).

$$Z(s) = \frac{r_0}{sr_0C + 1} \tag{4.4}$$

$$H(s) = gm\left(\frac{r_0}{sr_0C + 1}\right) \tag{4.5}$$

$$A_0 = gmr_0 \tag{4.6}$$

$$\omega_{3_{dB}} = \frac{1}{r_0C} \tag{4.7}$$

The amount of thermal energy delivered from a purely resistive device (such as a resistor) is given as kT,

$$E = kT$$

where k=1.38e-13 is Boltzmann's constant, and T is the temperature in Kelvin. Energy is power times time, and the energy dissipated in a resistor is

$$E = I_{\text{rms}}^2 R = \frac{1}{2} I^2 R \; sec$$

where $I_{\text{rms}} = I/sqrt2$.

From the maximum power transfer theorem, the maximum energy that the resistor can supply to a load is 1/2 of the total energy available from the resistor

$$E_{Resistor} = \frac{1}{4} I^2 R \; sec.$$

Equating the kT thermal energy to the amount of energy delivered from the resistor results in a function for the thermal noise current of a resistor.

$$kT = \frac{1}{4} I^2 R \; sec$$
$$I^2 = 4kT \frac{1}{R} \Delta f$$

Transconductance is $gm = 1/R_{eff}$, but the thermal noise current of the MOSFET does not exactly match the thermal noise current of an equivalent resistor.

$$I_{noise_textMOSFET}^2 \neq 4kT/R_{eff}$$

To account for this, it is common to include a noise scaling coefficient, γ [7], for equating the MOSFET noise current to the kT thermal energy. With this γscaling factor, the MOSFET output noise current is (4.8), and the output current can be input referred to a noise voltage by diving by $1/gm^2$ (4.9).

$$I_{noise_{\text{out}}}^2 = 4kT\gamma gm \tag{4.8}$$
$$V_{noise_{\text{in}}}^2 = 4kT\frac{\gamma}{gm} \tag{4.9}$$

The MOSFET device in Fig. 4.2 is getting its bias current from a perfect current source which does not have any associated noise current, but in reality, there is no such thing as a perfect current source. Instead, the current source itself will be a MOSFET biased at a DC voltage with its own $4kT\gamma gm$ noise current contribution.

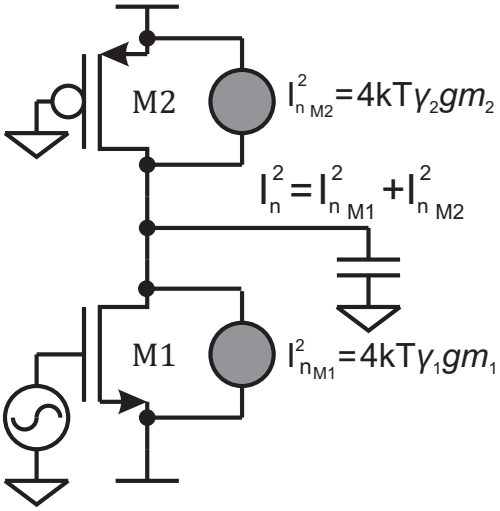


Figure 4.3: Input referred system noise current

How much extra noise current is being supplied by the load is very dependent on the load circuit. Later in this chapter, Sec. 4.3.1, a full derivation of the total amount of extra noise current is given. However, for the time being, the total input referred noise of the amplifier is given as the input device input referred thermal noise voltage, (4.9), multiplied by a thermal noise factor nf (4.10).

$$V^2_{noise_{\text{in}}} = 4kT\frac{\gamma}{gm}nf, \tag{4.10}$$

where nf is simply a scaling factor which is used to input refer the total output noise current to the input device's gm.

4.2 SC Noise Analysis

The SC amplifier is a fully differential SC amplifier with input and output offset cancellation circuitry (Fig. 4.4) [6]. In Fig. 4.5a, during SC switch phase $S0$, the amplifier is in reset configuration where the OTA's DC offset voltage V_{os} and the system noise voltage $V_{x_{ab}S0noise}$ are sampled across the nodes $V_{x_{ab}}$ (4.11). During phase $S1$, Fig. 4.5b, V_{os}, the system noise voltage $V_{x_{ab}S1noise}$, and the capacitance to voltage conversion result

are sampled across $V_{x_{ab}}$ (4.12).

$$V_{x_{ab}S0} = V_{os} + V_{x_{ab}S0noise} \tag{4.11}$$

$$V_{x_{ab}S1} = V_{os} + V_{x_{ab}S1noise} + \Delta V_{ab} \tag{4.12}$$

$$V_{x_{ab}S1} - V_{x_{ab}S0} = \Delta V_{ab} + V_{x_{ab}S0noise} + V_{x_{ab}S1noise} \tag{4.13}$$

Taking the difference between (4.12) and (4.11) results in (4.13). The noises are variance, and they are therefore summed together, but the offset voltage is deterministic, and is therefore subtracted away leaving only the conversion signal and the noise from the two sample stages.

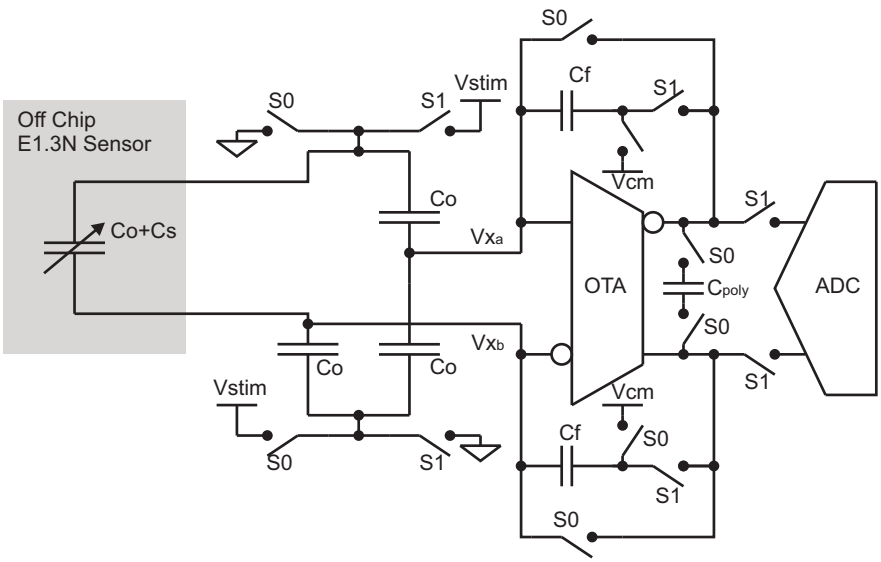


Figure 4.4: Schematic of the capacitive bridge and the SC amplifier with associated parasitic capacitances

4.2.1 SC Noise Analysis for Phase S0

To determine the noise from switching phase $S0$, the SC amplifier circuit from Fig. 4.4 can be reduced to the circuit in Figure 4.6. To find the amount of rms noise voltage sampled across $V_{x_{ab}}$ while the OTA is in reset, the noise voltage across $V_{x_{ab}}$ needs to be integrated over all frequencies. Looking at Fig. 4.6, the signal across $V_{x_{ab}}$ is simply the OTA output voltage, which in the reset phase is just the sum of the two input referred noise voltages (4.10), multiplied by the frequency dependent circuit transfer function

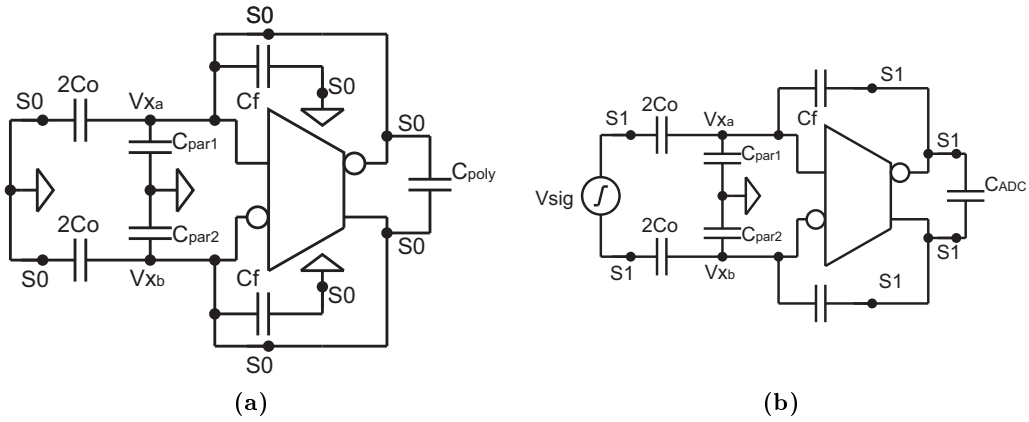


Figure 4.5: Simplified circuit diagram of the SC amplifier in its two switch phases.

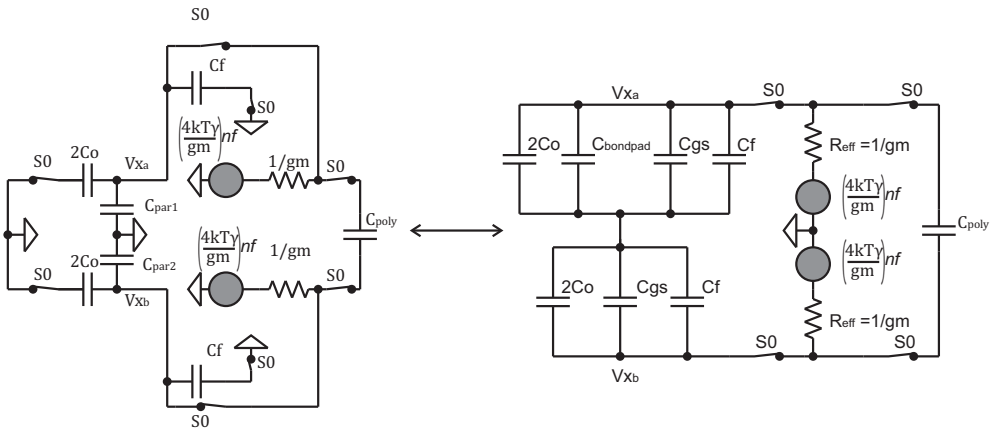


Figure 4.6: Schematic of the SC amplifier during phase S0 with the equivalent circuit for deriving C_{eq}.

across the equivalent capacitance, C_{eq}. The differential load capacitance across the outputs of the OTA during switching phase $S0$ in Fig. 4.6 can be derived as follows C_{eq} (4.14).

$$\begin{aligned} C_{eq_a} &= 2C_0 + C_{par1} + C_f \\ C_{eq_b} &= 2C_0 + C_{par2} + C_f \\ C_{eq} &= \frac{C_{eq_a} C_{eq_b}}{C_{eq_a} + C_{eq_b}} + C_{\text{poly}} \end{aligned} \tag{4.14}$$

Using C_{eq}, the $\omega_{3_{\text{dB}}}$ cutoff frequency in radians is

$$\omega_{3_{\text{dB}}} = \frac{1}{C_{eq}(2R_{eff})},$$

the transfer function from the noise voltage generator to the $V_{x_{ab}}$ nodes is

$$\begin{aligned} H(j\omega) &= \frac{1}{j\frac{\omega}{\omega_{3_{\text{dB}}}}+1} \\ H(j\omega) &= \frac{1}{j\omega C_{eq}(2R_{eff})+1} \\ H(j\omega) &= \frac{1}{j\omega\frac{2C_{eq}}{gm_1}+1}, \end{aligned} \tag{4.15}$$

and the frequency dependent output noise voltage at $V_{x_{ab}}$ is (4.16).

$$V^2_{out_{\text{noise}}} = 8kT\frac{\gamma_1}{gm_1}nf\left(\frac{1}{j\omega\frac{2C_{eq}}{gm_1}+1}\right)^2 \tag{4.16}$$

The last step for finding the total rms noise is to integrate (4.16) for all frequencies from DC to infinity. Once this integration is complete, the total rms noise for the CDC system while it is being held in switch phase S0 is (4.18).

$$V^2_{noise_{\text{rms}}} = 8kT\frac{\gamma_1}{gm_1}nf\int_0^\infty \left|\frac{1}{j\omega\frac{2C_{eq}}{gm_1}+1}\right|^2 d\omega$$

$$V^2_{noise_{\text{rms}}} = 8kT\frac{\gamma_1}{gm_1}nf\left(\frac{1}{4\frac{2C_{eq}}{gm_1}}\right) \tag{4.17}$$

$$V^2_{x_{ab}S0noise} = \frac{kT}{C_{eq}}\gamma_1 nf \tag{4.18}$$

It should be pointed out here that for a first order transfer function decaying at 20dB/decade from $\omega_{3_{\text{dB}}}$, such as (4.15), its integral from zero to infinity is 1/4 of its cutoff frequency in radians (4.19) [8].

$$\begin{aligned} \oint_0^\infty \left|\frac{1}{j\frac{\omega}{\omega_{3_{\text{dB}}}}+1}\right|^2 d\omega &= \frac{\omega_{3_{\text{dB}}}}{4} \\ NEB &= \frac{\omega_{3_{\text{dB}}}}{4} \end{aligned} \tag{4.19}$$

This factor is commonly called the noise equivalent bandwidth, (NEB), and it will be used several more times throughout the design process.

As the SC amplifier switches to phase $S1$, the OTA drives the nodes V_{x_a} and V_{x_b} to virtual ground, and the noise charge which was sampled onto $V_{x_{ab}}$ during SC phase

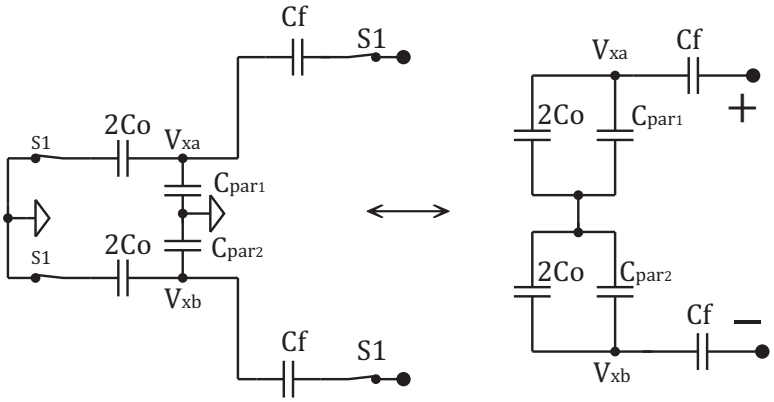


Figure 4.7: Equivalent schematic for deriving the phase S1 feedback factor (4.22)

$S0$ (4.18) gets transferred to the output nodes as a function of the feedback gain. To determine the switch phase S1 voltage gain from $V_{x_{ab}}$ to the output nodes it is only necessary to know the transfer function from output to input. Fig. 4.7 can be used to help determined the feedback factor from output to input. This term is commonly referred to as the feedback factor F, where $F = V_{x_{ab}}/V_{out}$. Taking $V_{x_{ab}}$ and multiplying by $1/F$ gives the output voltage.

$$V_{out} = \frac{V_{x_{ab}}}{F}, \tag{4.20}$$

and by combining (4.18) and (4.20), the final end of conversion output noise contribution from phase $S0$ is (4.21).

$$\begin{aligned} V^2_{out_{noise_{S0}}} &= \frac{V^2_{x_{ab}S0noise}}{F^2} \\ V^2_{out_{noise_{S0}}} &= \frac{kT}{C_{eq}}\frac{\gamma_{in}nf}{F^2} \end{aligned} \tag{4.21}$$

With the help of the equivalent circuit from Fig. 4.7, the calculation of F as the capacitive voltage divider from V_{out} to $V_{x_{ab}}$ is fairly straight forward with the result being (4.22).

$$F = \frac{V_{x_{ab}}}{V_{out}} = \frac{C_f}{C_f + 2\left(\frac{(2C_0+C_{par1})(2C_0+C_{par2})}{(2C_0+C_{par1})+(2C_0+C_{par2})}\right)} \tag{4.22}$$

According to (4.18), the greater the value for C_{eq}, the smaller the S0 $V_{x_{ab}}$ noise voltage. C_0 and C_f are fixed values determined by the sensor's nominal capacitance and the required closed loop gain, but C_{eq} can be made larger by increasing the other capacitances. However, increasing C_{par} will, according to (4.22), reduce the feedback factor which will result in greater phase S0 output noise (4.21).

The solution for reducing the phase S0 noise level while not reducing the amount of phase S1 feedback factor is to use the capacitor C_{poly}. C_{poly} is part of C_{eq} (4.14), but it is not part of F (4.22). Meaning it helps to reduce the phase S0 noise voltage, but the noise charge stored on its plates is not transferred to the output as noise voltage during phase S1. Also, because the OTA is in reset, C_{poly} can be A_{cl} times greater than the ADC sample and hold capacitor without having a negative impact on the reset phase S0 settling bandwidth.

4.2.2 SC Noise Analysis for Phase S1

Even though every switch in Figure 4.4 contributes to the total system noise, some of these switches can be ignored as noise sources if certain requirements are met. Assuming that the switches in the feedback and output path of the circuit have a resistance $R_{sw} \ll \frac{1}{gm\,F}$, which is a safe assumption when the bandwidth of the device is limited by the OTA's gm rather than the SC switch resistance, then it is safe to ignore these output switch noise sources during the noise analysis [9].

Ignoring the feedback and the output switches leaves two major noise sources for the SC switch phase $S1$ configuration. These two noise sources are the input switch noise and the OTA input referred noise voltage. Using the circuit from Figure 4.8, these two output noise voltages will be analyzed and summed together to derive the total switch phase $S1$ output noise.

First, considering the switch input noise, the S1 switch noise generators each have a noise voltage $4kTR_{S1}$ which results from their finite channel resistance. This gives a differential noise voltage which is the sum of the noise from the two switches (4.23), and a total output noise voltage which is the switch noise multiplied by A_{cl} and the NEB (4.24).

$$V^2_{noise_{input}} = 2(4kTR_{S1}) \tag{4.23}$$

$$V^2_{out_{noise_{RS1}}} = (8kTR_{S1})\ A^2_{cl}\ NEB \tag{4.24}$$

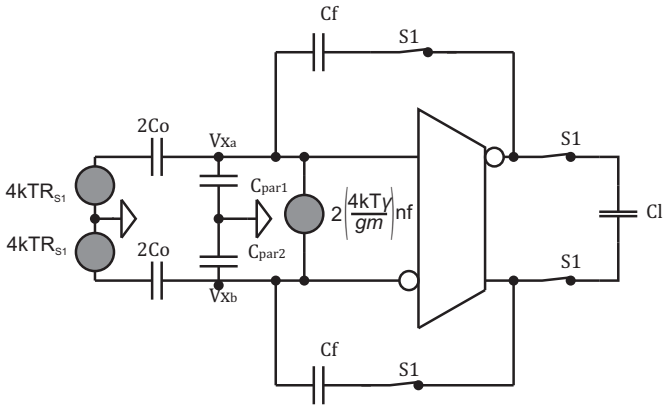


Figure 4.8: Schematic of the SC amplifier during phase S1.

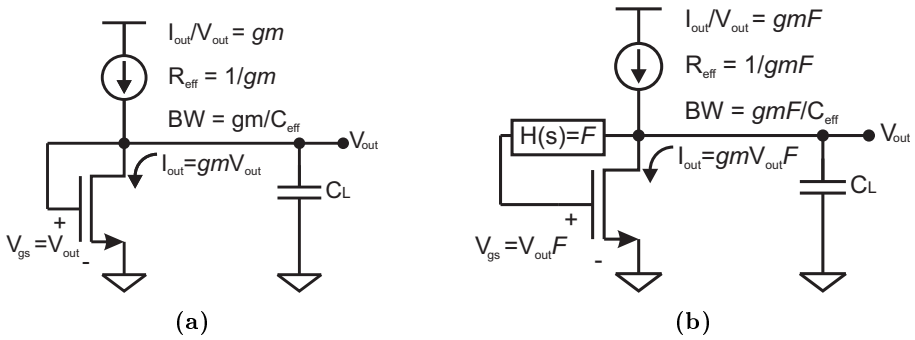


Figure 4.9: A transconductor operating with a feedback transfer function F will have an increased effective impedance R_{eff} and a corresponding decrease in bandwidth

In switch phase S1, operating the amplifier with the feedback network has the effect of decreasing the effective transconductance of the amplifier. When a transconductance device is operating with 100% of its output voltage being fed back to its gate, Fig. 4.9a, like how the OTA operates in phase S0, any change in V_{out} has a corresponding gmV_{out} worth of current giving an effective impedance of $1/gm$. Inserting a block into the feedback path attenuates the V_{out} to V_{gs} return signal, Fig. 4.9b, causing only $gmV_{\text{out}}F$ worth of output current response. Increasing the OTA gain by inserting the feedback block has the effect of increasing the effective impedance of the OTA.

To calculate the total output noise for the S1 switch resistors, the amplifier's $\omega_{3_{\text{dB}}}$ frequency is calculated to find the NEB (4.26), and then the NEB is substituted into (4.24). Assigning the variable name C_{leff} to represent the total effective output load capacitance, and remembering that a capacitor which is being driven differentially has an effective

capacitance twice its rated value, the total switch noise can be derived as (4.27).

$$NEB = \frac{BW}{4}$$

$$BW = \frac{gm_1 F}{2C_{leff}} \tag{4.25}$$

$$NEB = \frac{gm_1 F}{4(2C_{leff})} \tag{4.26}$$

$$V^2_{out_{noise_{RS1}}} = \frac{kT}{C_{leff}} A^2_{cl}\, R_{S1}\, gm_1 F \tag{4.27}$$

The other noise contributor for phase $S1$ is the OTA's thermal noise. The input referred thermal noise is directly at the input gates of the OTA, so the output noise is the OTA's input noise, (4.10), transferred to the output as a function of F and bounded by the NEB (4.28), which can be reduced to (4.29).

$$V^2_{onoise_{OTA}} = 8kT\frac{\gamma_1}{gm_1}\, nf\, \frac{1}{F^2}\, NEB \tag{4.28}$$

$$V^2_{onoise_{OTA}} = 8kT\frac{\gamma_1\, nf}{gm_1}\, \frac{1}{F^2}\, \frac{gm_1\, F}{8\, C_{leff}}$$

$$V^2_{onoise_{OTA}} = \frac{kT}{C_{leff}}\frac{\gamma_1\, nf}{F} \tag{4.29}$$

Summing the two noises (4.27) and (4.29) together results in (4.30), which is the total SC phase $S1$ noise contribution.

$$V^2_{noise_{S1}} = \frac{kT}{C_{leff}}\left(A^2_{cl}\, R_{S1}\, gm_1\, F + \frac{\gamma_1\, nf}{F}\right) \tag{4.30}$$

From (4.30), if the closed loop gain is approximated to be $A_{cl} \approx 1/F$ (the accuracy of this approximation is determined by actual ratio A_{cl} and F), and the $\gamma_1 nf \approx 1$ (it is normally greater than 1) then (4.30) can be reduced to show that as long as the R_{S1} switch resistance is much less than $1/gm$, then the phase S1 noise comes almost entirely from the OTA. Making the following rough approximation

$$A^2_{cl} \approx \frac{1}{F^2}$$

the noise formula can be simplified to

$$V^2_{noise_{S1}} = \frac{kT}{C_{leff}F}(R_{S1}\, gm_1 + 1)$$

If the transistor's $1/gm$ is much greater than the switch's resistance, $1/gm_1 \gg R_{S1}$, then the noise can be further simplified to

$$V^2_{noise_{S1}} = \frac{kT}{C_{leff}} \frac{\gamma_1 \ nf}{F}. \tag{4.31}$$

The switch R_{S1} is designed to have much less on resistance than the OTA input device effective resistance, $\frac{1}{gm_1}$, so that the OTA bandwidth is dominated by the OTA's gm and not by the swtich resistance. With this simplification, (4.21) and (4.31) can be summed together to give the total system noise (4.41).

$$\begin{aligned} V^2_{noise_{total}} &= V_{noise_{S0}} + V_{noise_{S1}} \\ V^2_{noise_{total}} &= \frac{kT}{C_{eq}} \frac{\gamma_1 nf}{F^2} + \frac{kT}{C_{leff}} \frac{\gamma_1 \ nf}{F} \\ V^2_{noise_{total}} &= kT \frac{\gamma_{in} nf}{F} \left(\frac{1}{C_{eq} \ F} + \frac{1}{C_{leff}} \right) \end{aligned} \tag{4.32}$$

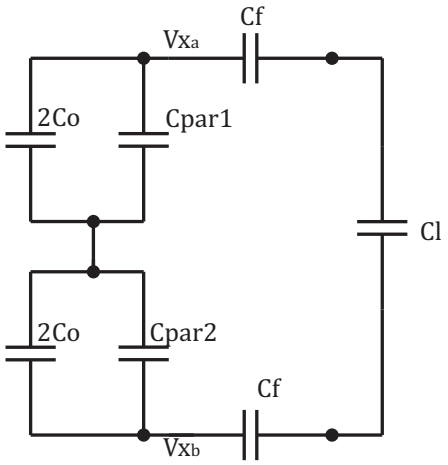


Figure 4.10: The circuit used to determine the OTA effective output capacitance C_{leff}.

C_{leff} is the effective load capacitance which is being driven by the OTA. C_{leff} includes all of the load, feedback, and parasitic capacitances which are being driven by the OTA's output node. The circuit in Fig. 4.10 can be used to calculate C_{leff}, and after a bit of algebra, C_{leff} can be expressed as (4.33).

$$C_{leff} = C_l + \frac{C_f}{2}(1 - F) \tag{4.33}$$

(4.32) can be used to solve for the amount of required C_{leff} required by the signal conditioning noise performance, and (4.33) can be rearranged to return the value for C_l (4.34).

$$C_l = C_{leff} - \frac{C_f}{2}(1 - F) \tag{4.34}$$

C_0 and C_f are constant design variables from the capacitive sensor and the required A_{cl}. The parasitics are themselves design constants because they can be pretty accurately approximated from the beginning of the design process, at least to the point where being slightly wrong will have only negligible impact on the system design. With constant values for C_0, C_f, and the parasitics, the design factors of C_{eq} and F can be calculated.

A major benefit for using (4.32) is that it is a formula which characterizes the entire switched capacitor thermal noise as a function of only two variables, $\gamma_1 nf$ and C_{leff} (because C_{eq} and F are determined by A_{cl} and the parasitics). As for the approximation of the parasitics, even if they are unknown and need to be guessed at, the chances that the on-chip parasitics are significantly greater than the 12 pF input capacitances from the capacitive sensor are pretty small, and therefore unlikely to significantly impact F (4.22). However, it is always good practice to revisit the early design steps as the design nears completion and update as necessary.

4.2.3 The Noise Factor and Effective Load Capacitance

To fully utilize the N bit ADC, the signal energy from the capacitive sensor versus the total error of the SC CDS system needs to be greater than or equal to the dynamic range (DR) of the ADC. Starting with a few basics, the signal energy is the rms squared energy of the OTA's peak to peak output voltage swing (4.35)

$$V^2_{signal_{rms}} = \left(\frac{\frac{1}{2} V_{out_{pp}}}{\sqrt{2}} \right)^2, \tag{4.35}$$

where $V_{out_{pp}}$ is the full scale output voltage from the pressure to analog conversion $V_{\mathrm{out_{FS}}} = A_{\mathrm{cl}} V_{\mathrm{in_{FS}}}$, which for this design is simply $2V_{\mathrm{dd}}$. The N bit ADC dynamic range

is the ratio of the total rms voltage energy that the ADC could measure at full scale versus the minimum amount of signal energy it could measure with 1 LSB (4.36).

$$DR = 10^{\frac{6.02*N+1.76}{10}}. \tag{4.36}$$

The total error budget is (4.37), which is the summation of the noise error and the settling error.

$$\epsilon_{total}^2 = \epsilon_{noise}^2 + \epsilon_{settling}^2 \tag{4.37}$$

Combining (4.35), (4.36), and (4.37) results in a formula which explicitly states how much error the system can tolerate based on the desired ADC resolution (4.38).

$$\epsilon_{total}^2 = \frac{V_{signal_{rms}}^2}{10^{\frac{6.02*N+1.76}{10}}} \tag{4.38}$$

The settling error, $\epsilon_{settling}$, from (4.37) is related to the bandwidth and the accuracy of the CDC conversion results, and will be discussed in a later section. This section will cover the derivation of two equations which solve for either $\gamma_1 nf$ as a function of C_{leff} (and therefore also C_l (4.34)) or C_{leff} as a function of $\gamma_1 nf$.

The total error is the sum of the $1/f$ noise, thermal noise, and the settling accuracy. For this project work, the $1/f$ noise has not been part of the noise calculations because the CDC system is using correlated double sampling techniques for the purpose of rejecting low frequency DC offset and noise. The noise design has been performed assuming that the low frequency noise response will be flat as long as the $1/f$ noise corner frequency is lower than the high pass cutoff frequency from the CDS system's transfer function [10].

Eq. (4.38) gives the entire noise error budget for the system, and if the noise design was performed to meet this requirement, then the total error budget would be used up entirely by the thermal noise leaving no margin for the settling error. At this point, it is a good idea to increase the required thermal noise SNR by a few dB, denoted by SNR_{extra} in (4.39). Creating the design variable SNR_{extra} will allow the designer to adjust how much error is given to noise and how much is given to settling. The percentage amount indicating how much is given to noise can be calculated with (4.40).

$$\epsilon_{noise}^2 = \frac{V_{signal_{rms}}^2}{10^{\frac{6.02*N+1.76+SNR_{extra}}{10}}} \tag{4.39}$$

$$noise\ fraction = 10^{-\left(\frac{SNR_{extra}}{10}\right)} \tag{4.40}$$

Now that there is an established value for the maximum allowed noise, it is possible to substitute

$$V^2_{noise_{total}} = \epsilon^2_{noise}$$

in the SC noise equation (4.41), and solve the resulting equation for either nf or C_{leff}.

$$\epsilon^2_{noise} = kT\frac{\gamma_{in}nf}{F}\left(\frac{1}{C_{eq}\ F} + \frac{1}{C_{leff}}\right) \tag{4.41}$$

$$\gamma_{in}\,nf = \frac{\epsilon^2_{noise}F}{kT\left(\frac{1}{C_{eq}F} + \frac{1}{C_{leff}}\right)} \tag{4.42}$$

$$C_{leff} = \frac{kT\gamma_{in}\,nf\,C_{eq}F}{\epsilon^2_{noise}F^2\ C_{eq} - kT\gamma_1 nf} \tag{4.43}$$

Most times (as is the case with this design), C_{leff} will already be a fairly large valued ADC input sample and hold capacitor. When this is the case, then it is only necessary to solve for nf (4.42).

4.2.4 Gain, Settling, and gm

The noise error is a purely random, non-deterministic error, and it is quantified using the output variance ϵ^2_{noise}, but the settling error is non-random, and quite deterministic. The settling error is comprised of two components, the dynamic settling error and the static settling error.

$$\epsilon_{settling} = \epsilon_{dynamic} + \epsilon_{settling}$$

Both of these errors can be described using the waveforms from Fig. 4.11. The waveform shows two traces, one of which was from the OTA when it was driving no C_l load capacitance, and the other when it was driving 4.6pF load capacitance. The settling error is the measure of how close the output voltage comes to reaching its target voltage, and as can be observed in Fig. 4.11, this error is not random. For this non-random error,

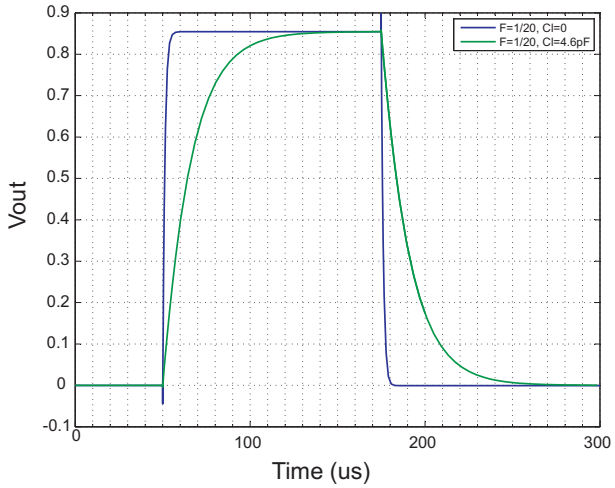


Figure 4.11: The OTA output voltage as the CDC system cycles through reset-sample-reset.

the total error (4.38) can be converted to its peak to peak equivalent (4.44), which should be around 1/2 LSB.

$$\epsilon_{total_{pp}} = \sqrt{\epsilon_{total}^2 2\sqrt{2}}, \tag{4.44}$$

and using (4.40), the remaining peak to peak error can be given to the settling error (4.45)

$$\epsilon_{settling} = \epsilon_{total_{pp}} \left(1 - 10^{-\left(\frac{SNR_{extra}}{10}\right)}\right) \tag{4.45}$$

The dynamic error in Fig. 4.11 is shown by the time it takes for the outputs to reach their desired goal of 850mV. The time constant for the dynamic error is $\tau = 1/\omega_{3_{\mathrm{dB}}}$ (4.25). From the two plots, it is evident that the waveform with the smaller time constant approaches its target potential much more quickly than the 4.6 pF loaded OTA, and should therefore be closer to the target output voltage than the slower wave at the end of the sample period. The other part of the settling error is the static error. This error arises from how close the waveform can get to its goal, $V_{\mathrm{out}} = V_{\mathrm{in}} A_{cl}$, if it had infinite time to settle. Eventually, as a function of the loop gain, $V_{\mathrm{out}} = V_{x_{ab}} T_0$, the amplifier will stop trying to get any closer to the target potential $V_{\mathrm{out}} = V_{\mathrm{in}} A_{cl}$.

Earlier it was calculated that the closed loop gain of the OTA is $2C_0/C_f$, but V_{out} is equal to $V_{\mathrm{in}} A_{cl}$ only if the open loop gain is infinite. A real amplifier circuit does not have infinite gain, and on top of that, because of F, it doesn't even have A_0 amount of loop gain.

The requirements for the settling error is that the gain and bandwidth of the amplifier must be great enough to settle the output to within ϵ_{settle} in only 1/2 period of the SC amplifier clock. The accuracy of the conversion is governed by the loop transfer function (4.46) which leads to the expression for the system static error (4.47).

$$T_0 = A_0\ F \tag{4.46}$$

$$\begin{aligned} \epsilon_{static} &= \frac{1}{T_0} \\ \epsilon_{static} &= \frac{1}{A_0\ F} \end{aligned} \tag{4.47}$$

The dynamic error of the amplifier can be solved using the amount of time available to settle, t_s, and the $\tau = 1/\omega_{3_{\mathrm{dB}}}$ time constant of the OTA. At low SC clock speeds, the settling time t_s is about one half the SC system clock period (where the clock period is $T_{sc} = 1/f_{sc}$, and the circuit bandwidth is (4.25), and the dynamic error is (4.48).

$$\begin{aligned} ts &= \frac{1}{2f_{sc}} \\ \tau &= \frac{2C_{leff}}{gm_1 F} \\ \epsilon_{dynamic} &= e^{-\frac{t_s}{\tau}} \\ \epsilon_{dynamic} &= e^{-\frac{gm_1\ F}{4\ f_{sc} C_{leff}}} \end{aligned} \tag{4.48}$$

Equations (4.47) and (4.48) can be combined to form (4.49), which solves the required gm as a function of the settling error and the open loop gain.

$$\begin{aligned} \epsilon_{dynamic} &= \epsilon_{settle} - \epsilon_{static} \\ e^{-\frac{gm_1\ F}{4\ f_{sc} C_{leff}}} &= \epsilon_{settle} - \epsilon_{static} \\ gm_1 &= -\frac{4\ C_{leff} f_{sc}}{F} \ln\left(\epsilon_{settling} - \frac{1}{A_0\ F}\right) \end{aligned} \tag{4.49}$$

For gm to be real and finite (4.50) must be true.

$$\epsilon_{settling} > \frac{1}{A_0 F} \tag{4.50}$$

Plotting (4.49) as gm versus A_0, Fig. 4.12, shows that minimum open loop gain requires infinite gm, and minimum gm requires infinite A_0, . However, increasing A_0 by a few dB quickly results in near minimum gm requirements.

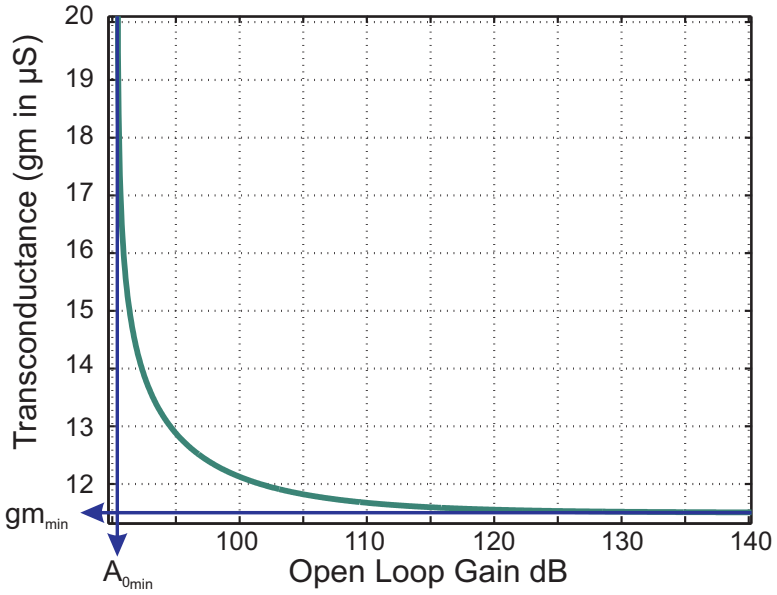


Figure 4.12: Plot of gm versus A_0 from (4.49) for $f_{sc} = 4kHz$ showing asymptotic behavior at minimum gm and minimum A_0.

4.3 The OTA Noise Factor Coefficient

At this point, the entire noise and bandwidth requirements of the capacitance to digital conversion system have been described in terms of nf, gm_1, and A_0. Achieving the required A_0 is a fairly in depth procedure and is discussed in a later chapter. This section will cover the design of the folded cascode amplifier to meet the nf and gm_1 requirements.

The folded cascode OTA, (without the gain boosting amplifiers), is given in Figure 4.13. The first step of the noise analysis is to realize that every MOSFET device in the circuit is contributing some noise current to the capacitive load, and the sum of all this current through the load shows up as output noise voltage. The noise current being generated by each of the devices is $I^2_{noise} = 4kT\gamma gm$, where k is Boltzmann's constant, T is the temperature in Kelvin, γ is the MOSFET thermal noise factor [7], and gm is the transconductance. For the noise analysis, the transistors can be replaced by their equivalent noise model, and simple current divider ratios can be used to determine the flow path of the individual noise currents, Fig 4.14.

Fig. 4.14a shows the N-type cascode load transistors, with the P-Type load replaced by a current source. Looking at the noise current flow at the source of the M2 transistor,

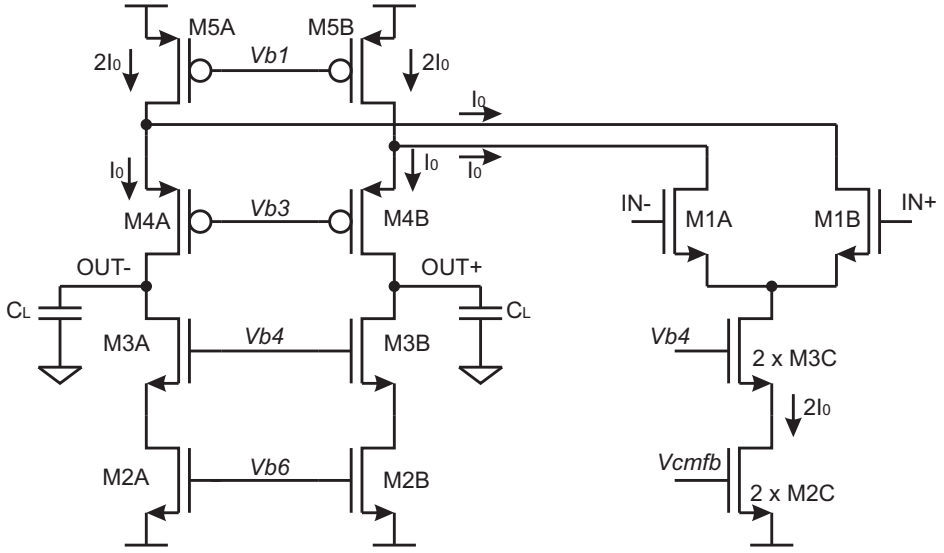


Figure 4.13: The folded cascode amplifier without the gain boosting amplifiers.

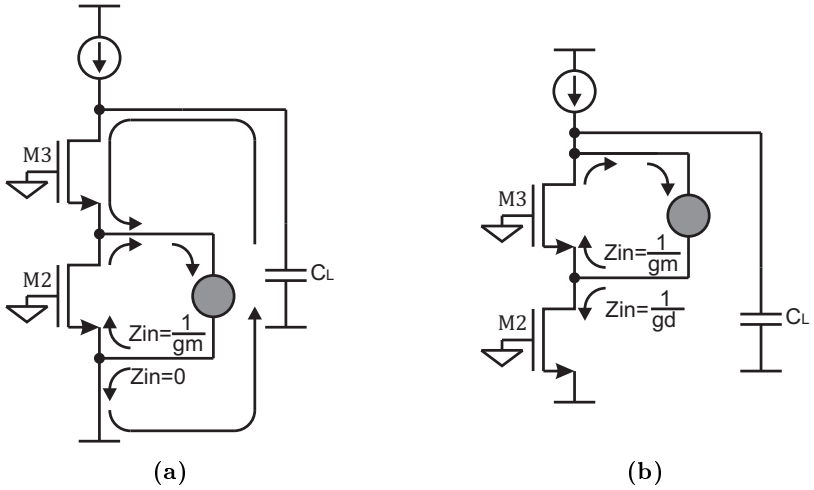


Figure 4.14: The cascode load noise sources showing some of the possible paths for current flow.
a) The equivalent circuit for noise analysis of the load device. All of the noise current will flow into the Zin=0Ω branch
b) The equivalent circuit for noise analysis of the cascode device. Becsause $1/gm \ll 1/gd$, almost 100% of the noise current will form a closed loop inside the cascode device.

there are two paths which the current could flow. One path is to flow back into the MOSFET device against the $1/gm_{\mathrm{M2}}$ source impedance, where it would, according to the Kirchoff's current law, form a closed loop and therefore not have any impact on

the output load. The other path is to flow into the 0Ω impedance ground where the current would flow through the load on its way back to the M2 current noise source. In this case it should be clear that 100% of the current will flow into the 0Ω impedance of ground rather than the $1/gm_{\mathrm{M2}}$ source impedance. This means that for the cascode amplifier, the M2 load transistor contributes all of its noise current to the output.

Performing the same type of analysis on the M3 cascode device, Fig. 4.14a, will result in a different outcome because at M3's source, the current once again is impeded on one path by $1/gm_{\mathrm{M3}}$ impedance, but the other path is the $1/gd_{\mathrm{M2}}$, where gd_{M2} is the device's output conductance. To know how much current flows through M3, a simple current divider ratio can be calculated (4.51).

$$i(M3) = i_{n_{\mathrm{M3}}} \left(\frac{gm_{\mathrm{M3}}}{gm_{\mathrm{M3}} + gd_{\mathrm{M2}}} \right) \tag{4.51}$$

Because normally normally $gm_{\mathrm{M3}} \gg gd_{\mathrm{M2}}$ (for the 130nm technology used in this project the ratio is usually at least 30:1), then (4.51) reduces to being close to unity. Because virtually all of the M3 noise current loops back through M3, then almost 0 current loops through the output load. Even though there is some noise current from the cascode devices, for the purpose of this amplifier design, the noise analysis will proceed as if the cascode devices do not contribute to the output noise current.

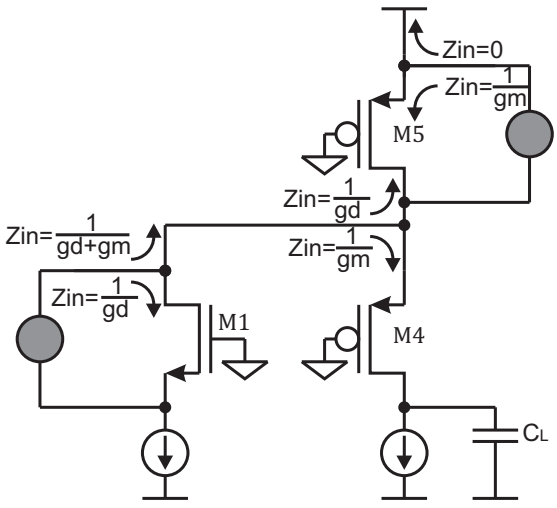


Figure 4.15: The circuit used for the noise analysis of the input device and P-type cascode load network.

The same analysis can be performed on the M4 and M5 cascode load devices, resulting in the same outcome as the M2 and M3 devices. Looking at the drain of the input device in Fig. 4.15, the noise current source also sees high impedance looking into the M1 drain, and low impedance looking into the M4 cascode source. Because of this, it will be assumed that virtually all of the of the input device noise is applied to the output load. The differential pair tail current biasing load transistor also sources noise current, but because this noise is common mode to the input differential pair, its contribution will not be considered in the noise analysis. At this stage, the noise sources of the folded cascode amplifier which source noise current to the outputs have been identified as M1, M2, and M5. The goal is to input refer this total output noise current to an input noise voltage so that the noise behavior of the amplifier can be well defined.

4.3.1 Noise Factor Derivation

The M1 input device of the folded cascode is the only amplifying device in the amplifier. All of the other devices act as the output load. The most effective method for input referring the OTA output noise current is to sum together all of the device noise currents, and to input refer them to the M1 input device. The V^2 to I^2 ratio of the M1 input device is gm_1^2, so if the device output noise current is divided by gm_1^2, this will result in the M1 input referred voltage (4.53).

$$I^2_{noise_{out}} = 4kT\gamma_1 gm_1 \tag{4.52}$$

$$V^2_{noise_{in}} = 4kT\frac{\gamma_1}{gm_1} \tag{4.53}$$

To input refer the total output noise current, the total OTA output current will be divided by the input device gm_1. The simplified common source amplifier circuit in Fig. 4.16 shows how the output currents are summed together (4.54) and input referred to the M1 input device (4.55). Comparing (4.53) and (4.55), the input device OTA noise scaling factor for the Fig. 4.16 circuit is (4.56).

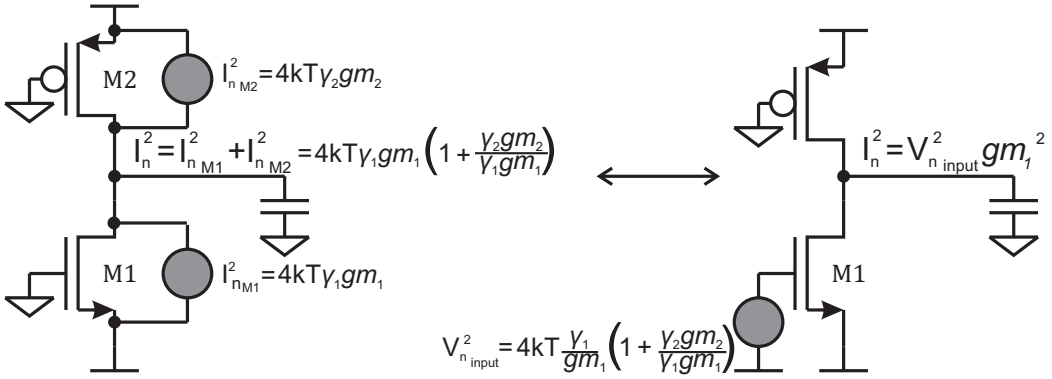


Figure 4.16: Input referred system noise current

$$I^2_{noise_{out}} = 4kT\left(\gamma_1 gm_1 + \gamma_2 gm_2\right) \tag{4.54}$$

$$V^2_{noise_{input}} = 4kT\frac{\gamma_1}{gm_1}\left(1+\frac{\gamma_2 gm_2}{\gamma_1 gm_1}\right) \tag{4.55}$$

$$nf = \left(1+\frac{\gamma_2 gm_2}{\gamma_1 gm_1}\right) \tag{4.56}$$

This folded cascode design uses MOSFETs biased in very different modes of operation. The input devices are operating in weak inversion and the load devices are operating in strong inversion, and the cascode devices are operating somewhere in between. Each device is operating at different levels of gm, but they are all biased with fixed current ratios. In Fig. 4.13, M5A and M5B are both is flowing $2I_0$, and every other transistor (not including the common mode current source M2C and M3C) is flowing I_0. To help relate the behavior of all of the different transistors, it is useful to represent each MOSFET in terms of its transconductance efficiency ratio (4.57), and to derive nf as a funtion of η_{gm} (4.58)

$$\eta_{gm} = \frac{gm}{I_d} \tag{4.57}$$

$$nf = 1+\frac{\gamma_2}{\gamma_1}\frac{I_{d_2}\eta_{gm_2}}{I_{d_1}\eta_{gm_1}} \tag{4.58}$$

If you replace gm with $I_d\eta_{gm}$, then for equal drain currents, the input referred noise

voltage for the circuit in Fig. 4.16 would reduce to (4.59).

$$V^2_{noise_{input}} = 4kT\frac{\gamma_1}{gm_1}\left(1 + \frac{\gamma_2\eta_{gm_2}}{\gamma_1\eta_{gm_1}},\right) \tag{4.59}$$

Eq. (4.59) shows that *nf* is always greater than 1 by the fraction $\gamma_2\eta_{gm_2}/\gamma_1\eta_{gm_1}$. The η_{gm} values are simply gm/I_d, but the γ noise coefficient is not so evident. Most of the textbooks [11, 12, 13] state that the thermal noise factor γ for devices in strong inversion is simply 2/3. However, as stated earlier, this amplifier has devices conducting in many different modes of operation. One big issue is that the M1 input devices are operating in weak inversion where the noise source stops being the MOSFET saturation noise current (where γ is roughly 2/3), and starts to behave more like the shot noise of a BJT device [14].

As a charge carrier crosses a PN junction, such as what occurs in the MOSFET channel operating in the subthreshold region, its velocity changes as it passes through, and reemerges, on the other side of the junction barrier. This increase and decrease in velocity creates a little spike of noise for each electron passing through the junction barrier. The random arrival of the charge carriers to the junction barrier creates a broadband output noise current which is directly proportional to the amount of current flowing through the device (4.60) [15]. Dividing (4.60) by the square of its weak inversion *gm*, (4.61), gives the input referred shot noise voltage of the device in weak inversion saturation to be (4.62).

$$I^2_{shotnoise_{out}} = 2qI_d \tag{4.60}$$

$$gm = I_d\left(\frac{nkT}{q}\right) \tag{4.61}$$

$$V^2_{shotnoise_{in}} = \frac{2q}{I_d}\left(\frac{nkT}{q}\right)^2 \tag{4.62}$$

The noise currents (4.60) and (4.52) are not equal to each other. This means that, if (4.59) is going to be used to quantify *nf*, then it is necessary to know the value of γ across all operating regions.

It would be possible to mathematically derive a set of functions which could quantify the η_{gm} and γ values across the entire spectrum from very weak inversion to very strong inversion. But, it would be very tedious work to accomplish this derivation, and it

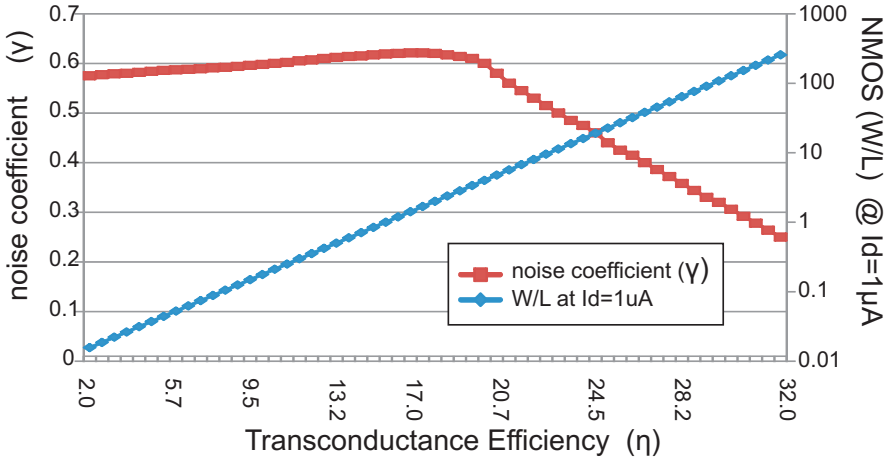


Figure 4.17: Simulation results plotting the noise coefficient γ and the device $\frac{W}{L}$ ratio at $I_d = 1\mu A$ and channel length $L = 400n$ as a function of an NMOS device $\eta = \frac{gm}{I_d}$ ratio.

would be easier if there was a lookup table which listed values relating the γ noise coefficient to the device η_{gm} values. So, instead of deriving general math equations for the γ characterization, Spectre simulations were performed to generate tabular data of the noise coefficients. From the Spectre simulations, the η_{gm} and γ were extracted from the results, and the results are plotted in Fig. 4.17.

The accuracy of the extracted η_{gm} and γ values are very dependent on the accuracy of the device model files. But, assuming that the IC fab was thorough in its device characterization, then all of the various characteristics of the particular technology being used, such as the short channel, long channel, weak inversion, strong inversion, depletion capacitance and so on, will be neatly bundled together in the simulation. The simulation output should be a nice clean curve which gives a very good idea of the transistors' behavior. The simulation data for characterizing the NMOS device γ coefficient and W/L ratio as a function of the device transconductance efficiency, η_{gm}, is plotted in Fig. 4.17. The same simulations were performed for the PMOS devices, but the simulation results, which are similar but slightly different to the NMOS results, are not listed here.

At this point, the nf for the folded cascode amplifier from Fig. 4.13 can be derived as a function of the ratios of the various device I_d drain currents, and their $\gamma\eta_{gm}$

values (4.65).

$$I^2_{noise_{OTA}} = 4kT\left(\gamma_1 gm_1 + \gamma_2 gm_2 + \gamma_5 gm_5\right) \tag{4.63}$$

$$V^2_{noise_{OTA}} = 4kT\frac{\gamma_1}{gm_1}\left(1 + \frac{\gamma_2 gm_2}{\gamma_1 gm_1} + \frac{\gamma_5 gm_5}{\gamma_1 gm_1}\right)$$

$$V^2_{noise_{OTA}} = 4kT\frac{\gamma_1}{gm_1}\left(1 + \left(\frac{I_{d_2}}{I_{d_1}}\right)\frac{\gamma_2\eta_{gm_2}}{\gamma_1\eta_{gm_1}} + \left(\frac{I_{d_5}}{I_{d_1}}\right)\frac{\gamma_5\eta_{gm_5}}{\gamma_1\eta_{gm_1}}\right) \tag{4.64}$$

$$nf = 1 + \left(\frac{I_{d_2}}{I_{d_1}}\right)\frac{\gamma_2\eta_{gm_2}}{\gamma_1\eta_{gm_1}} + \left(\frac{I_{d_5}}{I_{d_1}}\right)\frac{\gamma_5\eta_{gm_5}}{\gamma_1\eta_{gm_1}} \tag{4.65}$$

Substituting in the device current ratios, and choosing to design the load devices with equal $\gamma\eta_{gm}$ values give an nf of (4.66).

$$nf = 1 + 3\left(\frac{\gamma_{load}\eta_{gm_{load}}}{\gamma_1\eta_{gm_1}}\right) \tag{4.66}$$

4.4 The Folded Cascode Device Sizing

All of the design requirements for sizing the folded cascode M1, M2, and M5 transistors are fully characterized through the design equations for gm and nf.

1. Starting with the design's desired pressure read range, the capacitive sensor with its nominal capacitance C_0, and pressure sensitivity C_s, the required A_{cl} and $C_f = 2C_0/A_{cl}$ can be calculated (a detailed description of how to do this is given in Chapter 3).

2. Make some assumptions about the expected parasitics and solve for C_{eq} and F (4.14) and (4.22).

3. Based on the desired ADC dynamic range, (4.36), apportion some of the error for the noise error (4.39).

4. Solve for C_{leff} as a function of nf, or solve for nf as a function of C_{leff} (4.42), and (4.43)

5. Select the $\gamma\eta_{gm}$ efficiency values for the M1 input devices and the M2 and M5 load devices

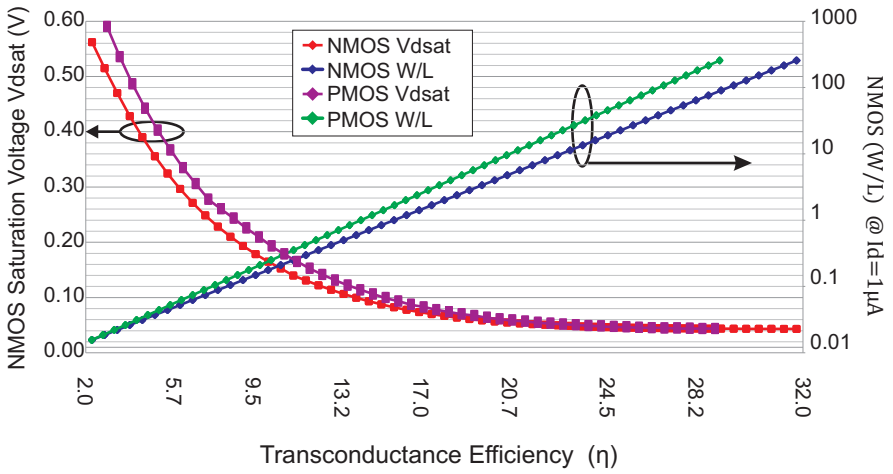


Figure 4.18: Spectre simulation results plotting the MOSFET device saturation voltage and W/L ratio versus the η_{gm} efficiency values of the 130nm MOSFET devices.

According to (4.65), the smaller the value given to the load $\gamma\eta_{gm}$, the easier it is to have a small *nf*. Unfortunately, as is shown in Fig. 4.18, smaller η_{gm} results in a larger V_{dsat} of the MOSFET device. Because the usable output voltage swing is limited on top and bottom by the saturation voltages of the output load devices, it is desirable to have a very small V_{dsat}. Load devices which have small V_{dsat} are devices with a large η_{gm} value, but load devices with large η_{gm} increase the *nf*. The optimal solution is to design the amplifier with as large of an η_{gm} value as possible for the load devices while still maintaining an *nf* which meets the noise requirements.

Taking the tabulated noise and efficiency values from Fig. 4.17 and loading them into Matlab, a 3D surface plot solving the folded cascode *nf* function can be created, Fig. 4.19a and (4.66). The surface plot plots all of the solutions to (4.66) as a function of the device η_{gm} values. In the Matlab environment, it is fairly trivial to limit the plotter output to only plot the values which fulfill the *nf* design requirements. Figs. 4.18 and 4.19b, can be used to choose an η_{gm} value for the input, η_1, and the load devices η_2, which will meet the *nf* requirements while providing the widest output swing with the best input device transconductance efficiency.

(. . . Continued from earlier. . .)

6. Find the required gm_1 for the sample rate and C_{leff} (4.49).

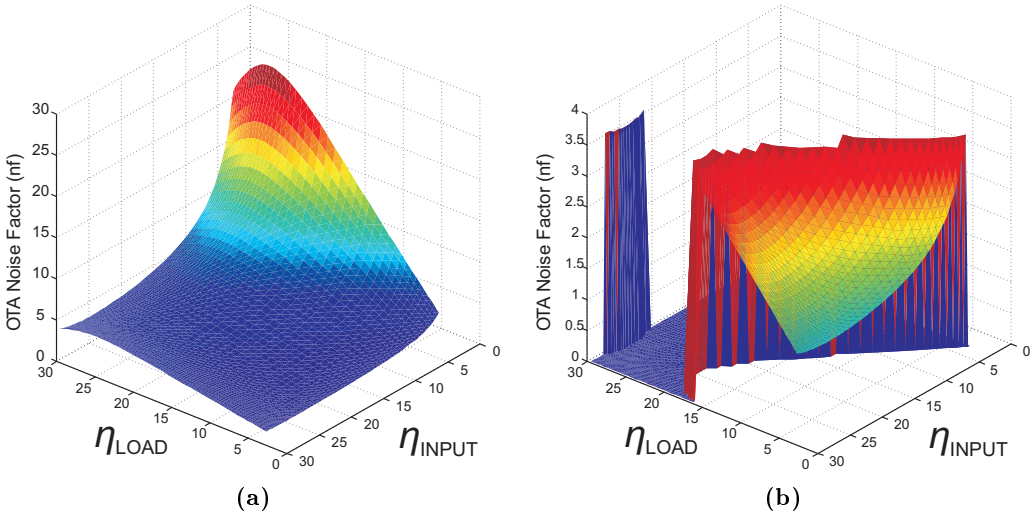


Figure 4.19: The solution for (4.66) using the data from 4.17
a) The solution for all values of *nf*.
b) The solution for only the values of *nf* less than 3.6.

7. With the required input device gm_1 and the chosen η_{gm} values, solve for the Fig 4.13 bias current $I_0 = gm_1/\eta_{gm_1}$

8. With the η_{gm} and I_d values, along with the plots for W/L vs. η_{gm}, Fig. 4.18 or 4.17, choose the W/L ratios for various OTA transistors.

The W/L data in Figs. 4.18 and 4.17 is a function of η_{gm}, but only for $I_{\text{ds}} = 1\mu A$, and it must be scaled to the actual device current to maintain the same η_{gm}. For example, if the bias current should be 2µA, then all of the W/L ratios from Fig. 4.18 need to be doubled. If the η_{gm} is maintained, then V_{dsat} remains virtually unaffected.

At this point, all of the design formulas which are used to design the folded cascode amplifier to meet the noise and bandwidth requirements of the signal conditioning system have been derived, and the method for sizing the various amplifier transistors to meet the bandwidth and *nf* has been shown. Noise and bandwidth are only two of the design characteristics which are important for ADC drivers, the third is the amplifier open loop gain which determines how accurately the amplifier is able amplify the input signal to the ideal output signal. For this design, the simple folded cascode OTA only gives about 70 dB of gain, but the required open loop gain from (4.50) is more than 100 dB. The following chapter will describe the method used for attaining the required

open loop gain, and the final amplifier design will be given listing the bias current and all of the transistor η_{gm} values.

5

The Gain Boosted Folded Cascode Amplifier Design

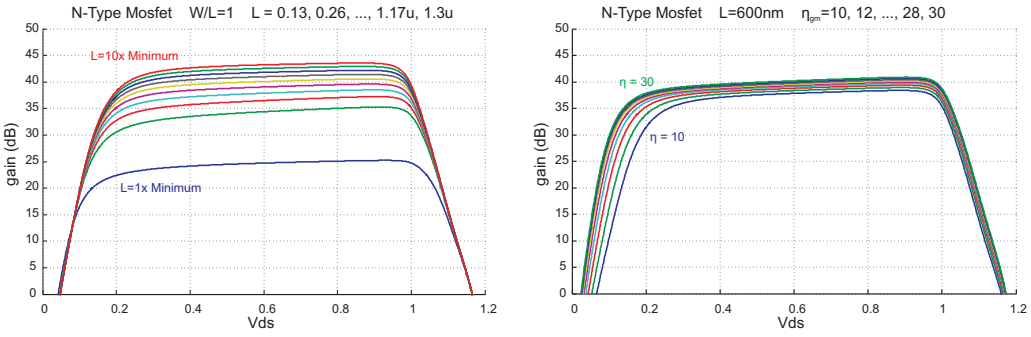
ADC drivers require very high accuracy to meet the settling requirements of the signal conditioning circuitry, and the amplifier's accuracy is determined by its open loop DC gain. High gain can be achieved using a multistage cascaded amplifier, but the main drawback is the greatly increased power consumption incurred by each successive amplifier stage. Another option for increasing the DC gain is to implement a gain boosted cascode stage as the amplifier's output load.

The amplifier developed for this project has been designed to provide very large DC gain over a wide output swing, and to consume an absolute minimum of power. Towards the goal of achieving wide output swing, a folded cascode architecture is used which allows the output node voltages to approach the power supply rail potentials minus the saturation voltages, V_{dsat}, of the load devices. To achieve very high DC open loop gain, the gain enhancement effect of a folded cascode architecture is further increased by adding extra amplifiers to drive the gates of the cascode devices. To keep the overall system power consumption low, all of the system's amplifiers (the main folded cascode OTA and the gain boosting OTAs) are single stage designs employing switched capacitor common mode feedback networks and floating bias voltage generators.

5.1 Enhancing the Amplifier Gain

The voltage gain of an amplifier is the input transconductance multiplied by the output impedance, $gm_1 Z_{out}$. The $\eta_{gm} = gm/I_d$ transconductance efficiency ratios for each device is determined by the OTA noise factor nf requirements, and to try to increase the gain by increasing gm_1 will increase the power consumption beyond what is necessary to meet the system SNR and bandwidth requirements.

The other option for increased gain is to increase the output impedance. One of the most basic options for increasing the output impedance of a MOSFET is to increase its channel length. Fig. 5.1a shows the gain improvement of the MOSFET device for increasing channel length while maintaining constant W/L ratio and η_{gm} values. The improvement from increasing the channel length from minimum channel length to only a few multiples of the minimum channel length is pretty large, but the improvements start to flatten out once the channel length is about 5x minimum channel length.



(a) (b)

Figure 5.1: Simulation for characterizing the MOSFET intrinsic gain gmr_0.
a) The W/L ratio and I_d are kept constant for constant η_{gm}, and the channel length is stepped across minimum length to 10x minimum length.
b) The I_d is kept constant, and the W/L ratio is stepped logarithmically to perform a linear sweep of η_{gm} from 10V^{-1} to 30V^{-1}.

Fig. 5.1b are the simulation results from stepping the η_{gm} value of the NMOS transistor from 10V^{-1} to 30V^{-1}. The plot shows that the gain of the device is not as greatly affected by different modes of operation as greatly as it is with different channel lengths, but that there is a pretty significant increase in the output swing of the device with increasing device gm. This is a direct consequence of the V_{dsat} reduction as the device

moves its mode of operation from strong inversion to weak inversion.

Considering the gain improvement from increased channel length, Fig. 5.1a shows that for every doubling of the channel length, which at constant W/L corresponds to a quadrupling of the device area, the gain is increased by only about 6 dB, or 2x the voltage gain. If the device's intrinsic gain was 30dB, but the system needed 60dB of gain, trying to achieve the extra 30dB of gain by increasing the channel length would require quadrupling the device area 5 times over. Multiplying the gate area by $4^5 = 1024$ would be a pretty painful way of getting an extra 30dB of gain.

5.1.1 The Cascode Load

A better method would be to use two transistors, each with 30 dB of intrinsic gain, and configure them in such a way that their gains were multiplied with each other, which would give a total of 60dB of gain with only 2x the amount of device area instead of 1024x the area. This method of increasing the gain is called cascode loading, and this operation is performed by the Fig. 5.2 transistors $M3_{ABC}$ and $M4_{AB}$.

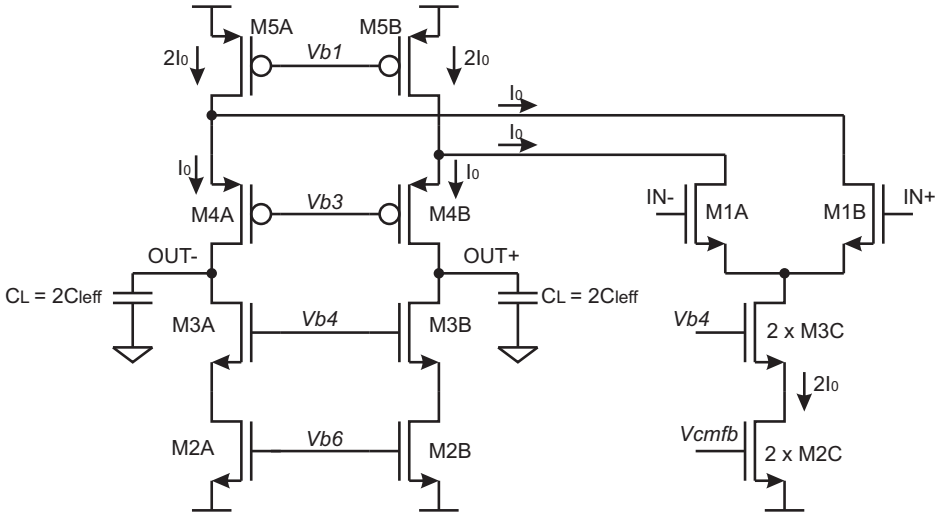


Figure 5.2: The folded cascode amplifier without the gain boosting amplifiers.

Cascoding is nice because with relatively little effort, the gain of the amplifier can be dramatically increased. If the intrinsic gain of the MOSFET device were 30 dB, the simple cascoded amplifier, such as the the one in Fig. 5.2, can increase the amplifier voltage gain to 60 dB without consuming any extra power. It is true that the enhanced 60 dB of gain is only available when the cascode devices are in saturation, but even

after the output voltage has swung to the point where the cascodes have come out of saturation and are no longer doing anything, the amplifier would still have the original, non-cascoded, r_0 impedance of the load device.

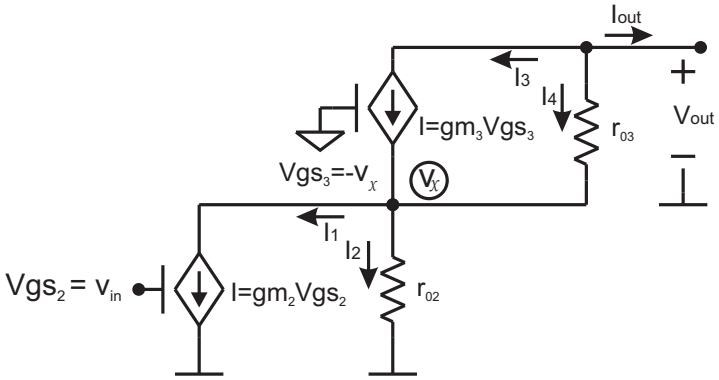


Figure 5.3: The cascode equivalent circuit for small signal impedance derivation

Using the circuit from Fig. 5.3, a small signal analysis on the equivalent N-Type cascode load can be performed to find the cascode load output impedance. The cascode amplifier's gain is its effective transconductance times the effective the effective output impedance, $A = gm_{eff}R_{ocasn}$.

To find the output impedance, the first step is to short circuit output to ground and to solve for $i_{out}/v_{in} = gm_{eff}$

$$i_1 + i_2 = i_3 + i_4 = -i_{out}$$

$$i_1 = v_{in}gm_2 \qquad i_2 = \frac{v_\chi}{r_{0_2}}$$

$$i_3 = -v_\chi gm_3 \qquad i_4 = \frac{-v_\chi}{r_{0_3}}$$

Solve for v_χ

$$i_1 = -i_2 + i_3 + i_4$$

$$v_{in}gm_2 = -v_\chi\left(\frac{1}{r_{0_2}} + \frac{1}{r_{0_3}} + gm_3\right)$$

$$v_{in}gm_2 = -v_\chi\left(\frac{r_{0_2} + r_{0_3} + r_{0_2}r_{0_3}gm_3}{r_{0_2}r_{0_3}}\right)$$

$$v_\chi = -v_{in}\left(\frac{gm_2 r_{0_2}r_{0_3}}{r_{0_3} + r_{0_2}(1 + r_{0_3}gm_3)}\right)$$

Substitute v_χ into $i_1 + i_2 = -i_{out}$ and solve for $gm_{eff} = i_{out}/v_{in}$

$$-i_{out} = v_{in} gm_2 + \frac{v_\chi}{r_{0_2}}$$

$$-i_{out} = v_{in} gm_2 - v_{in} \left(\frac{gm_2 r_{0_3}}{r_{0_3} + r_{0_2}(1 + r_{0_3} gm_3)} \right)$$

$$-i_{out} = -v_{in} \left(\frac{-gm_2(r_{0_3} + r_{0_2}(1 + r_{0_3} gm_3)) + gm_2 r_{0_3}}{r_{0_3} + r_{0_2}(1 + r_{0_3} gm_3)} \right)$$

$$gm_{eff} = \frac{-gm_2 r_{0_2}(1 + r_{0_3} gm_3)}{r_{0_3} + r_{0_2}(1 + r_{0_3} gm_3)}$$

The next step for deriving the cascode output impedance is to open circuit the output, and find $A = v_{out}/v_{in}$.

$$\begin{aligned} i_{out} &= 0 \\ i_1 &= -i_2 \\ v_\chi &= -v_{in} gm_2 r_{0_2} \\ v_{out} &= v_\chi + v_\chi gm_3 r_{0_3} \\ v_{out} &= -v_{in} gm_2 r_{0_2}(1 + gm_3 r_{0_3}) \\ \frac{v_{out}}{v_{in}} &= A = -gm_2 r_{0_2}(1 + gm_3 r_{0_3}) \end{aligned} \tag{5.1}$$

An interesting point about (5.1) is that the open loop gain of the common source M2 amplifier is $gm_2 r_{0_2}$, and the open loop gain of the M3 common gate amplifier is $(1 + gm_3 r_{0_3})$. Equation (5.1) shows that the open loop gain of the cascode is simply the product of the two individual open loop gains, and that if the gain of the $gm_3 r_{0_3}$ should go to zero there would still be the original uncascoded $gm_2 r_{0_2}$ amount of gain. If the cascode gain is $A = gm_{eff} R_{ocasn}$, then $R_{ocasn} = A/gm_{eff}$

$$R_{ocasn} = r_{0_3} + r_{0_2}(1 + r_{0_3} gm_3) \tag{5.2}$$

For the purpose of this amplifier design, the following approximation was made:

$$r_{0_3} + r_{0_2} \ll r_{0_2} r_{0_3} gm_3$$

which gives the N-cascode network an output impedance of (5.3). The same derivation can be performed on the M1, M4 and M5 input device if the P-type cascode load, and

the resulting impedance is (5.4). Combining (5.3) and (5.4), the folded cascode amplifier open loop DC gain is (5.6).

$$R_{ocasn_{folded}} \approx gm_3 r_{0_3} r_{0_2} \tag{5.3}$$

$$R_{ocasp_{folded}} \approx gm_4 r_{o4}(r_{o5}||r_{o1}) \tag{5.4}$$

$$R_{out_{folded}} = R_{ocasn_{folded}}||R_{ocasp_{folded}} \tag{5.5}$$

$$A_{folded} = gm_1 R_{out_{folded}} \tag{5.6}$$

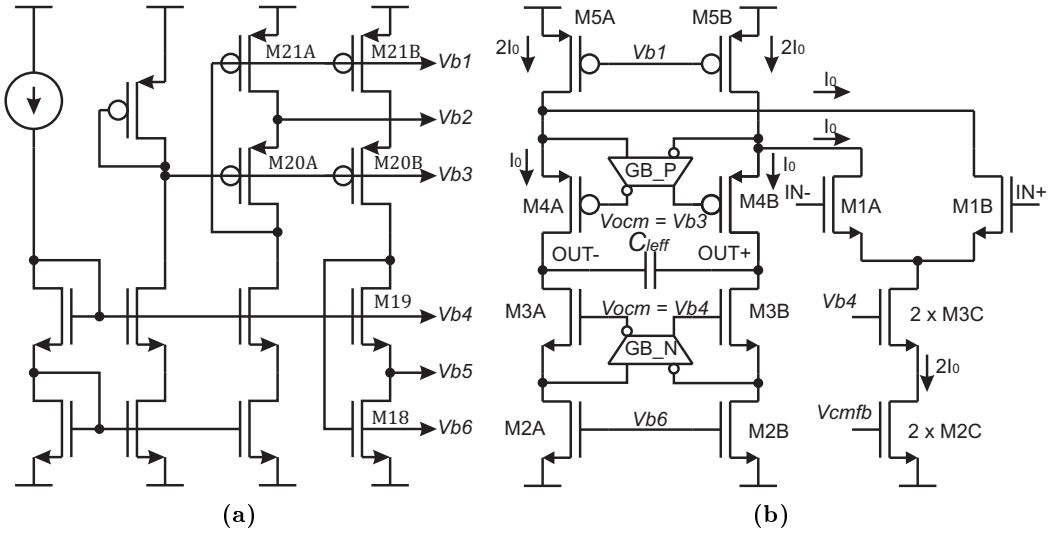


Figure 5.4: The circuit diagrams for the amplifier electronics
a) The system reference bias generator. b) The gain boosted folded cascode amplifier.

Adding gain boosting amplifiers to the Fig. 5.2 folded cascode results in the gain boosted folded cascode amplifier in Fig. 5.4b, shown alongside the reference bias circuit. The gain boosters work to keep the $M5_{AB}$ (and $M2_{AB}$) drain voltages equal by applying gate biasing to $M4_{AB}$ (and $M3_{AB}$). The gain boosting amplifiers increase the standard cascode output impedance (5.5) by a factor of $(A_{o_{GB_{pn}}} + 1)$, which is approximated to $A_{o_{GB_{pn}}}$ (5.7), where $A_{o_{GB_{pn}}}$ is the open loop gain of the corresponding P or N gain boosting amplifier. This results in a total gain boosted cascode amplifier gain of (5.9).

$$R_{ocasn_{GB}} \approx R_{ocasn_{folded}}(A_{o_{GB_n}}) \tag{5.7}$$

$$R_{ocasp_{GB}} \approx R_{ocasp_{folded}}(A_{o_{GB_p}})$$

$$R_{out_{GB}} = R_{ocasp_{GB}} || R_{ocasn_{GB}} \tag{5.8}$$

$$A_{total} = gm_1 R_{out_{GB}} \tag{5.9}$$

When the gains of the two gain boosters are about equal, then the output impedance of the gain boosted amplifier is the output impedance of the folded cascode multiplied by $A_{o_{GB}}$ (5.10). This makes the total gain (5.11), and combining (5.6) and (5.11) results in (5.12).

$$R_{out_{GB}} = R_{out_{folded}}(A_{o_{GB}}) \tag{5.10}$$

$$A_{total} = gm_1 R_{out_{folded}}(A_{o_{GB}}) \tag{5.11}$$

$$A_{total} = A_{folded}(A_{o_{GB}}) \tag{5.12}$$

5.1.2 Quantifying the Gain Enhancement

Very simply stated, each device has its own intrinsic gain, $A_0 = gmr_0$, and a cascode amplifier has a gain which is the product of those two gains. The gain of the boosted folded cascode amplifier is the product of the gains from the basic folded cascode amplifier and the gain of the boosting amplifier. If the gain boosting amplifiers are also cascode structures, then gain of the gain boosted folded cascode is a function of the MOSFET device intrinsic gmr_0 gain raised to the fourth power $A_{total} = A_0^4$.

It was previously stated that to increase the gain of a single transistor from 30 to 60 dB amplifier would require a 4^5 increase in device area. With cascoding, the simple act of adding a second equally sized transistor will provide the same 30 dB of gain at the expense of only about 50mV of device saturation voltage. Further enhancing the gain with cascoded gain boosting amplifiers will provide another 60 dB of gain with no cost in terms of output swing reduction. For an intrinsic device with gain of about $gmr_0 = 30$dB, the gain boosted folded cascode amplifier will have about 120dB worth of gain using almost minimum channel length transistors (Fig. 5.1a).

If the design calls for more than 120 dB, then the channel lengths can be increased to give more gain. However, the gain boosted folded cascode amplfier gain increases at a rate of about 24 dB per doubling of channel length instead of the 6 dB for every doubling of the channel length of a single transistor amplifier.

5.2 Gain Booster Stability

For stability, the gain boosting ampliiňĄers are designed so that their gain bandwidth product (GBW_{GB}) is greater than the closed loop bandwidth of the folded cascode amplifier (BW_{folded}) (5.13), and less than the transition frequency f_T (5.14) of the corresponding cascode device which it is driving (5.15) [16] (either $M3_{AB}$ or $M4_{AB}$ from Fig. 5.4b).

$$F = \text{Feedback Factor}$$

$$BW_{folded} = \frac{gm_1\, F}{2\pi C_{load}} \tag{5.13}$$

$$f_{T_{34}} = \frac{gm_{34}}{2\pi C_{gs_{34}}} \tag{5.14}$$

$$BW_{folded} < GBW_{GB_{pn}} < f_{T_{34}} \tag{5.15}$$

5.3 Gain Boost Input Level Shifter

The gain boosting amplifiers are the telescopic cascode amplifiers from Fig. 5.5. Telescopic cascode amplifiers consume 50% less current than a folded cascode design with equivalent gain and bandwidth parameters. However, a telescopic design has some severe limitations concerning the output voltage swing, and the input to output common mode voltage relationship. Considering the GB_N boost network from Fig. 5.4b, GB_N's output node potential must be at least V_{gs_3} greater than its input node potential. However, looking at Fig. 5.5, GB_N's input devices will come out of saturation as the output node voltage approaches and exceeds the input voltage potential.

To correct for this, GB_N's input voltage is level shifted up to a voltage which allows the amplifier to remain in saturation. The SC shifter in Fig. 5.6 applies a DC offset from the drain of M2 to the input node of GB_N equal to $\frac{VDD}{2}$ minus the drain reference bias voltage V_{b_5}.

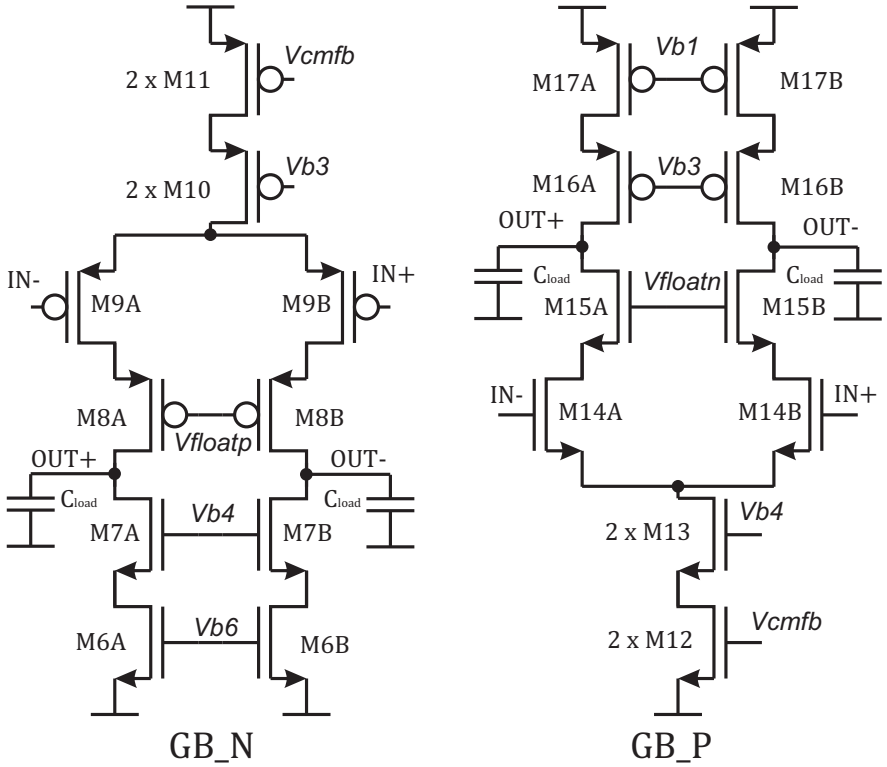


Figure 5.5: The gain boosting amplifiers for the P and N type cascode load networks.

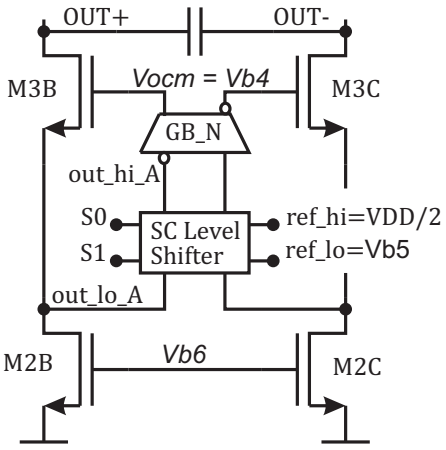


Figure 5.6: The SC shifter applies a DC shift from M2's drain to GB_N's input.

5.3.1 The Amount of Gain Boosting Enhancement

The level shifter schematic is given in Fig. 5.7, and it shows that in either switch phase $S0$ or $S1$, the SC level shifter has a total capacitance across its output nodes of

$C_{shift} = C_{sc_x} + C_d$. Fig. 5.8 gives a single ended representation of the gain boosting circuit with a half circuit of the SC level shifter. From Fig. 5.8, the feedback factor from M3's source to GB_N's input is (5.16) created by the SC network and the input parasitic capacitance giving an effective loop gain of (5.17).

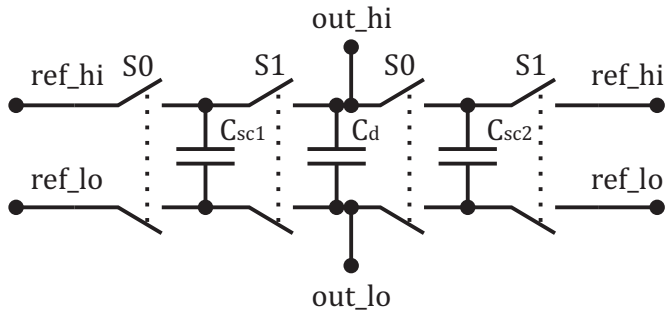


Figure 5.7: A single channel of the SC level shifter network used in Fig. 5.6.

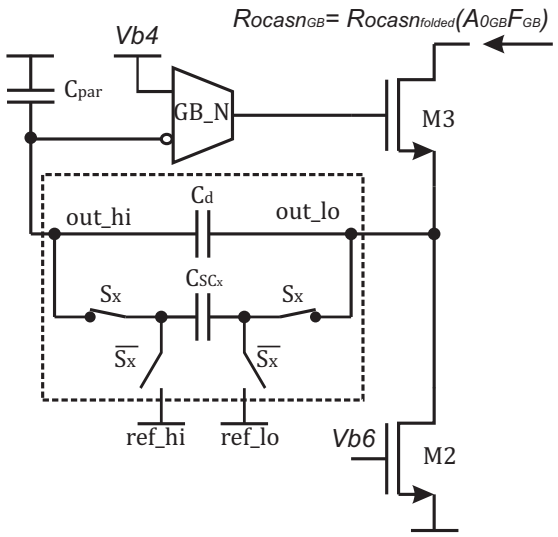


Figure 5.8: The half circuit model of the N-type gain boosted cascode for determining the feedback factor F_{GB} (5.16).

$$F_{GB} = \frac{C_{sc_x} + C_d}{C_{sc_x} + C_d + C_{par}} \tag{5.16}$$

The gain boosted amplifiers from Fig. 5.5 have an open loop gain which is given as $A_{0_{GB}}$. However, when the SC level shifter is used, then the effective gain of the gain

boosting amplifier is reduced by the feedback factor.

$$A_{0_{eff}} = A_{0_{GB}} F_{GB} \tag{5.17}$$

The reduction in the gain booster's open loop gain results in a reduction of the total amplifier gain to (5.18).

$$A_{total} = A_{folded}(A_{0_{GB}} F_{GB}) \tag{5.18}$$

C_{par} from Fig. 5.8 is dominated by the gain booster's input gate capacitance, and even in the extreme case where $C_{par} = C_{sc_x} + C_d$, $F_{GB} = \frac{1}{2}$, which results in only a 6 dB reduction in the effective open loop gain. When the SC network of Fig. 5.8 is designed so that (5.19) is true, then the feedback factor's impact on the overall system gain can be minimized.

$$C_{par} \ll C_{sc_x} + C_d \tag{5.19}$$

5.3.2 Gain Booster Network Transient Response

The SC level shifter in Fig. 5.7 uses a deglitch capacitor C_d to ensure that the gain booster's input gate is never floating, and it uses non-overlapping clocks to charge the deglitch capacitor up to $V_{C_d} = ref_{hi} - ref_{lo}$. The symmetric dual S_0-C_{sc_1}-$\bar{S}_1$ (and S_1-C_{sc_2}-$\bar{S}_0$) networks (Fig. 5.7) are SC resistors which supply charge to C_d twice every SC clock period T_{sc}, and the whole network acts as a switched capacitor RC low pass filter with an RC time constant τ (5.20). From (5.20), $C_d + C_{cs}$ can be sized to meet the system's startup time requirements.

$$\tau = \frac{C_d}{C_{sc}} \frac{T_{sc}}{2} \tag{5.20}$$

After the system's capacitors have been sized according to (5.16), (5.19), and (5.20), then the switches can be sized so that their static on resistance is small enough that the poles which they introduce are at a high enough frequency not to interfere with the normal operation of the amplifier.

5.3.3 Gain Boosted Network Noise Current

The noise current of the gain boosted cascode can be analyzed using Fig. 5.9 which is labeled with the input referred noise voltages of the different devices. The input referred noise voltages of M1 and M5 are $4kT\frac{\gamma}{gm}$, but the input noise voltage on M4 is the summation of its own $4kT\frac{\gamma_4}{gm_4}$ noise plus GB_P's output noise voltage (5.21).

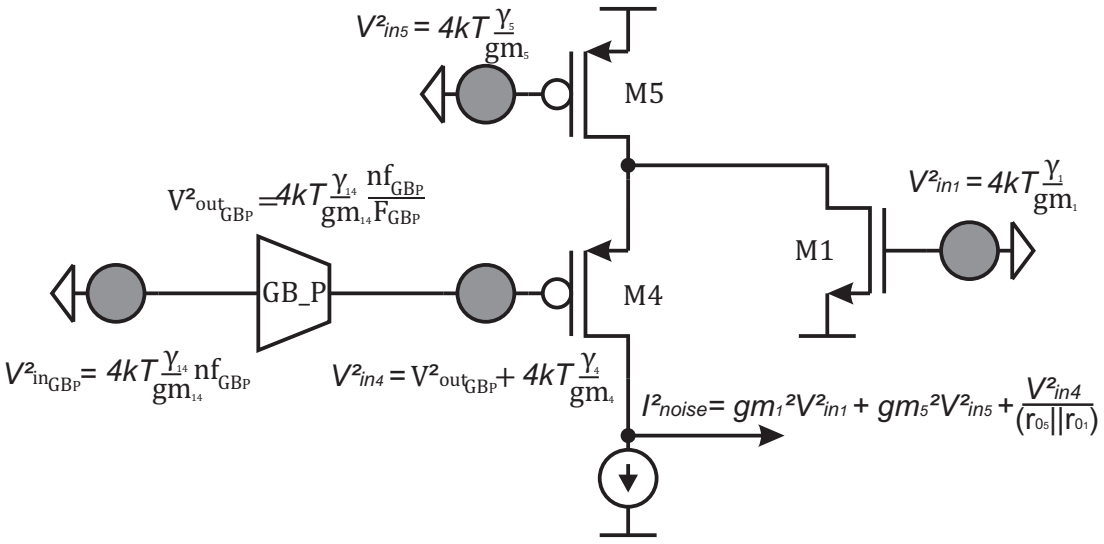


Figure 5.9: The gain boosted cascode half circuit.

$$
\begin{aligned}
V_{in_4}^2 &= 4kT\frac{\gamma_4}{gm_4} + 4kT\frac{\gamma_{14}}{gm_{14}}\frac{nf_{GB_P}}{F_{GB_P}} \\
V_{in_4}^2 &= 4kT\frac{\gamma_4}{gm_4}\left(1 + \frac{gm_4}{\gamma_4}\frac{\gamma_{14}}{gm_{14}}\frac{nf_{GB_P}}{F_{GB_P}}\right)
\end{aligned}
\tag{5.21}
$$

To get the noise current from M4, consider that M4 acts as a source follower, and because its I_d is set by M5, then V_{gs_4} must remain constant. If V_{gs_4} is constant, then M4's source voltage is equal M4's input referred noise voltage, which means that the output noise current from M4 is its input referred noise voltage divided by the parallel combination of M1 and M5's load resistances (5.22). Summing M1, M5, and M4's noise currents gives the total noise current for the P-side of the gain boosted folded cascode

amplifier (5.23).

$$I_{out_4}^2 = \frac{V_{in_4}^2}{(r_{0_1}||r_{0_5})^2} \tag{5.22}$$

$$I_{out}^2 = 4kT(\gamma_1 gm_1 + \gamma_5 gm_5) + \frac{V_{in_4}^2}{(r_{0_1}||r_{0_5})^2} \tag{5.23}$$

Substituting (5.21) into (5.23), and dividing by the square of gm_1, will give the total gain boosted folded cascode input referred noise voltage (5.24).

$$V_{in}^2 = 4kT\frac{\gamma_1}{gm_1}\left(1 + \frac{\gamma_5 gm_5}{\gamma_1 gm_1} + \frac{\gamma_4}{\gamma_1}\frac{\left(1 + \frac{\gamma_{14}}{\gamma_4}\frac{gm_4}{gm_{14}}\frac{nf_{GB_P}}{F_{GB_P}}\right)}{gm_1 gm_4 (r_{0_1}||r_{0_5})^2}\right) \tag{5.24}$$

From (5.24), the term $gm_1 gm_4 (r_{0_1}||r_{0_5})^2$ is roughly one fourth of the transistor's intrinsic gmr_0 gain squared. Even in the extreme case where the $\gamma_{14} gm_4 nf_{GB_P}/\gamma_4 gm_{14} F_{GB_P}$ ratio is very poorly proportioned, $gm_1 gm_4 (r_{0_1}||r_{0_5})^2$ should still be large enough to make (5.25) true, thereby minimizing the impact of the cascode noise current source (5.26).

$$1 + \frac{\gamma_5 gm_5}{\gamma_1 gm_1} \gg \frac{\gamma_4}{\gamma_1}\frac{\left(1 + \frac{\gamma_{14}}{\gamma_4}\frac{gm_4}{gm_{14}}\frac{nf_{GB_P}}{F_{GB_P}}\right)}{gm_1 gm_4 (r_{0_1}||r_{0_5})^2} \tag{5.25}$$

$$V_{in_{noise}}^2 \approx 4kT\frac{\gamma_1}{gm_1}\left(1 + \frac{\gamma_5 gm_5}{\gamma_1 gm_1}\right) \tag{5.26}$$

5.4 Switched Capacitor Networks

To help reduce the system's current consumption, switched capacitor networks are used to generate the system's dynamic bias voltages V_{cmfb} and $V_{float_{pn}}$. The SC level shifter in Fig. 5.10 generates the DC offset which biases M6's gate to a potential which ensures that the amplifier M1 remains in saturation, and the SC CMFB block generates the common mode feedback voltage V_{cmfb}

Fully differential amplifiers require a defined output common mode voltage, and the circuit from Fig. 5.11 is used to generate the V_{cmfb} bias voltage. The circuit operates by storing $(V_{ocm} - V_{bias})$ across the C_{sc_x} capacitors, and then connecting the C_{sc_x} capacitors differentially to the amplifier output nodes with the middle node V_{cmfb} applying the corrective feedback voltage to the common mode feedback transistor [17].

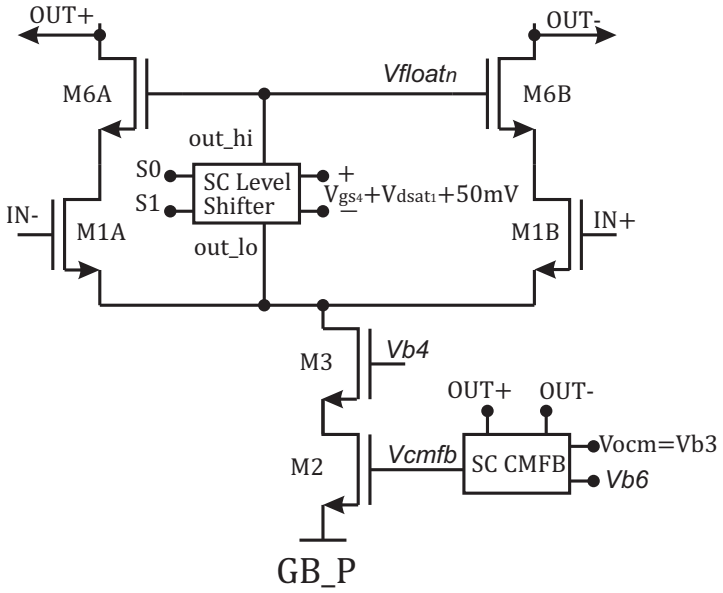


Figure 5.10: The SC level shifter is used to generate the floating cascode gate bias of the telescopic gain boosting cascodes.

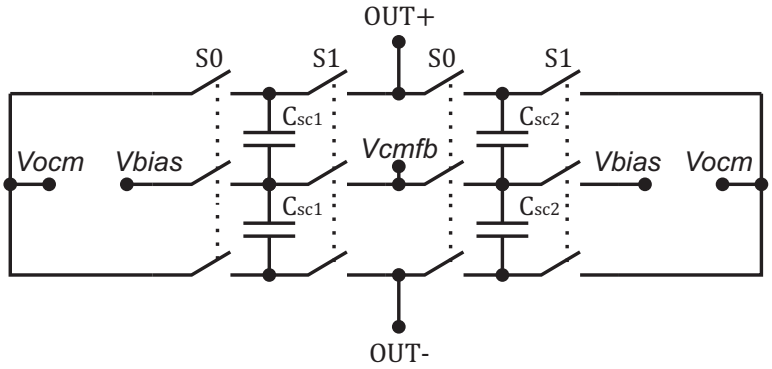


Figure 5.11: The SC common mode feedback voltage generator.

5.5 Gain Boosted Amplifier Design Verification

The system has been designed to measure absolute pressure with the Protron-Mikrotechnik capacitive absolute pressure sensor using a 1.2 VDC stimulation voltage at the human body temperature of 38°C. Table 5.1 lists the design constants such as the range and resolution requirements, the Protron Mikrotechnik sensor parameters, supply voltage, and parasitics capacitance of the bondpad. The sensor has nominal capacitance $C_0 = 6.0$pF at the absolute pressure of 1.1 atm, and a pressure sensitivity of $1.58\frac{pF}{atm}$ [3].

Table 5.1: Pressure sensor system design constants.

Parameter	Value
Temperature	38°C
ADC S/H Cap C_l	4.6 pF
Pressure Range	760mmHg
Resolution	0.75mmHg
Number of ADC bits	10
C_0	6.0 pF
Sensitivity	1.6pF/760mmHg
V_{stim}	1.2 VDC
$V_{out_{pp}}$	2.4 V
$C_{bondpad}$	5.5 pF

With the system design constants from Table 5.1, the previously derived system design equations, repeated here for convenience, can be used to calculate the various system parameters and total allowed noise which will be used later for the amplifier device sizing. Table 5.2 lists the values for C_f and ϵ_{total} based on the pressure read range and desired ADC resolution.

Table 5.2: Pressure sensor system C_f and noise.

Parameter	Eq.	Value
$C_{s_{\text{pp}}}$	(5.27)	1.6 pF
C_f	(5.28)	800 fF
ϵ_{total}	(5.29)	1.172 mV

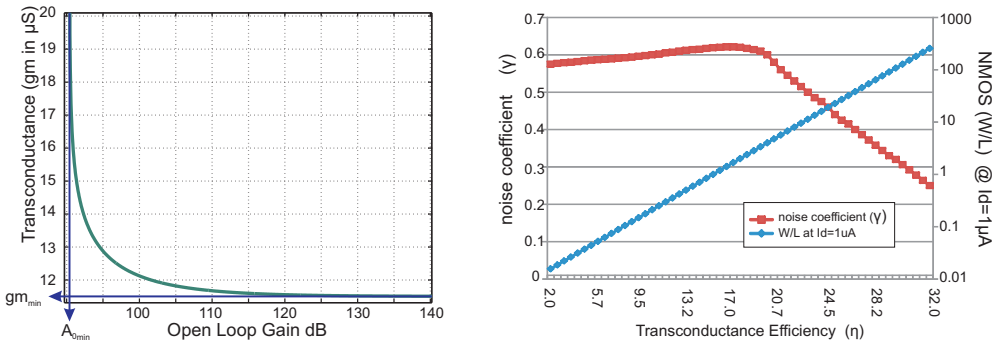
$$C_{s_{\text{pp}}} = \text{Sensor Sensitivity times Read Range} \tag{5.27}$$

$$C_f \approx \frac{C_{s_{\text{pp}}}}{2} \tag{5.28}$$

$$\epsilon_{total}^2 = \frac{V_{signal_{rms}}^2}{10^{\frac{6.02*N+1.76}{10}}} \tag{5.29}$$

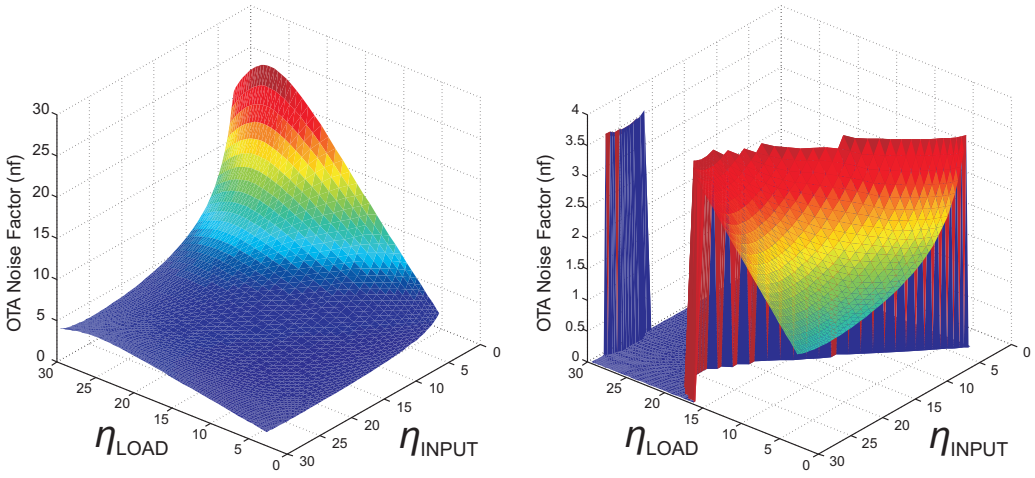
At this point, all of the system design constants have been declared. The remaining tasks are:

1. From the total allowable error, give some of the available error to noise, and some of the error to settling using the factor SNR_{extra} (5.34)
2. Calculate the maximum allowable nf based on the ϵ^2_{noise} and C_{leff} (5.38).
   - If a realistic nf is not achievable with the given ADC sample and hold capacitance, it may be necessary to add more C_{poly} or C_l to reduce the system noise.
3. Generate a 3D plot using the device data from Fig. 5.12b and solving for (5.39) Fig. 5.13a.
4. Limit the plot output to show only results that are less than the maximum allowed nf, Fig. 5.13b.
5. Choose values for η_{gm_1} and η_{load} which will give a good compromise of wide output swing and input device transconductance efficiency η_{gm_1}.
6. Plot gm as a function of A_0 (5.40) Fig. 5.12a, and select a good compromise of values for gm and A_0.
7. Calculate the required bias current (5.41) from the selected gm value.
8. With Fig. 5.12b, use the data as a lookup table to size all of the amplifier's W/L ratios according to their η_{gm} value and the amount of bias current they are conducting (Table 5.5).
9. Verify that the gain of the amplifier meets the required A_0 for the settling accuracy, and increase, or decrease, the channel lengths as necessary.



(a) (b)

Figure 5.12: Simulation data for choosing gm, A_0, and the W/L ratios.
a) Plot of the solution for gm vs. A_0 (5.40).
b) Spectre simulation plotting the noise coefficient γ and the N-type MOSFET W/L ratio as a function of the η_{gm} value.



(a) (b)

Figure 5.13: Plots for choosing the η_{gm} values to meet the nf requirement.
a) The 3D surface plot of the data points from Fig. 5.12b which solve (5.38).
b) The 3D surface plot only plotting the points which meet the nf requirement from (5.39).

$$A_{\mathrm{cl}} = \frac{2C_0}{C_f} \tag{5.30}$$

$$C_{eq} = \frac{C_{eq_a} C_{eq_b}}{C_{eq_a} + C_{eq_b}} + C_{\mathrm{poly}} \tag{5.31}$$

$$F = \frac{C_f}{C_f + 2\left(\frac{(2C_0+C_{par1})(2C_0+C_{par2})}{(2C_0+C_{par1})+(2C_0+C_{par2})}\right)} \tag{5.32}$$

$$C_l = C_{leff} - \frac{C_f}{2}(1-F) \tag{5.33}$$

$$\epsilon^2_{noise} = \frac{V^2_{signal_{rms}}}{10^{\frac{6.02*N+1.76+SNR_{extra}}{10}}} \tag{5.34}$$

$$noise\ fraction = 10^{-\left(\frac{SNR_{extra}}{10}\right)} \tag{5.35}$$

$$\epsilon_{settling} = \epsilon_{total_{pp}}\left(1 - 10^{-\left(\frac{SNR_{extra}}{10}\right)}\right) \tag{5.36}$$

$$C_{leff} = \frac{kT\gamma_{in}\, nf\, C_{eq}F}{\epsilon^2_{noise}F^2\, C_{eq} - kT\gamma_1 nf} \tag{5.37}$$

$$nf = \frac{\epsilon^2_{noise}F}{kT\gamma_1\left(\frac{1}{C_{eq}F} + \frac{1}{C_{leff}}\right)} \tag{5.38}$$

$$nf = 1 + 3\left(\frac{\gamma_{load}\eta_{gm_{load}}}{\gamma_1\eta_{gm_1}}\right) \tag{5.39}$$

$$gm_1 = -\frac{4\, C_{leff} f_{sc}}{F}\ln\left(\epsilon_{settling} - \frac{1}{A_0\, F}\right) \tag{5.40}$$

$$I_{d_{\mathrm{M1}}} = \frac{gm_1}{\eta gm_1} \tag{5.41}$$

$$GBW = \frac{gm_1}{2\pi 2C_{leff}} \tag{5.42}$$

5.5.1 Amplifier Design Verification

Three different designs have been created with the Cadence Design Framework using the UMC 130nm technology, and the design variables are listed in Table 5.3. The amplifiers are designed using Cadence Design Framework II, and simulated with Spectre circuit simulator. DC simulations are used to fine tune the transistor dimensions until they have the desired η_{gm} values. Then, two different analyses, the AC and the pss/pnoise analyses, are performed on each of the three amplifiers. The ac analysis is used to find the amplifier's gain bandwidth product, and the pss/pnoise is used to verify the $V^2_{noise_{rms}}$ of the circuit.

Table 5.3: CDS system design values.

f_{sc}		4ksps	40ksps	400ksps
C_{gs}		100fF	500fF	1.5pF
C_{eq}	(5.31)	7.58pF	7.79pF	8.3pF
F	(5.32)	$0.053\frac{V}{V}$	$0.0515\frac{V}{V}$	$0.0483\frac{V}{V}$
C_{leff}	(5.33)	4.98pF	4.98pF	4.99pF
SNR_{extra}	(5.34)	2.2 dB	2.1dB	2.1dB
ϵ_{noise}	(5.34)	522 μV	529μV	529 μV
$\epsilon_{settling}$	(5.36)	452 μV	436μV	420u μV
nf_{max}	(5.38)	3.62	3.60	2.69
gm_{min}	(5.40)	11.6 μS	120 μS	1.282 mS
$A_{0_{min}}$	(5.40)	92.4dB	93.0dB	98.9dB
$\eta_{gm_{in}}$	Fig. 5.13b	28	28	25
γ_{in}	Fig. 5.12b	0.35	0.35	0.45
$\eta_{gm_{load}}$	Fig. 5.13b	14	14	14
γ_{load}	Fig. 5.12b	0.6	0.6	0.6
A_0	Fig. 5.12a	102dB	102dB	102dB
gm	Fig. 5.12a	12.3μS	126 μS	1.364mS
I_d	(5.41)	440 nA	4.29 μA	48.8 μA

The three amplifiers were simulated using the exact device η_{gm} and I_d values listed in Table 5.3 without any further optimizations, and the pss/pnoise simulation were performed as per the guidelines documented in [9]. The result of the simulations verify the validity of this design methodology over 3 decades of sample frequency. The noise

simulation results listed in Table 5.4 show a very high degree of correlation between what the calculated bandwidth and noise voltage should be, and what the simulated bandwidth and noise should be.

Table 5.4: Spectre noise analysis simulation results.

f_{sc}		4 kHz	40 kHz	400 kHz
GBW	(5.42)	196 kHz	2.013MHz	21.79 MHz
GBW	simulation	212.5 kHz	2.086 MHz	22.32 MHz
$\epsilon_{noise_{rms}}$	(5.34)	522 μV_{rms}	529 μV_{rms}	529 μV_{rms}
$V^2_{noise_{rms}}$	simulation	487 μV_{rms}	507 μV_{rms}	547 μV_{rms}

5.6 Final Amplifier Design

For this system, the medical implant design specifications require an amplifier with a thermal noise factor nf less than or equal to 3.6. The amplifier will have a feedback factor of $F = \frac{1}{20}$, and it will be driving a differential effective load capacitance C_{leff} of 5pF. The amplifier has dynamic settling requirements of $\epsilon = 0.025\%$ and $t_s = 125\mu s$, and the static settling requires a DC gain greater than 102 dB over an output voltage swing of ±850mV.

The 4 kHz column from Table 5.3 lists the values which are used for designing this system's amplifier with only one slight adjustment. Instead of 440nA bias current, the bias current has been overdesigned up to 480nA. This was done for peace of mind that the system will meet the noise requirements.

Table 5.5 lists the η_{gm} values which have been chosen for the each of the design's MOSFET devices, the device drain current, and the required W/L ratios as given by Fig. 5.12b.

The amplifier is a switched capacitor design performing correlated double sampling for $1/f$ noise rejection. The switching period is $125\mu s$ for each half cycle, so the switching frequency is (5.43).

$$f_{sc} = \frac{1}{2 * 125\mu s} = 4kHz \tag{5.43}$$

The amplifier's low frequency noise rejection has a high pass cutoff frequency of (5.44) [10]. It is important that the $1/f$ noise corner occurs at a lower frequency than (5.44) to en-

Table 5.5: Device transistor η_{gm} values, the device drain current, and the device $\frac{W}{L}$ values normalized to the device current.

Transistor	Type	η_{gm}	I_d	$\frac{W}{L}\frac{I_d}{1\mu A}$
M1	N-type	28 V^{-1}	480nA	8.0
M2	N-type	14 V^{-1}	480nA	0.15
M3	N-type	25 V^{-1}	480nA	2.0
M4	P-type	22 V^{-1}	480nA	4.5
M5	P-type	14 V^{-1}	960nA	0.75
M6	N-type	14 V^{-1}	40nA	0.0125
M7	N-type	25 V^{-1}	40nA	0.17
M8	P-type	22 V^{-1}	40nA	0.38
M9	P-type	28 V^{-1}	40nA	7.2
M10	P-type	22 V^{-1}	40nA	0.38
M11	P-type	14 V^{-1}	40nA	0.06
M12	N-type	14 V^{-1}	40nA	0.0125
M13	N-type	25 V^{-1}	40nA	0.17
M14	N-type	28 V^{-1}	40nA	0.67
M15	N-type	25 V^{-1}	40nA	0.17
M16	P-type	22 V^{-1}	40nA	0.38
M17	P-type	14 V^{-1}	40nA	0.06
M18	N-type	14 V^{-1}	80nA	0.025
M19	N-type	25 V^{-1}	80nA	0.34
M20	P-type	22 V^{-1}	80nA	0.76
M21	P-type	14 V^{-1}	80nA	0.12

sure proper flicker noise rejection. The bandwidth of the amplifier, as determined by its effective impedance and its transconductance, is (5.45).

$$f_1 = 0.3 f_{sc} = 1.2 kHz \tag{5.44}$$

$$f_2 = \frac{gm_1 F}{2\pi C_{leff}} \approx 10.5\ kHz \tag{5.45}$$

$$f_1 \frac{2}{\pi} < NEB < f_2\ \frac{\pi}{2} \tag{5.46}$$

Each device of the gain boosted amplifier has been sized to fit the $\frac{W}{L}$ ratios given in Table 5.5. Starting with a 500nm channel length, while maintaining constant η_{gm}

values, the channel lengths are increased until the OTA gain is greater than 102 dB over the ±850mV output voltage swing, Fig 5.16. One the gain has been achieved, if the flicker noise corner of the amplifier is still greater than the allowed cutoff frequency, then the input device and load area can be scaled even further until the $1/f$ noise corner is low enough to be rejected by the correlated double sample action of the switched cap design.

5.7 Simulation Results

The amplifier has been designed to meet the settling time and bandwidth requirements set forth by the medical implant. The schematics are assembled using Cadence Design Framework II, and Spectre simulations are used to verify its small and large signal performance. The gain boosted folded cascode amplifier is simulated using the test schematic from Fig. 5.14, which has an effective differential output impedance of 5 pF, and a feedfack factor of $\frac{1}{20}$.

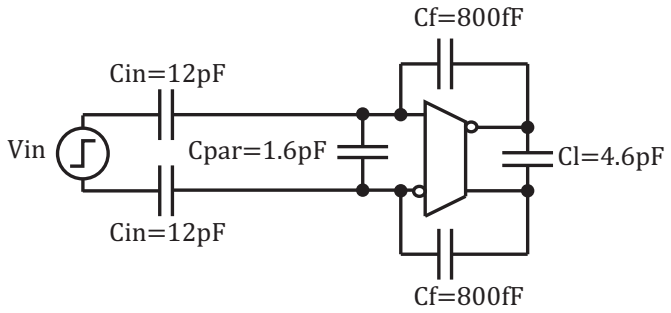


Figure 5.14: The test schematic used to perform simulations on the boosted folded cascode amplifier.

The AC simulations in Fig. 5.15 show that the amplifier has an open loop DC gain of a little more than 150 dB, and the closed loop 3 dB cut off frequency is a little bit more than 10 kHz as calculated by (5.45).

Fig. 5.16 gives the open loop DC gain over the amplifier's output voltage range. The plot shows that over the required ±850mV output voltage swing, the amplifier can deliver $>$ 114dB of open loop DC gain.

Fig. 5.17 shows the step response of the amplifier under load and no load conditions. Considering stability, there is no ringing present in the non loaded response. In regards

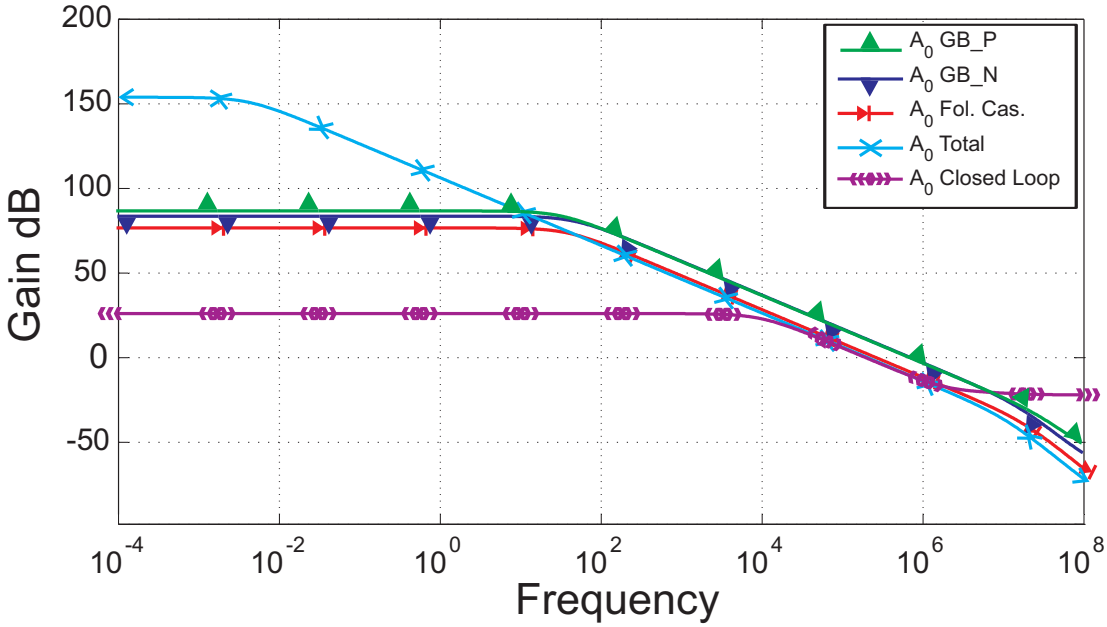


Figure 5.15: Spectre AC sweep simulation results that shows that the total output gain is roughly the product of the folded cascode amplifier open loop gain, and the average open loop gain of the two gain boosting amplifiers as predicted by (5.12).

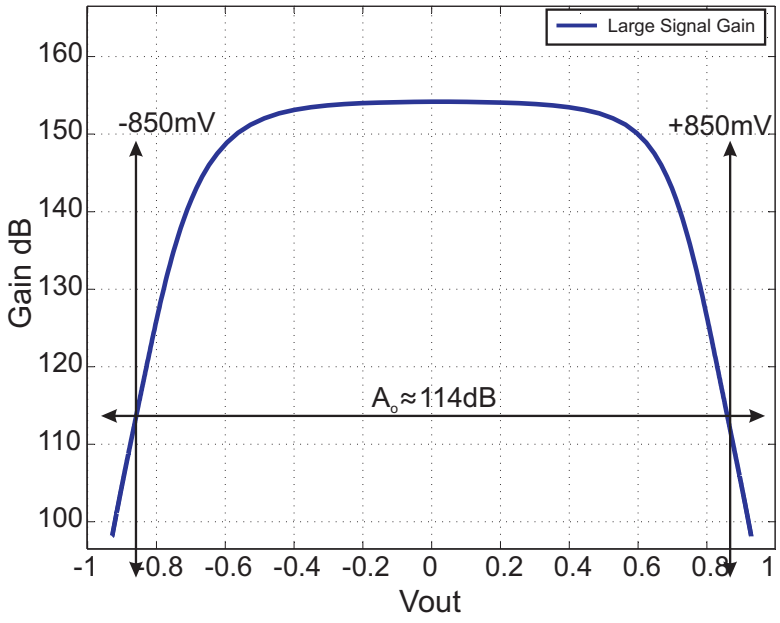


Figure 5.16: Spectre DC sweep simulation results showing the large signal DC gain over the whole output voltage swing.

to the accuracy and settling time, the step response verifies that the amplifier settles to the required output voltage in the $125\mu s$ of time which it is given to settle.

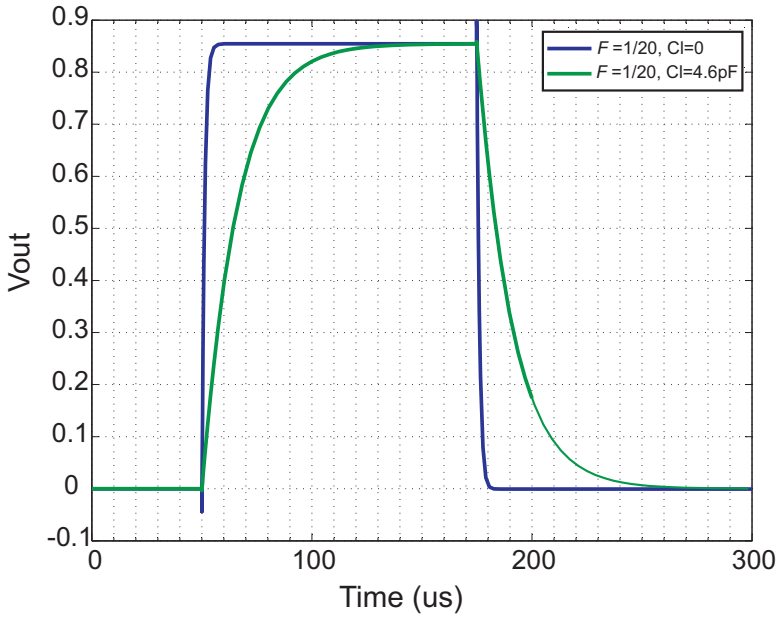


Figure 5.17: Spectre AC simulation showing the amplifier's step response for a load and no load configuration.

6

Analog to Digital Signal Conversion

For this design, a lot of attention has been given to the noise analysis of the active electronics, but noise is not the only source of pressure measurement error. Even in low power designs, as the system clock switches gates of the digital section of a mixed signal design, several millivolts to tens of millivolts of ripple voltage interference from the other device electronics can be injected onto the sensitive analog electronics. If this interference is not handled, it can have a devastating effect on a 10 bit ADC operating with a 1.2 VDC supply where each LSB is only a couple of millivolts of resolution. This unwanted interference is present everywhere inside the chip, and this brings about two conditions; there is nowhere on the chip that this switching interference will not be present, and because this interference is everywhere, its effect is generally common mode to the surrounding electronics.

It could be very costly, in terms of power and area, to try to totally eliminate these effects. However, the common mode nature of the interference can be exploited to design a system which is relatively unaffected by the interference. The active electronics of the signal conditioning chain have already been designed using a fully differential architecture, so the task is to construct an ADC which is also fully differential. The ADC architecture which was used for this design is heavily based on the ADC design from [18], and it is a fully differential architecture from input to output.

Section 6.1 will describe the design of the ADC charge redistribution capacitor array, and the unit cell capacitors which make up the binary weighted capacitor array. This section will describe how the unit cell capacitor has been designed to reduce the effects of EM interference and bottom plate capacitance [19], and Section 6.2 will describe how

the unit cell's physical size has been selected to minimize mismatch error. Section 6.3 will describe the operation of the ADC. The ADC's capacitive charge redistribution blocks will be described, and the method which the charge is redistributed from from one capacitor stage to the next is explained. Section 6.4 will describe the comparator block and the method which is used to perform the comparator input offset cancellation.

6.1 ADC Unit Cell Capacitor

To achieve good matching between different array capacitors, a unit capacitor is used to generate each of the ADC capacitors. The idea is to create the larger capacitors of the array with multiples of the smaller capacitors in an attempt to promote better accuracy in creating capacitors which are integer multiples of each other. The 130nm CMOS process used to fabricate this integrated circuit has 8 layers of metal available, and the ADC's unit capacitor cell uses 5 of these metal layers in its construction. A metal-oxide-metal capacitor, or a MOM-cap, behaves like a vertical plate capacitor [20], and the custom designed MOM-cap unit capacitor has been built specifically for this fully differential ADC architecture with the purpose of ensuring good matching while also helping to reduce the overall ADC area requirements. The minimum sized capacitor is made up of 4 unit cells so that they can be evenly placed into 4 quadrants using common centroid layout techniques. The unit cell in Figs. 6.1a and 6.1b is a custom designed MOM cap which has been wrapped in a Faraday cage placed symmetrically around the MOM-cap plates.

The purpose for the shielding around the unit cell capacitor plates is not to eliminate the bottom plate parasitic capacitance, but to incorporate the parasitics as part of the unit cell. The parasitic capacitance from the MOM cap plates to ground helps to prevent the plate potentials from floating beyond the power supply potentials. Also, because the parasitics are equal for both the top and the bottom plates, and from one unit cell to the other, then the parasitic capacitance presents itself as simply a little extra differential capacitance. The shielding around the MOM cap plates protects the unit cell capacitors from external interference. With the shielding in place, it is very easy to place the charge sharing and comparator electronics beneath the array of capacitors Fig. 6.2 without interfering with the ADC charge distribution array.

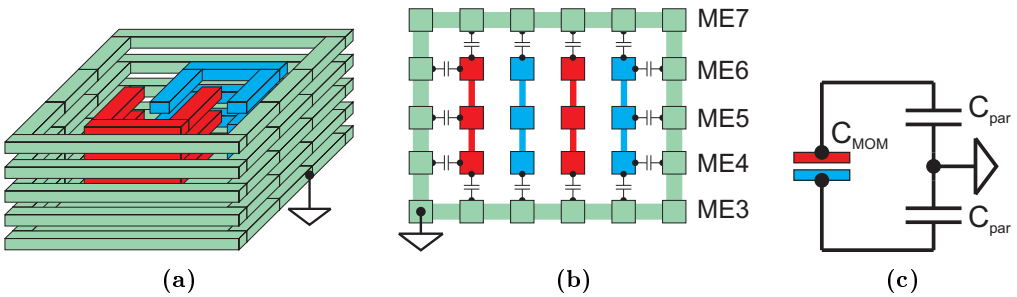


Figure 6.1: The fully differential ADC unit cell capacitor.
a) The unit capacitive MOM-cap surrounded in a Faraday cage for noise immunity (the top shield layer is removed for display).
b) The unit cell cross section showing how the parasitic bottom plate capacitance is simply just a little added differential capacitance.
c) The unit cell equivalent circuit.

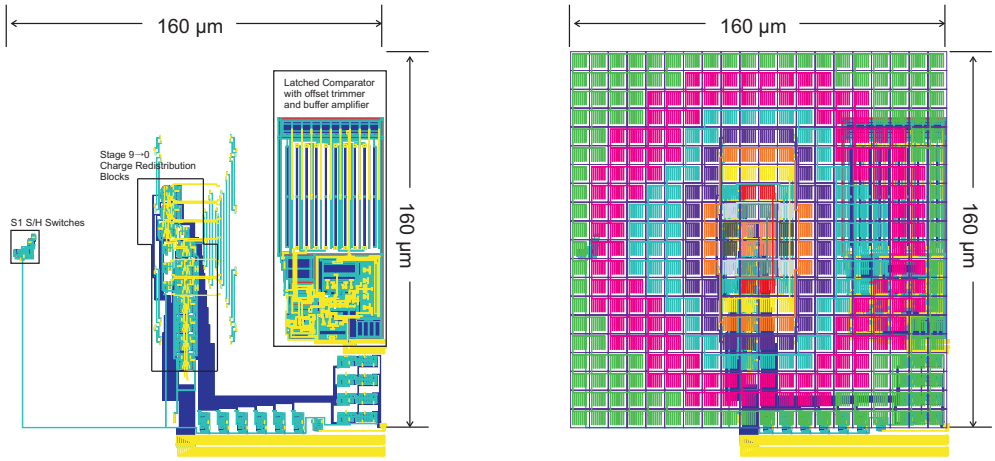


Figure 6.2: The complete layout of the ADC showing how the active electronics are placed underneath the ADC capacitor array.

6.2 ADC Unit Cell Mismatch

In analog CMOS design, there are different types of device mismatch variation. Some of the types of variation are lot to lot, wafer to wafer, and chip to chip, and these process variations come mostly from variations in metal layer and the oxide layer thicknesses. For the MOM caps which are located in the metalization layers, the variance in layer thicknesses are a direct result of the CMOS chip planarization chemical mechanical polishing process (CMP) [11], and as such can be considered to be constant on scales

within the area limits of the IC. These process variations which occur on a chip to chip scale or larger are not so detrimental for the ADC design because the ADC conversion process is performed by distributing charge between an array of capacitors which are simply integer ratios of each other. As long as the thickness variation is equally applied to all of the capacitors of the array, then precise capacitance ratios will be maintained.

The other source of mismatch is the on chip mismatch from one device to the other. The Pelgrom mismatch model, 6.1 [21], even though it was developed to describe the variation of MOSFET mismatch, can be used to gain an understanding of the mismatch characteristics of the MOM cap. The main idea behind the Pelgrom model is that the random mismatch is reduced as the devices are made larger, and increased as the separation distance is increased.

$$\frac{\sigma^2(\beta)}{\beta^2} \approx \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{6.1}$$

In (6.1), σ^2 is the variance of the capacitive mismatch between two capacitors, and β can be equated as the capacitance per feature size. On the right hand side, WL is the width and length capacitor area, D is the distance between the capacitors, and A_β^2 and S_β^2 are the process related mismatch constants which are measured by the chip foundry for the particular CMOS technology. According to 6.1, the general method for reducing the random mismatch is to increase the device area and to reduce the separation distance.

6.2.1 ADC Unit Cell Distance Mismatch

The variance caused by separation, is, to the first order, caused by linear gradients during any of the applied processing steps. These gradients can come from several sources such as pressure, temperature, or planarization effects to name just a few. One method for handling linear mismatch to is split each ADC unit capacitor into four unit cells, and to lay the capacitors out in a common centroid arrangement. The ADC's charge redistribution capacitor array is shown in Fig. 6.3. The common centroid configuration puts the physical center of each capacitor in the same location, which means that, to the first order, the distance mismatch effects are theoretically reduced to zero.

The innermost groupings of the capacitors in Fig. 6.3 belong to the least significant bits, getting progressively more significant towards the outer rings. The outermost ring

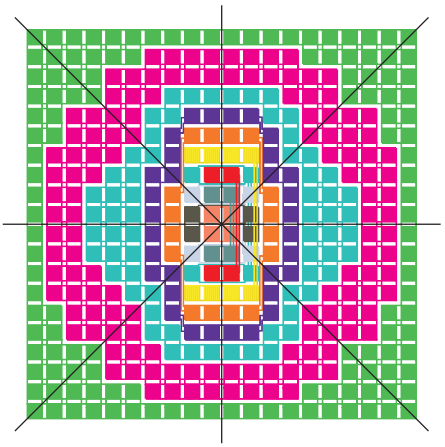


Figure 6.3: The common centroid layout of the ADC capacitor array with an outer ring of dummy cell capacitors. Each color corresponds to one capacitor from the ADC capacitor array, and each capacitor has equal capacitance in each of the four quadrants of the array.

in Fig. 6.3 is not part of the charge redistribution array. Its function is to reduce the device mismatch which can be caused by the chemical mechanical polishing when the metal density on one side of a critical device is not the same as the metal density on the other side of the device (Fig. 6.4). Placing the non-critical metal structures around the capacitor array helps to avoid this source of mismatch, and the added capacitors themselves can be used for improved AC decoupling.

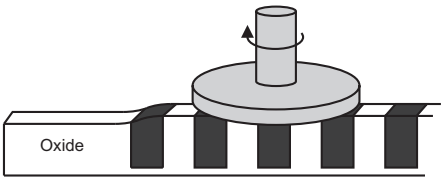


Figure 6.4: Different metal/oxide density ratios can cause thickness gradients during the CMP process.

6.2.2 ADC Unit Cell Mismatch from Device Area

Because the unit cells are custom made for this project, it would be possible to save chip area by making them as small as possible, but, according to (6.1), this would increase the random mismatch cause by the smaller device area. This random mismatch can come from several different sources. Every system has some amount of random noise, and because the manufacturing process is performed using several different electrical

and mechanical systems, there is randomness in the final manufactured product. The result is that the finished product does not look exactly as it looked on the computer screen in the CAD design program. In the layout environment, the various structures are displayed on the computer screen with nice straight edges and 90° corners, but what actually gets manufactured are structures with some degree of random edge roughness like in Fig. 6.5.

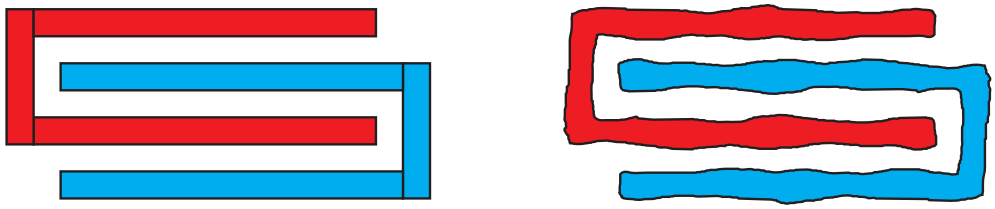


Figure 6.5: Comparison of the appearance of the MOM cap fingers in the layout environment with nice straight edges and 90° corners, and what they look like after fabrication with random edge roughness.

This edge roughness causes a random deviation in the capacitor electrode plate separation which in turns causes a random deviation in the capacitance per unit area. This random deviation in the capacitance is a real problem for the SAR ADC because the accuracy of the conversion is dependent on the accuracy of the capacitor ratios. Increasing the length of the MOM cap fingers, which is in essence the act of increasing the capacitor size, will act to average out the edge roughness thereby decreasing the random variation from one capacitor to the next. If the unit cells are made large enough, then the variance caused by the edge roughness will be reduced to a value less than the dynamic range of the ADC.

To determine how large the capacitor needs to be, it would usually be possible to run a Monte Carlo mismatch analysis on the capacitor, and the designer could choose the unit cell capacitor which results in an array mismatch standard deviation to array capacitance less than 1/2 LSB. The manufacturing foundry provides Monte Carlo simulation model files for the devices which are available for their standard library. Unfortunately, the capacitor used in this ADC is a custom made cell, and the foundry's model file is not designed for a MOM cap which has fingers only on metal layers M4 through M6. Luckily, it is possible to take the foundry's Monte Carlo model file, decompose it into the information which is relevant for the individual metal layers, and to plot the mismatch information for only the metal layers which are in use.

The Spectre Monte Carlo model file is simply a series of functions which take a few design variables such as MOM cap finger length, number of fingers, and a few different process related constants, and returns a capacitance which is the sum of the ideal capacitor plus the mismatch capacitance. Monte Carlo simulations of complex circuits are handled well in the Cadence environment, but the Monte Carlo analysis of a single unit cell capacitor is a very simple analysis, and the overhead of a complete simulation in Cadence can cost a lot of time. The amount of time per simulation might only be 1 or 2 seconds, but a good Monte Carlo analysis might need several hundred to several thousand runs to generate an accurate Gaussian distribution. Performing this analysis with a technical computing software package can save an enormous amount of time compared to performing the analysis in a Cadence environment.

One such technical computing software package is Matlab, and, because the Spectre file is just a series of formulas written in script language, it is fairly trivial to adapt the Spectre model file to a Matlab M-file. Matlab has several built in functions which allows it to perform Gaussian distribution analyses on a set of functions with very little overhead. In Cadence, the simulator will run a full simulation on the circuit for each Gaussian distributed mismatched capacitance value, and only when all of the simulations are complete does the designer have access to the simulation results and the list of mismatched capacitors. For the purpose of determining the standard deviation of the capacitance cell mismatch, the only information necessary is the Gaussian distributed list of mismatched capacitors making all of the time spent performing the full schematic analysis unnecessary.

Table 6.1 shows a comparison of the time spent in Matlab versus Cadence for finding the standard deviation of the mismatched capacitor values. The Cadence Monte Carlo simulation takes about 3 hours to run one 10,000 point normal distribution simulation on 1 capacitor (roughly 1 simulation per second). On the other hand, Matlab can create a 50,000 point Gaussian distribution, and run that 50,000 point simulation on 2,500 different cells (equivalent to running 125,000,000 Cadence simulations) in about 30 seconds.

6.2.3 Sizing the ADC Unit Cell

The reason for wanting to characterize the mismatch distribution is to get an idea of how large the unit cell needs to be to reduce conversion error accuracy to an acceptable

Table 6.1: Monte Carlo vs. Matlab simulation comparison.

Simulation Environment	Number of cells simulated	Number of normally distributed points	Number of Simulations	Time to completion
Cadence	1	10,000	10,000	≈3 hours
Matlab	2500	50,000	125,000,000	≈30 sec.

level. There has been significant work investigating the ability to compensate for the mismatch between SAR ADC capacitors [22, 23, 24], usually using some form of post manufacturing capacitance trimming or using extra active electronics. But this work does not employ any post trimming or added electronics to ensure accuracy. Therefore, the unit cells must be sized large enough to ensure an acceptable yield of 10 bit ADC capacitor arrays. Equations (6.2) and (6.3) return the expected number of integral nonlinearity (INL) error bits and differential nonlinearity error bits [11] as a function of the number of cells times the ratio of standard mismatch deviation to individual cell size under worst case conditions where all of the cells with mismatch of one polarity belong to the S/H capacitor, and all of the cells with opposite polarity mismatch belong to the rest of the capacitor array.

$$INL_{\text{bits}} = 2^{(N-1)} \left(\frac{|\Delta C|_{\max}}{C_{\text{cell}}} \right) \tag{6.2}$$

$$DNL_{\text{bits}} = \left(2^{N} - 1\right) \left(\frac{|\Delta C|_{\max}}{C_{\text{cell}}} \right) \tag{6.3}$$

N is the number of ADC bits, $|\Delta C|_{\max}$ is the maximum deviation per unit cell, and C_{cell} is the nominal capacitance of the unit cell. If the value used for $|\Delta C|_{\max}$ in (6.2) and (6.3) is 3 times the standard deviation of mismatch, σ, then the calculated number of error bits would be valid for about 99% of the capacitor arrays.

To use the Spectre Monte Carlo file provided by the foundry to generate mismatch data, there are a couple of rules that needed to be followed. The function variables for calling the Monte Carlo file are the number of MOM-cap fingers, the length of each finger, and 1 single point from a random sample of points normally distributed with zero mean and standard deviation equal to 1. Based on the finger length and the number of fingers, the Monte Carlo file determines the capacitor's length, L, and width, W, with the requirement that each metal finger has a width of 200nm, and a finger to

finger separation of 200nm. This ADC's cell capacitor is designed to follow this sizing convention so that the results from the Monte Carlo analysis will be valid.

The Monte Carlo function is called with the number of fingers, the finger length, and a single point from a normal distribution of random points, and the function call returns a single capacitance value which is the ideal capacitance plus some value of Gaussian normal distributed mismatch. Calling the Monte Carlo function for all of the points of the random distribution results in a collection of randomly mismatched capacitors, which have a mean value equal to the ideal value, and a standard deviation, σ.

The plots in Fig. 6.6 solve (6.2) and (6.3) for the number of error bits versus the capacitor size. The lines which are plotted are the solutions for setting $|\Delta C|_{\max}$ equal to different levels of ADC mismatch standard deviation σ. As the plot shows, reducing the allowed $|\Delta C|_{\max}$ mismatch to ever smaller values of σ results in less and less error bits, but this comes with the cost of much reduced process yield. For $\sigma = 0.1$, under the worst case capacitor mismatch distribution, only about 8%, or 1 out of 12, of the manufactured capacitor arrays would have an INL<1 bit and a DNL<2 bits.

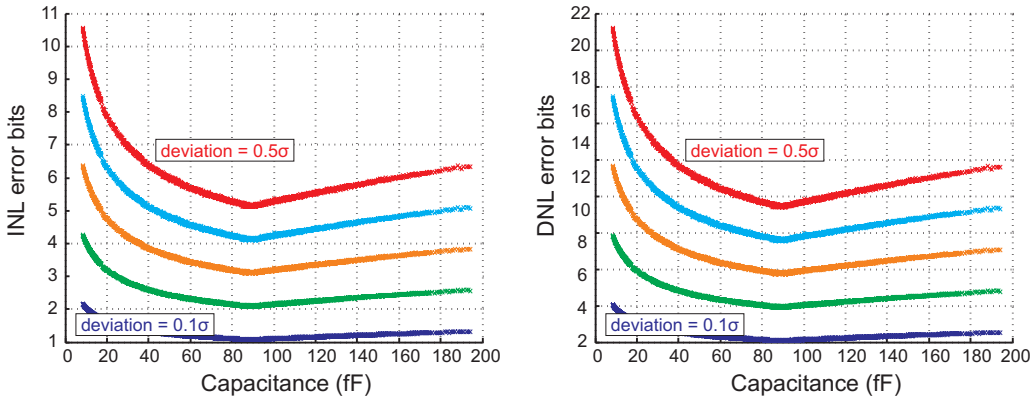


Figure 6.6: Matlab simulations of the Spectre Monte Carlo model file solving (6.2) and (6.3) with the mismatch value $|\Delta C|_{\max}$ being allowed progressively less deviation mismatch from the ideal mean capacitor value.

The plots in Fig. 6.6 shows that the accuracy increases with increasing capacitor size, until the increasing capacitor size starts to make the separation between the capacitors the dominating factor in the mismatch calculation. This behavior is in accordance with the Pelgrom mismatch model (6.1), but it does not take into account the common centroid layout method which was employed to reduce the distance mismatch effects.

Unfortunately, there is no variable in the Spectre Monte Carlo file which can be set to tell the simulator not to include the distance error in the mismatch calculation, so the error still shows itself in the simulation results (the part of the plot where the error bits start to increase despite the increasing capacitor size). The common centroid layout does help to reduce the effects of the distance related mismatch, and the design process has proceeded with the assumption that the mismatch error continues to reduce for at least a few more tens of femtofarads.

The plot in Fig. 6.6b show that only a very small percentage of the capacitor arrays from an entire process run would have less than one DNL bit of error, perhaps only devices which fall within 0.01σ of the ideal mean. A yield of just 1 chip out of 1000 is just too small, even for this medical implant where small size is considered more important than yield. So a method for decreasing the mismatch was implemented with the intention of not increasing the power consumption or the chip size.

The calculation for maximum INL and DNL (6.2) (6.3) comes from the idea that each unit cell will have some random deviation from the ideal value, and the maximum possible error is caused by the size ratio of the of the S/H capacitor to the rest of the capacitor array. The method used to try to reduce the matching error is to use an ADC capacitor array with a smaller S/H capacitor to capacitive array ratio. By reducing the ratio, then the mismatch error will be summed over fewer capacitors, resulting in a smaller total mismatch error. For this design, the ratio of the S/H capacitor to the LSB capacitor is not $2^9/2^0 = 512$, as is common for a 10 bit SAR ADC. Instead, the ADC S/H to LSB capacitor ratio is $2^5/2^0 = 32$ unit capacitors (Fig. 6.11). The 6 LSB capacitors are all equally sized capacitors with the 5 LSB capacitors employing a method of charge sharing (the charge sharing is explained in Section 6.3.2). By using this method of charge sharing, the 5 LSB capacitors still contribute binary weighted amounts of charge, but the signal is sampled onto a $32C$ MSB capacitor, and the reference charge is sampled onto a $(16+8+4+2+1+1)C = 32C$ capacitor array. Because the mismatch error is summed up for only 32 capacitors instead of 512 capacitors, the amount of accumulated error is only about 1/16 the amount as before. By reducing the number of unit cells in the S/H capacitor, not only is the overall size of the capacitor array greatly reduced, but the summation of the random mismatch capacitance is reduced to 1/16 the amount as before.

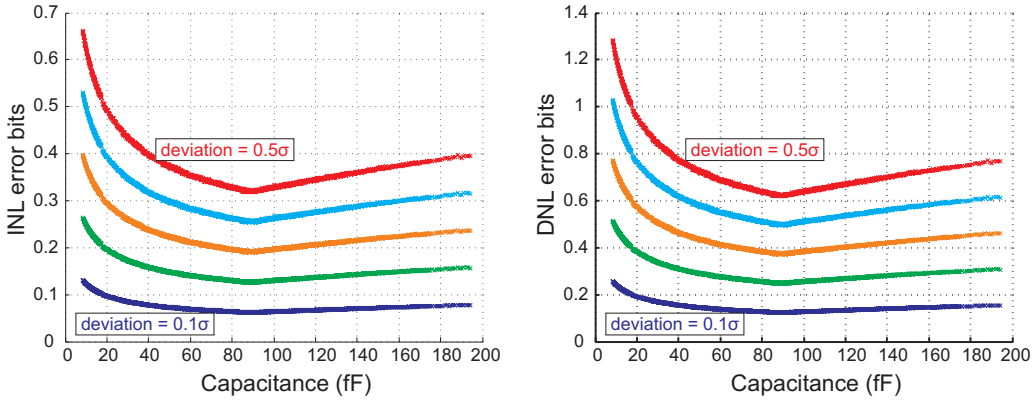


Figure 6.7: Matlab simulations of the Spectre Monte Carlo model file solving (6.2) and (6.3). The INL and DNL is for the implemented charge sharing capacitor array where the S/H capacitor is only 32x the size of the LSB capacitor.

The simulation results for the smaller count S/H capacitor is given in Fig. 6.7. For this design, only the capacitor arrays which fall within 0.4σ (the trace second from the top) of the ideal value will, according to (6.2) and (6.3), have DNL errors which are less than 0.5 LSB. This is a yield of only about 30%, but because this system is for a medical implant, small size has been given higher priority than high yield. Also, this 30% yield is itself a worst case scenario yield because (6.2) and (6.3) return the worst case INL and DNL errors. These worst case INL and DNL errors would occur only when every single unit cell capacitor which has a positive (or negative) ΔC belongs to the S/H capacitor, and all of the rest of the unit cells which have an opposite sign of mismatch belong to the rest of the array. This situation is itself not a random distribution, and the more probable distribution where the positive and negative mismatched capacitors are randomly spaced throughout the array will result in INL and DNL errors which are smaller than the worst case distribution that (6.2) and (6.3) solve.

The final size chosen for the ADC capacitor array unit capacitor value is 120fF. Under the worst case mismatch distribution, capacitor arrays where the mismatch standard deviation is about 0.45σ of the ideal mean value will have an INL of about 0.3 bits, and a DNL of about 0.5 bits.

6.3 Passive Fully Differential ADC Conversion

The implant's ADC is fully differential from input to output, and its charge redistribution routine is based on the design from [18]. One aspect of this capacitance to digital conversion system which can be exploited is the fact that the output voltage of the final pressure to analog voltage conversion is simply the product of the stimulation voltage, the sensor transfer function, and the OTA closed loop gain.

$$V_{\text{out}} = V_{\text{stim}} \left(\frac{C_s}{C_s + 2C_0} \right) A_{cl},$$

Because the pressure to analog conversion output is a ratiometric conversion from the stimulation voltage, there is no need to generate an accurate reference voltage generator for the ADC conversion. Instead, the best reference for the ADC conversion is the actual stimulation voltage which was used to generate the pressure sample.

During switch phase S1, the ADC samples the CDC conversion result from the OTA onto the top and bottom rails, and the reference potential gets sampled onto the ADC charge redistribution capacitor array at $V_{\text{REF}}\pm$. During phase S0, the ADC is electrically disconnected from the rest of the CDC system, and the ADC conversion takes place entirely during CDC switch phase S0. There are no timing conflicts between the CDC and ADC during phase S0 because the CDC is running at 4 kHz which means it remains in phase S0 for 125µs, and the 10 bit ADC clock is running at 500 kHz which means it only needs about 20µs to do a complete conversion. As the conversion progresses, each successive ADC capacitor either adds or subtracts charge from the ADC rail potentials until the final differential voltage across the top and bottom rail is zero.

6.3.1 The Charge Redistribution Block

The charge redistribution block of the ADC, shown in Figure 6.9a, uses a system of switches to control the charge redistribution of the ADC binary weighted capacitor array as the conversion progresses. Fig. 6.9b shows how during the S1 switch phase, the capacitance to analog signal conversion output from the OTA is sampled onto the ADC sample and hold (S/H) capacitor $V_{\text{RAIL}}\pm$, and how the stimulation voltage is applied directly from the capacitor bridge to the ADC capacitor array at nodes $V_{\text{REF}}\pm$. When V_{up}, V_{dwn}, and rst are all open, the ADC capacitor is essentially a floating packet of

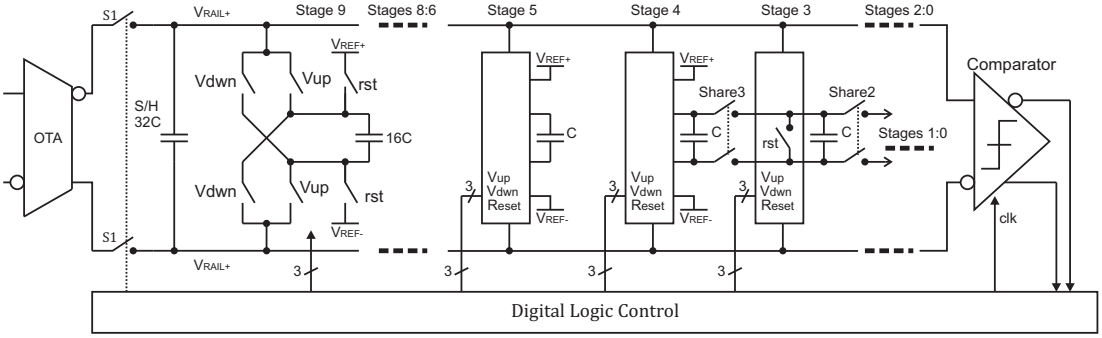


Figure 6.8: The SAR charge redistribution switching array showing the charge redistribution block with LSB charge sharing structures [18].

charge $Q = CV_{\mathrm{REF}\pm}$ waiting to be added to or subtracted from the charge on the $32C$ S/H capacitor.

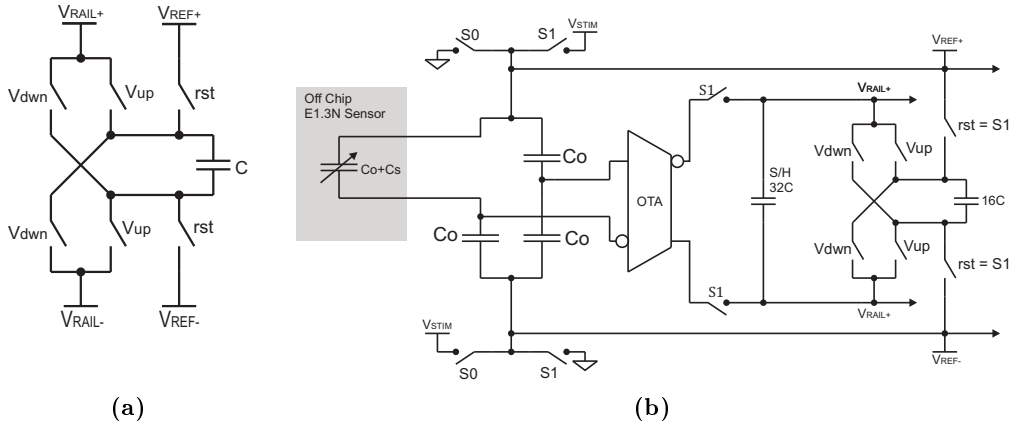


Figure 6.9: The ADC capacitor charge redistribution block.
a) The generic charge redistribution block.
b) The MSB stage charge redistribution block.

Each block of the ADC charge redistribution array in Fig. 6.8 operates as follows:

- During switch phase S1, the CDC conversion result is sampled onto the S/H capacitor, rst is closed sampling the reference onto the ADC capacitor, and V_{up} and V_{dwn} are open.
- Next, during switch phase S0, the phase where the rest of the CDC system is resetting itself, S1 and rst are opened, and the ADC conversion commences.

- The comparator determines the polarity across $V_{\mathrm{RAIL}}\pm$, and closes stage 9's either V_{up} or V_{dwn} switches to add or subtract charge from the S/H capacitor.
- The total rail capacitance is now

$$C_{\mathrm{RAIL}} = 48C,$$

the total charge is

$$Q_{\mathrm{RAIL}} = C(32V_{\mathrm{in}} \pm 16V_{\mathrm{REF}}),$$

and the voltage across the rails is

$$V_{\mathrm{RAIL}}\pm = \frac{Q_{\mathrm{RAIL}}}{C_{\mathrm{RAIL}}} = \frac{32V_{\mathrm{in}} \pm 16V_{\mathrm{REF}}}{48}.$$

- The comparator makes a decision for the $V_{\mathrm{RAIL}}\pm$ polarity and switches stage 8 accordingly. After the stage 8 charge redistribution, the voltage across the rails is

$$V_{\mathrm{RAIL}}\pm = \frac{Q_{\mathrm{RAIL}}}{C_{\mathrm{RAIL}}} = \frac{32V_{\mathrm{in}} \pm 16V_{\mathrm{REF}} \pm 8V_{\mathrm{REF}}}{56}.$$

- The process is repeated through the rest of the ADC capacitors in successive order until $V_{\mathrm{RAIL}}\pm = 0$ (Fig. 6.10).

Figure 6.10 shows the post layout simulation results of an ADC conversion. As the ADC conversion progresses, the ADC rails $V_{\mathrm{VRAIL+}}$ and $V_{\mathrm{VRAIL\text{-}}}$ are step by step brought closer to each other as their differential voltage is steadily reduced to zero.

6.3.2 ADC Capacitor Array LSB Charge Sharing

Charge sharing among the 5 LSBs of the ADC capacitor array has been implemented for a couple of different reasons. It was stated earlier that using charge sharing among the 4 LSBs helps to improve the INL and DNL performance by reducing the amount of accumulated random error. A larger LSB capacitor is desirable because according to [21] (6.1), the random mismatch attributable to the device area gets smaller as the area increases. There is another reason to try to reduce the MSB/LSB size ratio. The standard design of an N-bit SAR ADC calls for an MSB/LSB ratio of $2^9/2^0 = 512$ [11]. Even with a 20fF LSB, which would have horrible random mismatch properties (Fig. 6.6b), the MSB would be greater than 10pF which is more than twice the required

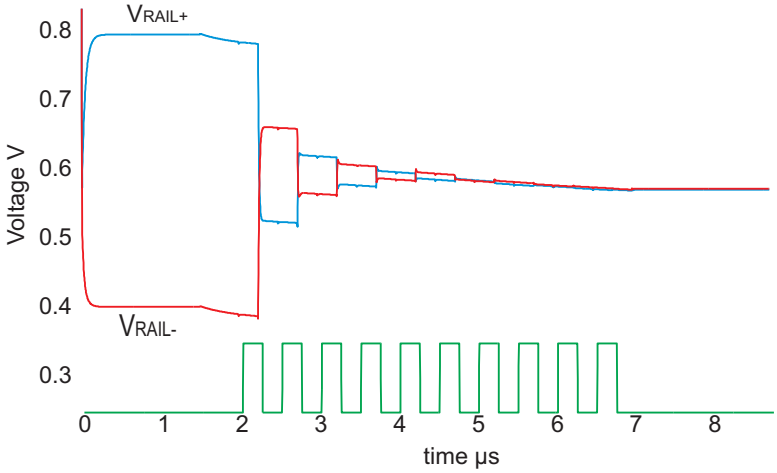


Figure 6.10: Spectre post layout simulation results from a single ADC conversion. With each step of the ADC conversion, the differential voltage gets closer to having 0VDC differential voltage across the outputs.

capacitance necessary for the OTA amplifier to meet its noise requirements which would require more than twice as much power per CDC channel.

The 5 LSB capacitors (stages 5 through 1) plus 1 dummy capacitor (stage 0) are equal in size, and charge sharing is performed between the 4 LSBs and the dummy capacitor as follows [18]

1. During rst, the stage 9 through stage 4 ADC capacitors are reset to the reference voltage, and the stage 3 through stage 0 ADC capacitors are cleared of any stored charge.

2. After rst is released, stage 5 and stage 4 each have $Q = CV_{\text{ref}}$ charge stored on their plates.

3. As the comparator is clocking the stage 9 decision, Share3 is closed, and the Stage 4 and Stage 3 capacitors are shorted together giving each capacitor $CV_{\text{ref}}/2$ of charge.

4. On the next comparator decision, Share3 is opened, leaving $CV_{\text{ref}}/2$ of charge on stage 4 and stage 3, and share2 is closed.

5. With the stage 3 and stage 2 ADC caps shorted together, the $CV_{\text{ref}}/2$ charge from stage 3 is evenly divided between stage 3 and stage 2 into $CV_{\text{ref}}/4$.

6. This process is repeated through to stage 0 resulting in a binary weighting of charge across the entire capacitor array, while maintaining a more easily achieved 32x ratio between the MSB S/H and LSB capacitor.

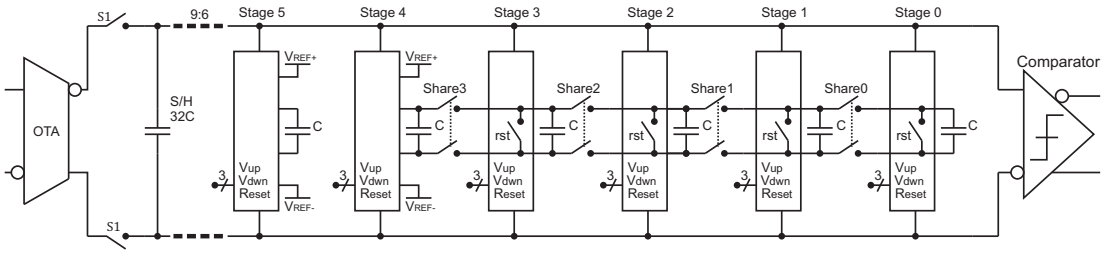


Figure 6.11: The charge sharing blocks of the ADC Charge redistribution switching array.

6.4 Comparator with Offset Cancellation

The comparator block for the ADC uses a fully differential preamplifier with input offset voltage compensation followed by a clocked regenerative latch comparator, followed by a static SR latch (Figure 6.12).

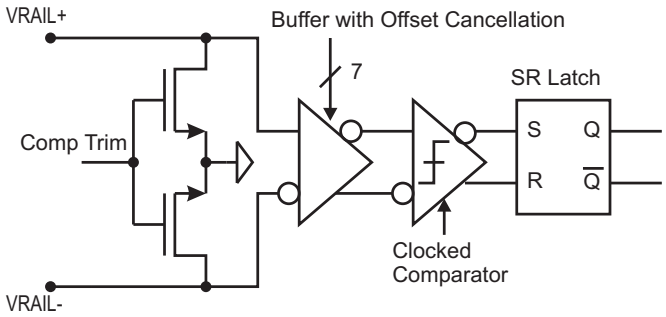


Figure 6.12: The comparator block of the ADC with: the comparator trimmer routine input shorting switches, the input buffer with integrated current steering offset calibration current sources, and the clocked comparator with the SR latch output.

6.4.1 The Comparator Preamplifier

The main purpose for the preamplifier is not to apply gain to the signal from the capacitor array. Instead, its main purpose is to reduce the comparator kick-back effect by providing a linear, differential, low output impedance signal to the clocked comparator.

As the comparator is clocked, there can be a significant amount of charge injected onto the comparator inputs from the C_{gs} capacitance of the comparator's input devices [25]. This flow of charge over the relatively short rise time of the comparator clock causes large voltage spikes even across a low impedance, and these spikes become quite unmanageable if the impedance is large. Driving the comparator with a low output impedance buffer will help to keep the voltage spikes from the kick-back current from exceeding the supply rail potentials.

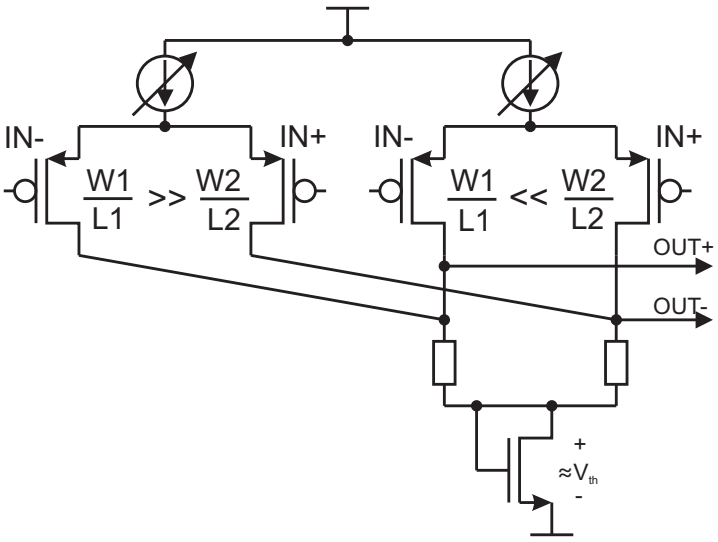
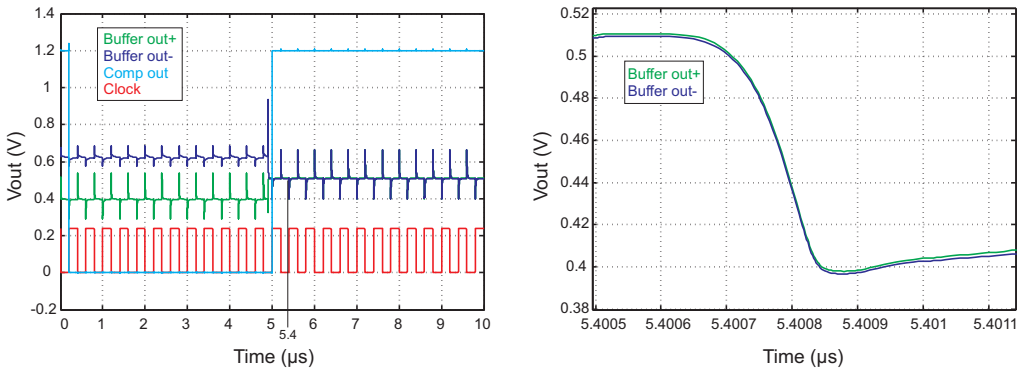


Figure 6.13: The comparator preamplifier buffer schematic with the adjustable tail current sources for the comparator offset trimming.

The reason for wanting a linear differential output impedance is because the charge kick-back voltage jump cannot be totally eliminated by the buffer, therefore it is important that the voltage jump not interfere with the comparator decision. The charge which is being kicked back by the comparator is a fairly common mode charge injection, and if this common mode charge is injected onto two loads which are of equal impedance, and linear by nature, then the differential voltage across the two input nodes will remain unchanged even though the common mode voltage takes a jump. Fig. 6.14b shows that even with a very small differential voltage, the polarity remains unchanged even though the common mode is significantly affected. For this reason, the amplifier's load in Figure 6.15 is implemented using poly resistors rather than MOSFET devices because of their linear $\frac{dI}{dV}$ relationship.



(a) (b)

Figure 6.14: The comparator preamplifier buffer kick-back reduction.
a) The comparator overdrive recovery simulation for when the input steps from very large negative voltage to very small positive 500µVDC.
b) The zoomed in view of the kick-back onto the comparator inputs. The inputs make a common mode jump, but the differential voltage remains constant.

For this design, the amplifier outputs are directly coupled to the clocked comparator's N-type MOSFET input devices, Fig. 6.12. To ensure that the comparator input devices are operating in strong inversion, Fig. 6.17, the buffer output voltages should be at least 100mV greater than the N-type threshold voltage of about 300mV. To get 400mV across the passive resistor output loads, the system will need either very large output impedance, which would consume a lot of chip space and defeat the purpose of have the amp for a low output impedance, or it will need a large amount of current flow.

The load resistors which were chosen for the buffer output impedance are 300kΩ, and the bias current was chosen as 320nA. The bias current of 320nA gives a gm of about 7µS, which gives an $A_0 = gmR_0$ gain of about 2 V/V, but it only gives about 100mV of drop across each resistor. To increase the common mode output voltage of the amplifier, the resistor bottoms are wired together and diode connected to ground, Fig. 6.13. Wiring the bottoms together ensures that the amplifier output load impedance is differential, and the diode serves to make sure that the resistor bottom potential is about V_{th}. The 100mV drop across the load resistor, plus the V_{th} drop across the diode connected MOSFET ensures that the gate potential on the comparator inputs are about V_{th}+100mV.

6.4.2 Comparator Input Offset Cancellation

The fully differential 10 bit ADC should be able to resolve the sampled signal down to about 2mV of resolution, but it is difficult to design an amplifier with only 2mV of input offset voltage. On top of this, the comparator itself also has input referred offset voltage which will further degrade the ADC conversion accuracy.

To get very low offset voltage from an amplifier, all devices need to be very closely matched, especially the input devices. To get good matching between the input devices, the devices need to be made large with common centroid layout, but this can create problems with the ADC operation. The inputs to the preamplifier are driven directly by the $V_{\mathrm{RAIL}}+$ and $V_{\mathrm{RAIL}}-$ conductors of the ADC capacitor array. This means that the buffer's input gate capacitance shows up as an added parasitic capacitance to ground. To keep the added parasitic capacitance small, the amplifier's input pair gate areas are kept as small as possible which results in a fairly large threshold voltage mismatch between two input transistors. The mismatch and resulting input offset voltage can never be reliably eliminated, therefore, comparator offset cancellation has been implemented to help zero out the error caused by the input referred offset voltage.

To perform the input offset cancellation, the preamplifier buffer has been designed with two parallel differential pair inputs which have input pair transistors that have been purposefully greatly mismatched with each other [26] (Fig. 6.13). As bias current is steered from one pair to the other, the different W/L ratios of the two devices results in different amounts of DC current flow through the load resistors, which acts to shift the DC differential output offset voltage. The circuit from Fig. 6.15 is the 7 bit current steering circuit used for biasing the offset trimmer buffer amplifier.

The method for performing the offset trimming is to assert the control signal "Comp Trim" from Figure 6.12 which shorts the amplifier inputs to virtual ground, and to then run a series of zero input voltage ADC conversions. If the comparator is by chance already perfectly matched with zero input offset voltage, then, because there is always some thermal noise present in the system, running a series of ADC conversions should result in equal amounts of ones and zeros. If, instead, there is mismatch, then the series of ADC conversions will come out mostly ones or mostly zeros depending on the direction of the amplifier mismatch. If this is the case, then the current can be steered

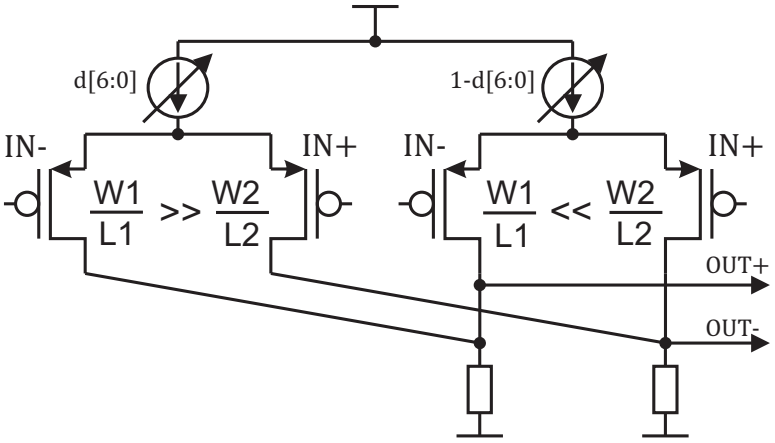


Figure 6.15: The buffer amplifier offset cancellation current steering circuit.

towards the appropriate differential pair which will bring the input referred mismatch down towards zero.

6.4.3 The Clocked Comparator

The comparator design is a clocked comparator which is driving an SR latch. The clocked comparator and latch do not consume any static power (except for leakage), and they only dissipate dynamic power upon switching. This makes this combination a low power solution for clocking the ADC conversion data to the implant's digital controller. The circuit in Fig. 6.16 is the original comparator latch designed for the StrongARM RISC microprocessor [27], and it is commonly referred to as the StrongARM latch.

In the circuit from Fig. 6.16, the transistors M_{TAIL} and M_{PRE} are used to precharge and clock the comparator, M_{LONG} provides a DC path to ground for the leakage current on nodes C and C' to prevent the SR latch output from changing if the inputs change during the precharge phase, and the 4 M_{REGEN} transistors make up a regenerative sense amp.

When the clock is low, M_{TAIL} is off and the comparator is in its off state. The transistors M_{PRE} are on and they are pulling nodes C and C' to V_{dd} which keeps the cross-coupled NAND gate SR latch in its current state. Because nodes C and C' are at V_{dd}, nodes B and B' are pulled up to $V_{dd} - V_{th}$, and then they slowly climb up to V_{dd}. M_{TAIL} is turned off, so node A also climbs upwards depending on the leakage ratio of M_{TAIL} and the input devices.

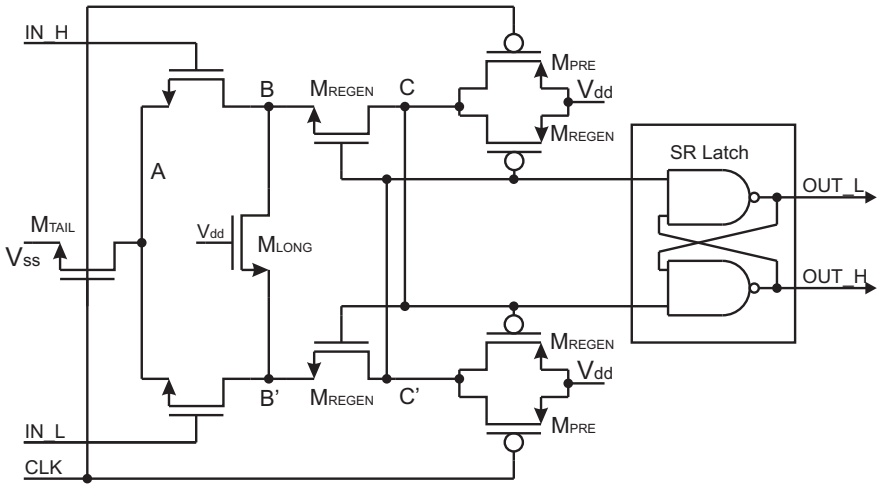


Figure 6.16: The StrongARM latched comparator.

As the clock switches from low to high, M_{TAIL} is turned on, and M_{PRE} is turned off. As node A is pulled to ground, the input device with the greater input gate potential will flow a greater amount of current which will pull either B or B' down more quickly than the other input device's drain potential. Because nodes C and C' are at V_{dd}, the faster falling B or B' will cause the regenerative latch to latch to a stable configuration, which depending on the regenerative latches final state will cause the cross coupled NAND gate SR latch to latch to the decision state. The NAND gate SR latch will then hold this state through the next precharge cycle until the next comparator decision.

The basic StrongARM latch can suffer from some hysteresis effects because of the time it takes for the comparator to precharge all of its nodes to the reset state. At the end of the last cycle's conversion, the nodes on opposing sides of the comparator are at either V_{dd} or ground. If at the end of the last conversion C was high, then C' is low, and both B and B' will be low. As M_{pre} are switched on, because C is already high, B' will track the rising C' potential, but B will not start to rise until C' has exceeded the V_{th} potential. Also, during precharge, node A is more or less a floating potential once it is greater than $V_{in} - V_{th}$ which can also be a source for indeterminate behavior.

For the original StrongARM purpose, hysteresis was not a major concern because the inputs were supposed to be driven by full on or full off input potentials, but for the purpose of ADC decision making it is good design practice to address all known sources of indeterminate behavior. The possible sources of hysteresis have been handled

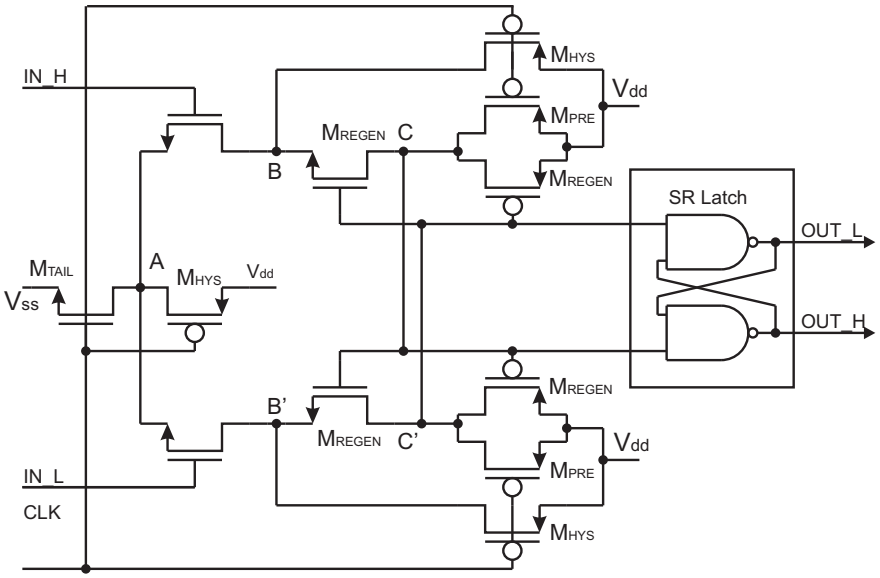


Figure 6.17: The ADC's low hysteresis StrongARM based latched comparator.

by driving all of the comparators nodes to a fixed potential during the recharge state. Fig. 6.17 is the comparator which was used for this ADC, and it shows the addition of 3 MOSFETs for hysteresis rejection, labeled M_{HYS}, and because the B and B' nodes are actively driven to V_{dd} during the precharge phase, the transistor M_{LONG} has been removed.

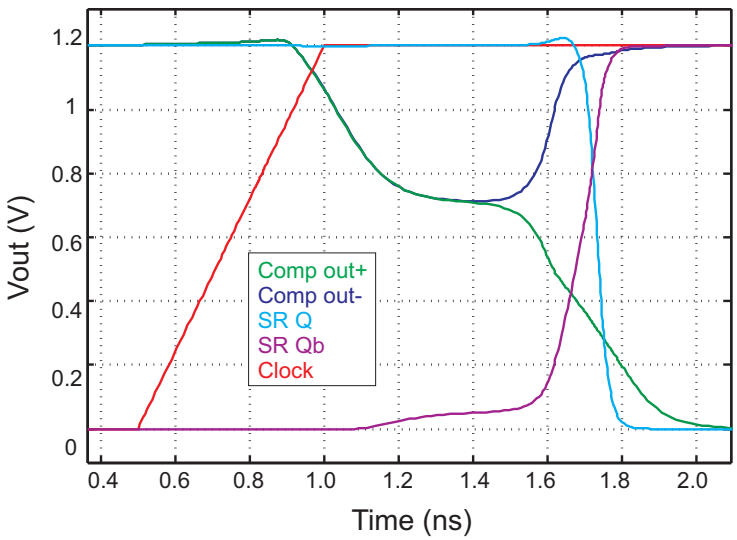


Figure 6.18: The comparator block switching with an input voltage of 200µV causing it to dwell in its metastable state for an extended period of time.

During simulations, the maximum amount of time that the comparator dwelled in its metastable state occurred with an input voltage of about 200μV. Even with the long delay caused by the metastability, the propagation delay from rising clock edge to SR latch update was only about 1ns. This greatly exceeds the requirements of the clock period decision time of 1μs.

6.4.4 The Comparator Input Offset Cancellation Routine

Fig. 6.19 shows the measured results of the implants 4 CDC channels performing the comparator offset cancellation routine. This routine is run once on power up, and the trim settings are stored in the implant's configuration settings register bank. Each comparator trimmer starts off at the 7 bit midpoint decimal value 64, and performs the offset cancellation routine independent from the other comparators.

The comparators begin by shorting their inputs together (Fig. 6.12) and running a series of comparator decisions. Depending on if the majority of the comparator decisions are 1's or 0's, the digital control either increments or decrements the offset trimmer control register which steers more current through one of the mismatched input diff pairs and less current through the other oppositely mismatched diff pair.

By flowing more or less current through the mismatched diff pair, this causes a slightly different amount of current to flow through one of the load resistors as compared to the other which results in an output voltage which counteracts the comparator input offset voltage. The routine repeats the process of sampling the shorted inputs until the comparator decision results start to become a fairly even ratio of 1's and 0's indicating that the input offset has been trimmed.

6.4.5 Minimizing the ADC Power Consumption

The ADC capacitor array is a passive array of capacitors which are driven by the CDC conversion active electronics, and this power consumption has already been designed to be as small as possible according to the noise and bandwidth requirements. The static power consumption of the ADC is mostly from the comparator buffer amplifier with some static power being consumed by the leakage current through the clocked comparator and the ADC digital control logic.

On conversion start, the current steering trim register has already been programmed during the chip power on initialization, so the only delay is the charging up of the current

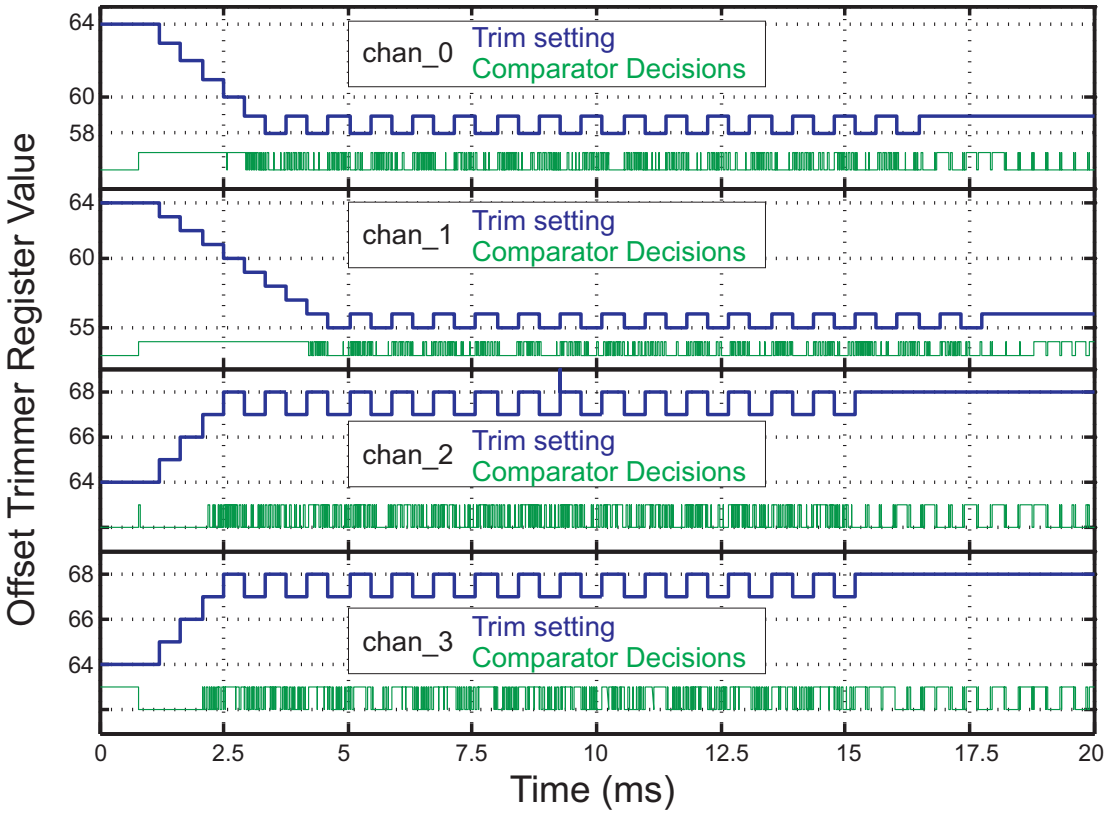


Figure 6.19: The measured behavior of the comparator input offset voltage cancellation routine trimming out the 4 ADC channels. Each channel starts at midpoint value of 64, and then the ADC is trimmed until the trimmer is only toggling between two trim settings which produce mostly 1's and mostly 0's. Once the trim routine is complete, the CDC begins sampling the pressure at a rate of 4ksps.

steering current circuits' V_{gs} bias voltages. If the trimmer were totally powered down, then the gate biases could reduce all the way down to ground potential. Simulations showed that the time required to turn on and stabilize all of the current sources and the buffer amplifier from this state was around 25 µs. However, if the trimmer is only put into a very low power mode, for example sourcing only 5 nA of current instead of the full 700 nA, then, using this power down routine, the amount of time required to restore full functionality to the current starved trimmer and buffer amplifier is greatly reduced to only a couple of microseconds.

The comparator current steering circuit is powered down by a short channel, very wide transistor which, even when turned off, leaks enough current that the buffer ampli-

fier's electronics don't ever totally power down, Fig. 6.15. This supply current modulation from full 700nA for 25µs to 5nA for 225µs brings the average current consumption down to 74.5nA, or about a 90% reduction in power consumption compared to if the buffer were not powered down. The leakage current through the comparator and latch is also only a couple of nA, and the leakage through the digital control logic blocks, according to the RTL synthesis power report, the leakage current is only about 22nA. This gives a total average static current consumption of about 100nA per ADC channel.

The majority of the power consumption of the ADC converter is the dynamic power consumption. There is some dynamic switching current consumption from from the charging of the 4.6pF ADC capacitor array from 0VDC to V_{DD} 4 thousand times per second

$$4.6(10^{-12}) * 4(10^{3}) \frac{Coulomb}{second} = 18.4nA,$$

but the majority of the dynamic current consumption is spent on the digital control logic. Post layout simulation of the digital control block shows a total dynamic current consumption of about 3µA. This dynamic current consumption of the digital control logic is about the same as the current consumption of the signal conditioning amplifier (about 3 µA), which brings the total current consumption of each CDC conversion channel up to around 6µA which is roughly 7.2µW of power per channel.

6.4.6 ADC Performance Measurements

Design verification for an ADC usually includes measurements for the signal to noise ratio, and INL and DNL measurements. Unfortunately for this ADC, a method for measuring INL and DNL has not been developed. Normally, the signal conditioning and conversion circuit could be connected to a voltage source with very fine resolution and control, and the voltage source would sweep across the ADC's input range, and the ADC conversion results could be compared against the voltage source's voltage.

The difficulty in accurately measuring INL and DNL is attributable to the structure of the capacitance to digital converter circuit. Looking at Fig. 6.9b, the capacitive bridge output is the gate input to the CDC system OTA. This means that the only effective way to sweep the input would be to take a reference capacitor and sweep it across the ADC full scale range, but, as of this thesis submission, such a measurement system has not yet been constructed.

It is possible to measure the system noise by letting the CDC conversion cycle run a few minutes worth of samples on a system where there is no input pressure modulation. At 4 ksps, a few minutes of measurements are a few hundred thousand samples. Performing an FFT analysis on the conversion results will give the energy content of the zero input signal, and summing the energy across the frequency and finding the ratio of the full scale signal power versus the average noise energy per Hz will give the SNR value of the CDC converter from OTA input to ADC output. Fig. 6.20 is the FFT SNR analysis of the measured results of the zero input signal CDC converter system, and it shows that the signal conditioning OTA exceeds the ADC's 10 bit dynamic range by about 0.13 bits of resolution.

$$ENOB = \frac{SNR - 1.76}{6.02} = 10.13 \text{ bits.}$$

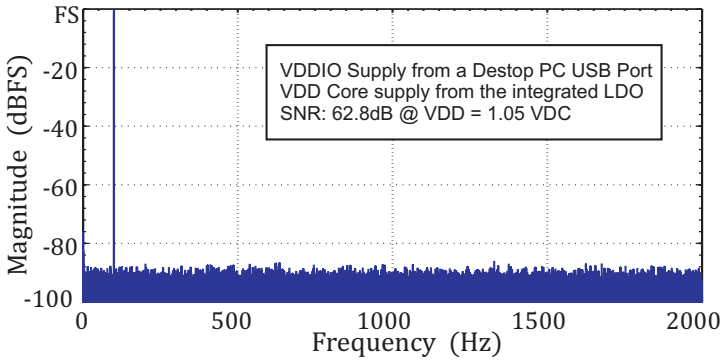


Figure 6.20: The noise spectrum is collected by running the CDC converter with constant sensor capacitance, and the tone is a sinusoid generated in software with the full scale 2^(10) peak to peak amplitude to be able to have a full scale reference for the SNR determination.

A common figure of merit (FOM) given to ADCs is calculated as the ratio of their power consumption to the product of their sample rate f_s and effective number of bits (ENOB).

$$FOM = \frac{Power}{2^{\text{ENOB}} f_s}$$

Making the admittedly optimistic assumption that the ADC has a full 10 ENOB, and only considering the power used by the ADC's capacitive array and the digital control logic, the FOM of the ADC is about

$$FOM = \frac{3\mu A * 1.2VDC}{2^{10} * 4kHz} = \frac{900\text{fJ}}{conversion}.$$

To reduce this FOM to an even smaller number, the most obvious target to go after is the control logic. The ADC design which this system implemented, [18], used asynchronous logic which allowed the conversion to be completed more quickly, and it greatly reduced the gate count of the control logic.

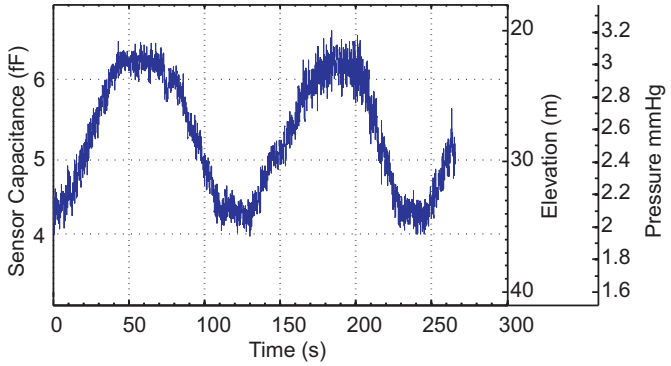


Figure 6.21: The measurement results from measuring the capacitive pressure sensor as it was carried up and down by an elevator across 4 building floors. The effective sample rate for this pressure test was 16 sps.

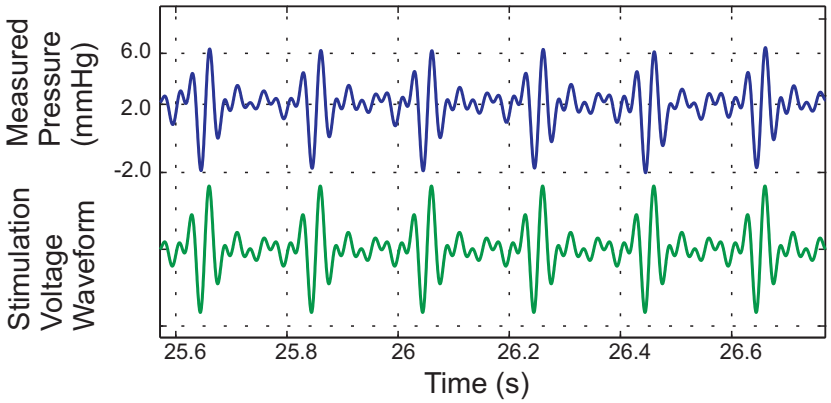


Figure 6.22: The pressure measurement results of the pressure inside of an audio subwoofer enclosure (top trace) when the subwoofer is being stimulated by a 5-tone chord of 25, 30, 35, 40, and 45 Hz (bottom trace). The effective sample rate for this pressure test was 96 sps.

Fig. 6.21 shows the measurement results from riding an elevator up and down across 4 building floors while recording the air pressure. The system has been designed for 0.75 mmHg resolution at 4 ksps, but, by implementing 128 times oversampling, the pressure resolution sensitivity can be increased. The elevator test measurement decimates the

4-ksps full speed sample rate down to 32 sps, which results in a capacitance resolution of about 200 aF, and a pressure resolution of about 0.05 mmHg. This increased resolution is achieved at the cost of sample rate, but the total analog power consumption remains less than 3 μW per CDC channel.

A third test was performed by placing the pressure measurement system inside of an audio subwoofer enclosure, and playing a 5-tone chord of 20, 25, 30, 35, and 40 Hz while measuring the pressure inside the enclosure. Fig. 6.22 gives the timespace plots of the measured pressure wave inside the enclosure (top trace), and the subwoofer input voltage signal (bottom trace).

7

Wireless Power Transmission

Any portable device which implements active electronic components requires a power source, and in most circumstances that power source is a battery. When it comes to medical implants, sometimes a battery based power supply is not the most desirable solution because a battery based system requires the periodic replacement of the depleted cells. Because of this drawback, a method for powering the implant using wireless power transmission has been developed which can meet the implant's energy requirements.

In the strict sense of the term "wireless power transmission" (WPT), power grid transformers accomplish this everyday with transmission efficiencies approaching 100% at the gigawatt power levels. However, these levels of efficiency are possible only because of the tight coupling between the primary and secondary coils, usually coupled together with a magnetically conductive core, giving approximately 100% flux linkage. Unfortunately, the implant's antenna does not benefit from any sort of tight coupling with the power sender antenna. Because the power sender antenna diameter is generally several orders of magnitude larger than the implant antenna's diameter, the two coils are very loosely coupled, and the usual transformer formulas, where $V_{\text{out}}/V_{\text{in}}$, is entirely determined by the primary to secondary turns ratio does not apply. Instead, it is necessary to design an energy transmission link designed to maximize the utilization of the power transmission medium, which in this case is the magnetic field through open space. This chapter will describe the method of wireless power transmission implemented during this research project's progression, starting with the RF power generator, then the power transmission antenna, and finally the energy harvesting antenna.

7.1 The Class E Power Amplifier

A switching amplifier has improved efficiency compared to a linear amplifier by using the power transistor as a switch which is either fully on or fully off. When the switch is fully on, then $V_{\text{ds}} = 0$, and when the switch is fully off $I_{\text{ds}} = 0$. Both of the states result in $P = IV = 0$, theoretically resulting in zero losses for 100% efficiency. However, in reality, large currents will flow with considerable voltage drop during the transistor's transition from full on to full off and back to full on. This is where the switching losses come from.

A class E power amplifier (PA) architecture maximizes amplifier efficiency by minimizing the transistor switching losses. The general term for the switching behavior of a class E PA is called zero voltage switching (ZVS), meaning that the power transistor switches on and off only when the drain voltage is at 0 Volts potential. The PA achieves ZVS by using as its output load a tuned LC resonant circuit which is tuned to resonate at the switching frequency. The step response into an undamped resonant load causes ringing, and by switching the transistor only at the zero crossings of the drain voltage caused by this ringing effect, the transistor switching losses can be eliminated.

The original inventor of the Class E amplifier [28, 29], and more recent papers as well [30, 31, 32, 33], all call for an RF choke to be used as the amplifier's load. For this design, instead of using an RF choke, the load network of the PA uses a parallel LC tuned tank circuit. The tuned circuit elements L_p and C_p make up a parallel resonant LC circuit, and such circuits have very high impedance (theoretically $Z = \infty + j0$) at $\omega_0 = 1/\sqrt{L_p C_p}$ and low impedance at all other frequencies.

Using a tuned LC network as the amplifier load has several benefits, making it a much more attractive load than a simple RF choke. All of these benefits arise from the singular fact that using a tuned LC network makes it possible to have a very large load impedance while using a much smaller load inductance than what would be necessary when using an RF choke. The benefits to using a smaller valued inductor in the PA are several fold such as:

- Smaller inductance values require smaller package sizes
- Smaller inductors need fewer windings which reduces the inductor's parasitic series resistance and parallel capacitance

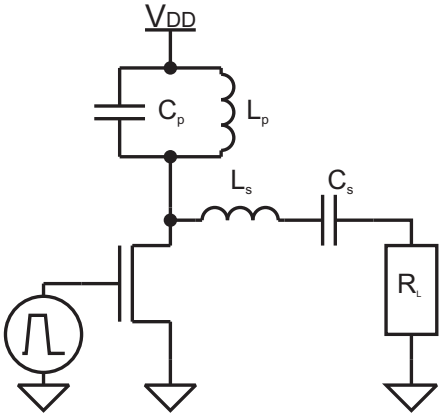


Figure 7.1: The class E power amplifier architecture used in this project.

- Smaller inductors need fewer windings which reduces the inductor's series resistance
- Smaller inductance with less parasitic capacitance results in higher self resonant frequencies

Another critical point where a smaller load network inductor helps is that power MOSFETS have an intrinsic output capacitance $C_{\text{oss}} \approx C_{\text{ds}} + C_{\text{dg}}$, where

$$C_{\text{ds}} + C_{\text{dg}}$$

are the MOSFET drain-source and drain-gate capacitance. A power MOSFET's C_{oss} can easily be several hundred picofarads, and if C_{oss} is larger than the parallel load capacitance called for by the standard set of design formulas (7.3) then that particular MOSFET cannot be used in the tuned amplifier. In addition to this, C_{oss} is very C_{ds} dependent, and C_{ds} is proportional to the drain voltage, causing the amplifier's behavior to change as the transistor's drain voltage oscillates up and down. Using a resonant load network helps with these problems because as the inductance gets smaller, the required resonant capacitance gets larger making it fairly easy to have $C_p > C_{\text{oss}}$. As C_p is made larger, then the drain voltage induced variations to C_{oss} will have less of an impact on the amplifier's resonant tuned output. In general, throughout the duration of the project, there were no occasions where it would have been preferable to use an RF choke as the load impedance.

7.1.1 Designing and Tuning the Power Amplifier

Almost any design reference on the class E amplifier gives a list of explicit design equations full of design factors which are derived by directly solving the amplifier under different operating conditions [28, 29, 30, 31, 32, 33]. To illustrate this point, the class E explicit design equations from [29] are given in (7.1) through (7.5),where V_0 is the MOSFET drain source voltage when it is switched on, Q_L is the network quality factor, ESR is the parasitic electrostatic resistance of the respective reactive component, R_L is the PA output impedance, R_{on} is the MOSFET on resistance, t_f is the MOSFET V_{ds} fall time, and T is the $1/f$ period

$$R = \left(\frac{(V_{\text{dd}} - V_0)^2}{P}\right) 0.576801 * \left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L^2} + \frac{0.205967}{Q_L^3}\right) \tag{7.1}$$

$$R_L = R - ESR_{\text{L}_s} - ESR_{\text{C}_s} - 1.365R_{\text{on}} - 0.2116 * ESR_{\text{C}_p} \tag{7.2}$$

$$C_p = \frac{1}{2\pi f R\left(\frac{\pi^2}{4} + 1\right)\frac{\pi}{2}}\left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right) + \frac{0.6}{(2\pi f)^2 L_p} \tag{7.3}$$

$$C_s = \frac{1}{2\pi f R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{(2\pi f)^2 L_p} \tag{7.4}$$

$$L_s = \frac{Q_L R}{2\pi f} \tag{7.5}$$

The design method presented here does not use these explicit design equations. Instead, a more intuitive design method, based entirely on the desired PA output impedance and quality factor, is used to choose the reactive components. The PA in Fig. 7.1 has a parallel LC network as its load with a series LC output network, and both networks have a resonant frequency $\omega_0 = 1/\sqrt{LC}$. The PA is tuned when the series network, L_s and C_s, is tuned to a resonant frequency $\omega_s = \omega_0 - \Delta\omega/2$, and the parallel network, L_p and C_p, is tuned to $\omega_p = \omega_0 + \Delta\omega/2$. For this design method, knowing the exact value of $\Delta\omega$ before constructing the amplifier is not too critical. A circuit design simulator, such as Spice [34], can be used to find the required $\Delta\omega$. But, in a real life environment, it is much quicker to place the reactive component values with $\omega_s = \omega_p = \omega_0$, and to then simultaneously tune ω_s to a lower frequency, and ω_p to higher frequency using trimmer capacitors or inductors until the drain voltage operates with the desired zero voltage switching.

Starting with the PA Fig. 7.1, a desired Q_L, R_L, and operating frequency f, the design process proceeds as follows:

1. Choose a value for Q_L based on the design requirements.
   - Q_L is usually chosen to be a value somewhere between 3 and 20.
   - A higher Q_L has sharper bandpass filtering resulting in less sideband energy.
   - Lower Q_L amplifiers were usually easier to tune.
2. Choose an amplifier output impedance (7.6) based on the available supply voltage and desired output power[1].
   - Lower R_L delivers more power using lower V_{dd}
   - Higher R_L requires less load current for the same output power resulting in less power loss to the PA's parasitic resistances.
3. Choose a nominal value for L_s (7.7), C_s (7.8), and L_p (7.9).
   - Choosing L_p is a fairly non-critical step because a very wide range of values are acceptable, and it was only necessary that $L_p < L_s/2$.
   - Eq. (7.9) was shown to be effective for $2 \leq Q_L \leq 30$
4. Choose a nominal value for C_p (7.10).
5. Trim, simultaneously, the parallel load to a higher resonant frequency, and the series network to a lower resonant frequency until $\omega_p - \omega_s = \Delta\omega$. An oscilloscope is used to determine when $\omega_p - \omega_s = \Delta\omega$ as this is the point where zero voltage switching is achieved.

[1] The PA output power is not exactly given by (7.6). The effective supply voltage seems to be reduced as the quality factor is increased, but even with this scaling, the PA output power is still a function of the square of the supply voltage

$$R_L = \frac{V_{\mathrm{dd}}^2}{P} \tag{7.6}$$

$$L_s = \frac{Q_L R_L}{\omega_0} \tag{7.7}$$

$$C_s = \frac{1}{\omega_0^2 L_s} \tag{7.8}$$

$$L_p = \frac{L_s}{2\sqrt{Q_L}} \tag{7.9}$$

$$C_p = \frac{1}{\omega_0^2 L_p} \tag{7.10}$$

There are no real requirements for the parallel network ω_p and serial network ω_s to be equally spaced above and below ω_0. Instead, it is only necessary that $\omega_s < \omega_0$ and $\omega_p > \omega_0$, and that $\Delta\omega$ is large enough to achieve zero voltage switching as in Fig 7.3a.

On the practical side of the design process, trimming the ω_s and ω_p resonant frequencies was performed using trimmer capacitors instead of trimmer inductors. This is because it was easier to find high voltage, temperature stable, mica film capacitors with a wide adjustment range than it was to find high current, high frequency, inductors which could be tuned across a wide range.

7.2 Output Load Impedance Matching and Filtering

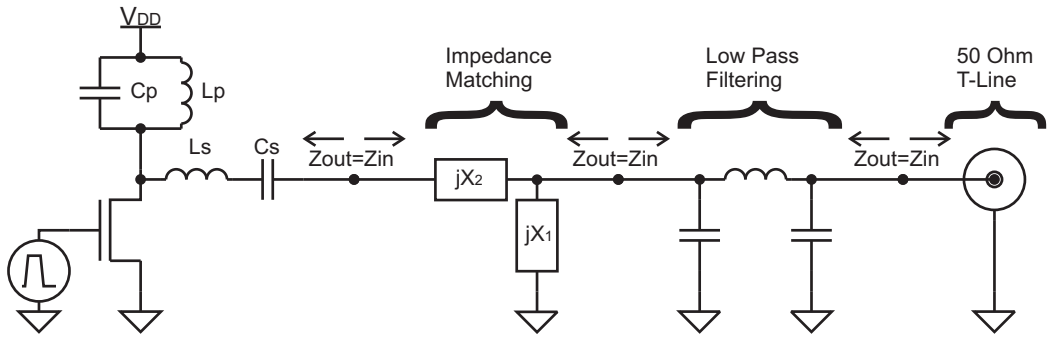


Figure 7.2: The class E amplifier with impedance matching and output low pass filtering.

The PA is connected to an antenna by a 50Ω coaxial transmission tine, for which it is necessary to match the PA's output impedance to the 50Ω transmission line impedance.

7.2.1 Output Impedance Matching

Depending on the required output power and the available supply voltage, R_L (7.6) will probably not be equal to the transmission line impedance of 50Ω. If this is the case, then it is necessary to transform the PA's R_L output impedance to match the 50Ω coaxial line impedance. The PA output impedance R_L can be transformed into a different output impedance by populating the $jX1$ and $jX2$ components with their appropriate values (Fig. 7.2). The appropriate values can be derived using equations which generate the lumped reactive element values [35], or through the use of a vector network analyzer (VNA) [36].

7.2.2 Output Low Pass Filtering

The PA's output has fairly significant amounts of harmonic energy because of the non-sinusoidal nature of the V_{ds} signal voltage, Fig. 7.3a. Many of the harmonics are suppressed by the bandpass properties of the series resonant L_sC_s circuit, but there are limits to the amount of Q_L which can be designed into the amplifier. Designing a PA with a higher Q_L can bring about difficulties caused by the large valued L_s, and a very high Q system is also more difficult to keep perfectly tuned when compared to lower Q designs (this statement is made according to general observations, and not necessarily true under all conditions). In order to ensure compliance with the various spurious sideband emission requirements [37], a 3^{rd} order low pass filter is placed after the impedance matching network to give an additional 18dB/octave rejection.

7.2.3 The Output Power Level

Any extra energy harvested by the implant is dissipated as heat into the surrounding tissue, so it is important that the PA's output power can meet the energy requirements of the implant without transmitting too much extra power. To accommodate non-optimal operating conditions such as patients of different sizes, implants implanted with non-perfect receiving antenna orientation, and different power consumption requirements, the PA's output power level needs to be dynamically adjustable. Being able to dynamically control the PA's supply voltage is an effective way of ensuring that the PA is not transmitting too much or too little power.

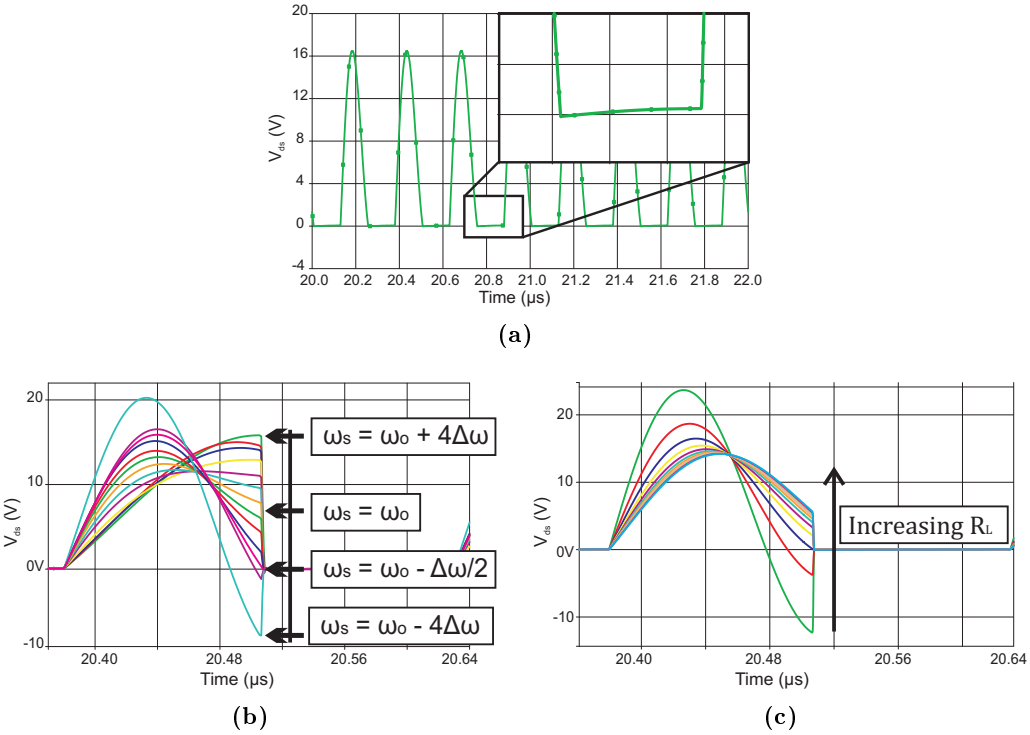


Figure 7.3: The power efficiency of the class E amplifier comes from its ZVS operation. The four figures show the measured and PSpice simulation of characteristic V_{ds} waveforms:
a) V_{ds} of the constructed class E amplifier
b) V_{ds} of the PA when R_L is stepped from $R_{L_{\text{tuned}}}/4 \rightarrow 2.5R_{L_{\text{tuned}}}$
c) V_{ds} of the PA when $\Delta\omega$ is stepped from $\omega_s = \omega_0 - 4\Delta\omega_{\text{tuned}}$ up to $\omega_s = \omega_0 + 4\Delta\omega_{\text{tuned}}$

According to (7.6), the output power follows the general $P = V^2/R$ relationship. Therefore, in order to adjust the amplifier output power, it is only necessary to adjust the amplifier's supply voltage. The amplifier supply voltage regulation circuit is given in Fig. 7.4. It is a single ended primary inductor converter (SEPIC) with duty cycle (D) dependent buck and boost output voltage (7.11).

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D}{1-D} \tag{7.11}$$

This switched mode DC-DC voltage converter has no difficulty bucking and boosting the input voltage by 4x up and down for a dynamic output voltage range of 1-16x, or 24dB, which allows a single amplifier design to operate with an output power from 150mW to 40W by only adjusting the PWM duty cycle from 20% to 80%. The resolution of the SEPIC converter output is dependent on the resolution of the PWM controller

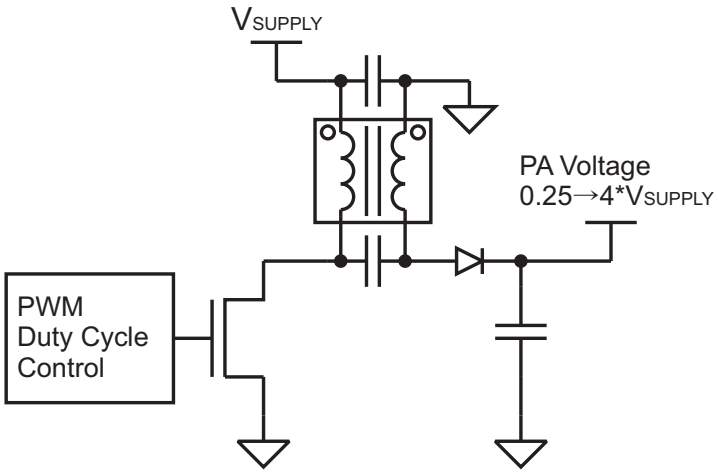


Figure 7.4: The power amplifier supply voltage SEPIC DC-DC voltage converter circuit supplies the PA with a DC voltage which ranges from Vsupply/4 to 4xVsupply.

duty cycle, which, thanks to the wide availability of fast microcontrollers with 16 bit counters, can very easily be in excess 0.1%.

7.3 The Power Transmitting Antenna

Because of the electrolytes dissolved throughout the various tissues, the human body is a fairly good electrical conductor. Some tissues do have less electrical conductivity than other tissues [38, 39], but in general, the human body's conductivity will act to short the electric field component of the RF energy, thereby absorbing the electric field and dissipating it as heat. These losses can be very high. For example, microwave ovens are very effective at heating food using 2.45 GHz RF energy, where 90% of the RF energy is dissipated as heat for every ≈5cm of penetration depth into muscle tissue. Luckily for our purposes, even though the human body is an electrical conductor, it is not a magnetic conductor. Therefore, the magnetic field component does not suffer attenuation when its field lines penetrate human tissues in the same way that the electric field would be attenuated.

To avoid dissipating large amounts of energy as heat into the human body, the power coupling is performed using the magnetic field. Fig. 7.5 shows a simplified model of the antenna design and how the magnetic field is stored in the space volume around the inductor, and the electric field is stored between the plates of the capacitor.

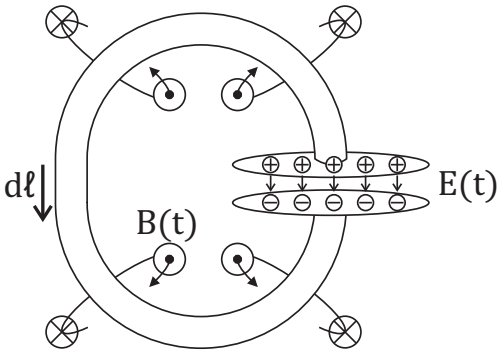


Figure 7.5: Simplified diagram of the LC resonant power transmitter antenna. The enclosed B field points out of the sheet, and $\frac{\partial B}{\partial t} > 0$. The B field is entirely stored in the space around the loop conductor, and the E field is stored between the capacitor plates.

7.3.1 Current Carrying Wire Loop

The transmitting antenna for this design is constructed by wrapping a strand of braided wire around the torso of the patient. Efficient transmission of power from the transmitting antenna to the receiving antenna requires that the magnetic field generated by the power sender at the location of the receiving antenna needs to be maximized. Starting with a statement of the Biot-Savart law (7.12), the magnetic field at the center of a single turn current carrying loop is given by (7.13). If the wire loop is placed around the torso so that the implant is located directly at the center of the wire loop ($z = 0$), then for an N-turn wire loop antenna with current I the magnetic field at its center is given by (7.14).

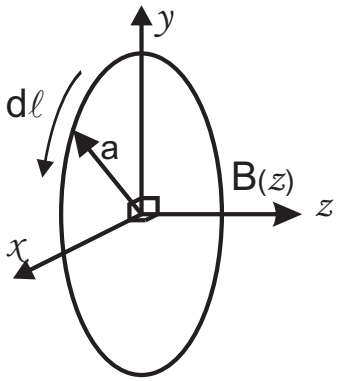


Figure 7.6: Magnetic field generation from a current carrying wire loop.

$$B = \frac{\mu_0 I}{4\pi} \oint \frac{dl \times \hat{a}}{|a^2|} \tag{7.12}$$

$$B_{L_1}(z) = \frac{\mu_0 I_{L_1}}{2} \frac{a_1^2}{\left(a_1^2 + z^2\right)^{\frac{3}{2}}} \tag{7.13}$$

$$B_{L_1}(z=0) = N\left(\frac{\mu_0 I}{2a_1}\right) \qquad \text{where } N = \text{number of loops} \tag{7.14}$$

7.3.2 The Antenna

The transmitting antenna is wire loop inductor L_1 with radius a, current I, and magnetic field strength (7.14) in a series RLC circuit like Fig. 7.7. L_1 is the wire loop antenna, and C_1 is the resonance matching capacitor, and R_{par} is the parasitic resistance of the wire loop. To determine the amount of B_{L_1} field which is generated by the wire loop, the frequency dependent impedance of the series RLC circuit, (7.15), can be used to find the current I_{L_1} through the wire loop inductor, (7.17). Eq. (7.17) can then be used to solve for the loop current as a function of input power (7.18).

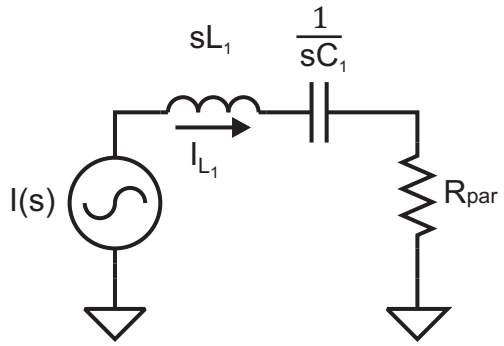


Figure 7.7: The series RLC circuit.

$$Z(s) = R_{\text{par}} + sL\left(1 + \frac{1}{s^2 LC}\right) \tag{7.15}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$s = j\omega$$

$$Z(j\omega_0) = R_{\text{par}} + j\omega_0 L(1 + (-1)) = R_{\text{par}} \tag{7.16}$$

$$I_{L_1}(j\omega_0) = \frac{V_{\text{in}}}{Z(j\omega_0)} = \frac{V_{\text{in}}}{R_{\text{par}}} \tag{7.17}$$

$$P = I^2 R$$

$$I_{L_1}(j\omega_0) = \sqrt{\frac{P_{\text{in}}}{R_{\text{par}}}} \tag{7.18}$$

In accordance with 7.14, increasing the number of turns will increase the magnetic field strength. However, increasing the number of turns will also increase the conductor length which increases the parasitic resistance which reduces the amount of current flowing through the RLC circuit. If we take R_0 to be the parasitic resistance per inductor loop so that for N number of turns, $R_{\text{par}} = NR_0$, then (7.18) becomes (7.19), and combining (7.14) and (7.19) results in (7.20) which is a statement of the B field as a function of the input power, P_{in}, and the antenna dimensions and parasitic resistance per loop.

$$I_{L_1}(j\omega_0) = \sqrt{\frac{P_{\text{in}}}{NR_0}} \tag{7.19}$$

$$B_{L_1} = \frac{\mu_0}{2a_1}\sqrt{\frac{P_{\text{TX}} N}{R_0}} \tag{7.20}$$

From (7.20), the field strength generated from a fixed input power increases with the square root of the number of turns N. However, increasing the magnetic field strength by increasing number of turns has a practical limit set by the ease of installing a multi-loop antenna around the torso of the patient. Also, as the number of loops is increased, the

proximity effects caused by the decreasing loop separation plus the eventual necessity of reducing the conductor cross section to be able to fit more loops, will increase the parasitic R_0 further reducing the incremental gains provided by more wire loops.

For the animal testing conducted during this project, with the implant located inside the abdominal aorta of a 100kg swine, a single loop antenna oscillating at 4 MHz with $P_{\text{in}} = 500\text{mW}$ was more than sufficient to supply the implant's $400\mu\text{W}$ power requirements.

7.3.3 Antenna Impedance Matching

The antenna's input impedance needs to be matched to the transmission line's 50Ω line impedance. This project's earlier antenna designs used a rigid copper coil which was tuned in the laboratory, and then put to use in the operating environment. It was noticed that making very slight changes to the antenna's surrounding environment could easily reduce the transmitted power by 20 dB (90%) or more. Instead of using a rigid antenna which has been tuned in a laboratory environment, the antenna for this wireless power transmission system was first placed around the patient's torso and then tuned to 50Ω impedance.

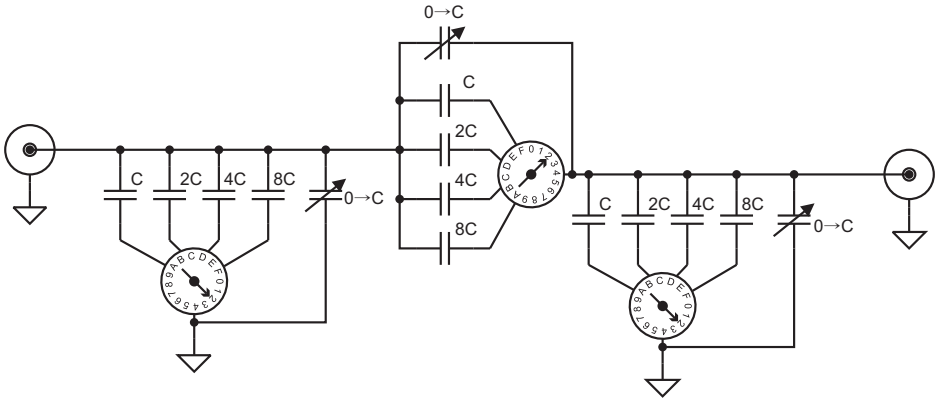


Figure 7.8: The antenna matching board for quickly tuning the antenna.

Tuning the antenna on the spot produced very good results, but this method required that the matching could be completed very quickly. To enable quick 50Ω tuning of the antenna, the network of capacitors and switches in Fig. 7.8 is used as the impedance matching network. The switches are implemented with binary encoded rotary switches, and the capacitors are arranged in a binary weighted progression. With the help of a

vector network analyzer and the circuit from Fig. 7.8, the whole process of antenna installation and impedance matching was easily accomplished in less than 5 minutes time. Initially, there was concern that the switches would degrade the antenna performance, but at 4 MHz transmission frequency, there was no evident performance degradation.

7.3.4 Choosing the Transmission Frequency

A few different factors need to be considered when choosing the frequency which will be used for the power transmission. Higher frequencies allow for smaller valued reactive components in the implant. This single fact makes it very desirable to use the highest frequency possible. However, there are limits to the maximum frequency, mostly as a result of the dielectric losses to the various body tissues.

As stated earlier, the goal is to transmit the power using only magnetic field coupling. This requires that the loop antenna conducts as much current as possible through its wire loop, with as small of a radiated EM field as possible. To do this, it is necessary that the wire loop antenna be a very poor radiator of the electromagnetic fields. If the EM field is not radiating away from the antenna, this means the reactive energy of the EM field is only oscillating between the L and the C of the antenna and not between the the $\vec{H}$ and $\vec{E}$ fields of free space. A common term used for describing the amount of free space electromagnetic field radiation generated by the current flowing through a conductor is the radiation resistance R_r of that conductor. The radiation resistance of a wire loop is given as (7.21) [40]

$$R_r = 120\pi\frac{8}{3}\pi^3\left(\frac{A}{\lambda^2}\right)^2, \tag{7.21}$$

where 120π is the free space impedance, A is the surface enclosed by the loop, and λ is the wavelength. Fig. 7.9 shows a plot of the radiation resistance as a function of the ratio of the wavelength over antenna loop diameter.

The common term for an antenna which is a poor radiator is an "electrically short" antenna, where the electric length indicates the ratio of the electrical wavelength λ to the electrical conductor length. A conductor is electrically short when $\lambda \gg$ conductor length. Keeping in mind, that because of the velocity of propagation through copper, λ in copper is about 2/3 of the free space λ. This project used antennas

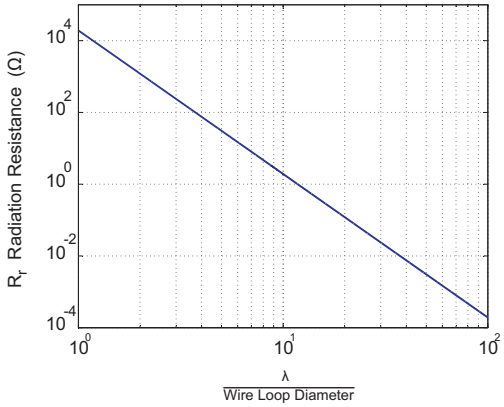


Figure 7.9: The wire loop antenna radiation resistance as a function of $\frac{\lambda}{\text{diameter}}$.

with loop diameters smaller than $\lambda/50$, with the maximum size and frequency combination of a 1m wire loop diameter oscillating at 4 MHz (which has an electric length of about $\lambda/50$).

7.4 The Power Receiving Antenna

The implant is powered by harvesting the magnetic field being generated by the transmitting antenna (7.20) with a ferrite core inductor in a parallel LC resonant circuit. The transmitter maximizes its magnetic field generation, B_{L_1}, by minimizing its parasitic resistance thereby maximizing the current flow. The implant maximizes the amount of energy it can collect per unit volume by using a magnetic core with high permeability μ_r to amplify the B_{L_1} magnetic field. The total effective magnetic field of the implant solenoid inductor is (7.22).

$$B_{L_2} = \mu_r B_{L_1} \tag{7.22}$$

The implant needs the energy collecting inductor be as small as possible, therefore it is helpful to derive a formula which can give guidance on how to size the implant inductor in terms of package size and inductance value [41]. Starting with the formulas describing self inductance (7.23), the magnetic field of a solenoid (7.24), and the energy

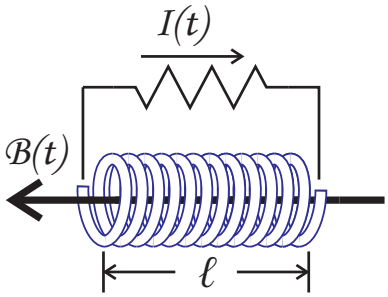


Figure 7.10: The energy harvester solenoid antenna.

stored in the solenoid inductor L_2 (7.25)

$$L = \frac{\Phi}{I} \tag{7.23}$$

$$B = \mu n I \tag{7.24}$$

$$E_L = \frac{1}{2} L I^2, \tag{7.25}$$

where $n = N/l$, l is the solenoid length, and $\mu = \mu_0 \mu_r$, it is necessary to derive a formula which solves for the energy stored in the solenoid as a function of the magnetic field strength and solenoid volume V_{sol}. The flux of the solenoid's magnetic field is

$$\Phi_B = \mu n I A \tag{7.26}$$

where A is the solenoid cross sectional area. The total flux linkage from all of the N number of solenoid turns to the flux Φ_B flowing through the turns is

$$\Phi = \mu n I A N \equiv L I \tag{7.27}$$

from which the solenoid self inductance is

$$L = \mu n A N. \tag{7.28}$$

The solenoid energy in terms of its self inductance is

$$\frac{1}{2} L I^2 = \frac{1}{2} \mu n A N I^2,$$

and substituting $N = nl$ results in an expression for the implant antenna's L_2 solenoid

energy as a function of its magnetic field B_{L_2}, permeability μ_r and volume (7.29).

$$\frac{1}{2}LI^2 = \frac{1}{2}\mu n(nl)AI^2$$

$$\frac{1}{2}LI^2 = \frac{1}{2\mu}(\mu nI)^2(lA)$$

$$E_L = \frac{B_{L_2}^2}{2\mu}V_{\text{sol}} \tag{7.29}$$

Because the magnetic field which is energizing the implant's solenoid is the field generated by the power transmission antenna B_{L_1} (7.20), then combining (7.20), (7.22) and (7.29) results in (7.30), which is the solenoid's energy storage as a function of the TX antenna's power and dimensions and the implant's volume and permeability.

$$E_{L_2} = \frac{P_{\text{TX}}N_{L_1}}{a_1^2R_0}\frac{\mu_0\mu_r}{8}V_{\text{ol}} \tag{7.30}$$

The main point about (7.30) is that the amount of energy which can be collected by the implant is not a function of its amount of inductance. Instead, aside from the factors governed by the power transmitting antenna, the energy harvester's energy collection is a function of the solenoid's relative permeability and volume, and it has nothing to do with the number of wire loops around the solenoid core.

7.4.1 Choosing the Implant Inductor

In the Laplace domain, the inductor impedance is given as

$$Z = sL$$

and the maximum amount of power which the inductor can source to a load is

$$\frac{dE}{dt} = P = VI = (sLI)I = I^2(sL) \tag{7.31}$$

Equation (7.31) shows that for a fixed amount of E_{L_2} there is a fixed amount of available P for which I and V are inversely proportional to each other. As the energy harvester sources more voltage, it must source less current, and vica versa for sourcing more current it must source less voltage. Because an inductor has the frequency dependent voltage current relationship

$$V = sLI, \tag{7.32}$$

which shows that increasing V will reduce I, it is important that the inductance be chosen according to the $P = IV$ requirements of the implant, rather than trying to simply generate the highest voltage possible.

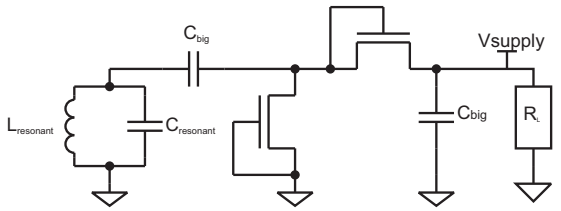


Figure 7.11: The implant energy harvesting electronics

The implant energy harvester is a resonant network feeding a rectifier followed by a large AC decoupling capacitor Fig. 7.11. The rectifier load looks like an open circuit until the diodes start to conduct, at which point the load looks like a short. This very nonlinear behavior of the load made accurately quantifying the exact volume and inductance requirements using mathematic equations quite difficult. Throughout the course of the project, several attempts were made to develop a set of general equations which could be used to derive the exact required size requirements of the implant inductor, but none of the attempts were particularly successful. Instead, the general design guidelines for energy harvester sizing which were followed are:

- Choose a solenoid ferrite material which had the highest permeability available.
  - The frequency dependence of the ferrite core's permeability must be taken into account because high permeability materials get real lossy at higher frequencies.
- Size the solenoid to be the largest volume allowed by the implant size requirements.
- Construct a few different inductors with the solenoid, and determine which inductance is able to power the implant with the lowest transmitter power.

7.5 Maximizing the Power Transmission Efficiency

The wireless power transmission system has two resonant coils, the primary side coil L_1 which is the series RLC configuration of Fig. 7.12a, and the secondary side coil L_2

which is the parallel RLC configuration in Fig. 7.12b. A common observation during the project was that increasing the number of turns in the primary side, and reducing the number of turns in the secondary side would result in better power transmission efficiency. The reason for this can be explained by considering the requirements for efficient wireless power transfer.

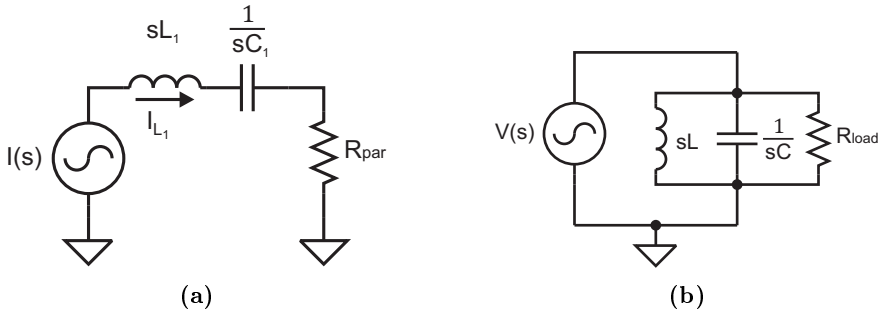


Figure 7.12: a) Series and b) Parallel RLC resonant circuits

There have been many different methods presented in recent years concerning maximizing the power transmission efficiency [42, 43, 44, 45], and while each method might differ slightly in their details, there is one main overriding constant message which is always appearing in literature covering loosely coupled wireless power transmission. The main idea expressed for maximizing wireless power transmission is to use high quality factor (Q, or Q-factor) transmitters and receivers, where Q is the ratio of reactive versus resistive energy. To determine the Q-factors of the two antennas, it is only necessary to derive the peak reactive energy storage against the time average resistive power dissipation.

$$Q_{\text{series}} = \frac{\omega_0 E_{\text{peak reactive}}}{P_{\text{rms}}}$$

For the series RLC circuit, Fig. 7.12a, $I_L(s) = I_{R_{\text{par}}}(s)$, so the resistive and reactive

energies are found according to their current flow. The Q-factor, (7.36), at ω_0 is :

$$E_{\text{peak reactive}} = \frac{1}{2}LI^2 \tag{7.33}$$

$$P_{\text{rms}} = I_{\text{rms}}^2 R_{\text{par}} = \frac{1}{2}I^2 R_{\text{par}} \tag{7.34}$$

$$Q_{\text{series}} = \frac{\omega_0 \frac{1}{2}LI^2}{\frac{1}{2}I^2 R_{\text{par}}} \tag{7.35}$$

$$Q_{\text{series}} = \frac{\omega_0 L}{R_{\text{par}}} \tag{7.36}$$

Similarly for the parallel RLC circuit, Fig. 7.12b, $V_C(s) = V_L(s) = V_{R_{\text{load}}}(s)$, so the resistive and reactive energies are found according to their voltage. The Q-factor, (7.41), is derived as follows:

$$E_{\text{peak reactive}} = \frac{1}{2}CV^2 \tag{7.37}$$

$$P_{\text{rms}} = \frac{V_{\text{rms}}^2}{R_{\text{load}}} = \frac{1}{2}\frac{V^2}{R_{\text{load}}} \tag{7.38}$$

$$Q_{\text{parallel}} = \frac{\omega_0 \frac{1}{2}CV^2}{\frac{1}{2}\frac{V^2}{R_{\text{load}}}} \tag{7.39}$$

$$Q_{\text{parallel}} = \omega_0 C R_{\text{load}} \tag{7.40}$$

$$C = \frac{1}{\omega_0^2 L}$$

$$Q_{\text{parallel}} = \frac{R_{\text{load}}}{\omega_0 L} \tag{7.41}$$

For the power transmitter antenna, the behavior observed in the laboratory was that increasing the number of turns increased the $\vec{B}$ field, (7.20), and thereby the power transmission efficiency was also increased. With its series configuration, (7.36) shows that as L is increased or R_{par} is reduced, its quality factor and power transmission efficiency should increase. Increasing the number of inductor turns scales L by N^2, but it only scales R_{par} by N. So according to (7.36), increasing N will increase Q_{series} by $N^2/N = N$, this is in good accordance with (7.20) and (7.25) which shows that

the $\vec{B}$ field and energy per per volume from the transmitter will both be increased by increasing N.

For the receiving antenna, the laboratory observations were that increasing N reduced efficiency. With the secondary side's parallel configuration and a load resistance determined by the implant electronics (the inductor series resistance was considered negligible in the parallel configuration), (7.41) shows that under constant load, because L scales with N^2, increasing N will decrease Q_{parallel} by $1/N^2$. This is in good accordance with (7.27), which shows that, assuming that the transmitter's $\vec{B}$ field generation remains constant, increasing the number of solenoid turns increases the flux which increases the voltage potential across the load which increases the power loss across R_{load} as a function of V^2.

8

Wireless Data Reception

When the implant is activated, the power supply electronics power up while the rest of the chip remains in a powered down state. There are no CDC conversions taking place, and the data transmission circuits are powered down. This allows the energy harvesting electronics to reach a steady state of charge storage in the energy storage capacitors before powering up the various digital and analog blocks. At power up, the only block which is active is the wireless data reception block, given in Fig. 8.1.

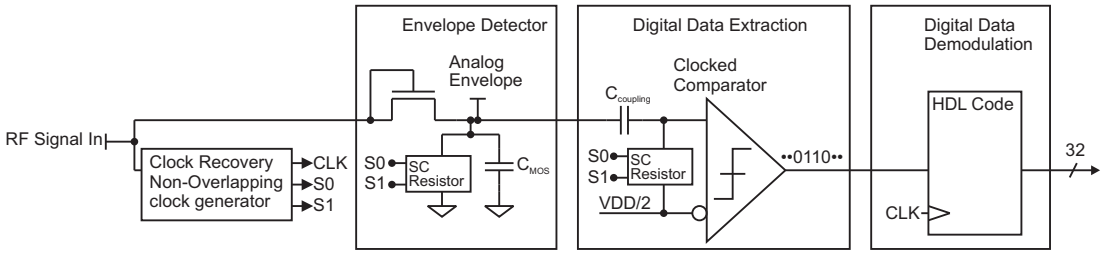


Figure 8.1: The block diagram of the wireless data RX electronics.

8.1 Wireless RX Electronics

The wireless data RX block cannot be disabled because it is only through the wireless interface that the rest of the implant can be powered up and configured. After the base station starts transmitting power, the implant is given a couple of seconds to charge its energy harvester storage capacitors. After this start up period, the base station begins transmitting configuration data, and the implant starts demodulating the incoming data. Even though the RX electronics are always active, they can be built using very

low power circuits because the performance requirements of the RX system are relatively relaxed. Data transmission from base station to implant does not occur very often, so the data rate is allowed to be very slow. The only blocks required for effective data demodulation are the envelope detector, which extracts the analog AM envelope from the AM carrier, the clocked comparator, which extracts the digital 1's and 0's from the analog envelope, and the digital data demodulation block which extracts the bytewise data from the digital stream of 1's and 0's.

The data demodulation clock is extracted directly from the power sender's RF frequency, and this results in 100% coherence of the data sender's clock and the data RX clock. This greatly simplifies the data demodulation because all of the data RX blocks can be designed to extract the data as a function of the number of clock cycles rather than as a function of frequency. The implant data RX electronics have been designed to demodulate data from a wide range of RF power carriers. This is accomplished by setting the baud rate to carrier frequency at a constant ratio, and then making the data demodulation electronics demodulate the AM signal as a function of the RF carrier frequency, which might be different from one system to the other, rather than against a static reference frequency.

8.1.1 Envelope Detection

The data transmission signal from the base station to the implant is coupled directly onto the RF power transmission carrier using AM modulation. An AM modulated signal, (8.1), is the carrier $c(t)$, (8.2), plus the product of the message $m(t)$ and the carrier, (8.3). The result is a carrier wave which is amplitude modulated by the message (8.4).

$$x(t) = c(t) + c(t)m(t) \tag{8.1}$$

$$c(t) = A_c sin(\omega_c t + \phi_c) \tag{8.2}$$

$$m(t) = A_m cos(\omega_m t + \phi_m) \tag{8.3}$$

$$x(t) = A_c sin(\omega_c t + \phi_c) + A_c A_m \left[sin(\omega_c t + \phi_c) cos(\omega_m t + \phi_m)\right] \tag{8.4}$$

Setting the carrier and message initial offset phase, $\phi_{c,m}$, to zero, and applying a product to sum trigonometric identity to (8.4) results in (8.5).

$$x(t) = A_c sin(\omega_c t) + \frac{A_c A_m}{2} \left[sin(\omega_c t + \omega_m t) + sin(\omega_c t - \omega_m t)\right] \tag{8.5}$$

The AM signal in (8.5) is the sum of three signals. One is the constant energy carrier, and the other two signals are the products of $A_c A_m$ at the two sideband frequencies of $\omega_c + \omega_m$ and $\omega_c - \omega_m$.

The amount of signal energy depends on the amount of RF carrier power which is available, and how great the modulation amplitude is. The RF signal is, by default, a very high energy signal, or else there would not be enough energy content to power the implant. And, if necessary, the modulation depth can be made very large. This means that the signal to noise ratio of the received data transmission can be large enough (it can essentially be as large as the designer wants it to be) that there is no need for any on chip active electronics for signal amplification. The circuit which the implant uses to extract the analog message data from the RF power transmission wave is given in Fig. 8.2.

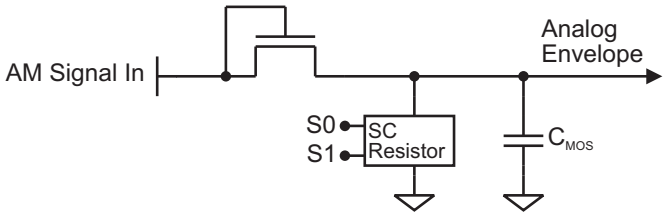


Figure 8.2: The RX electronics envelope detector circuit.

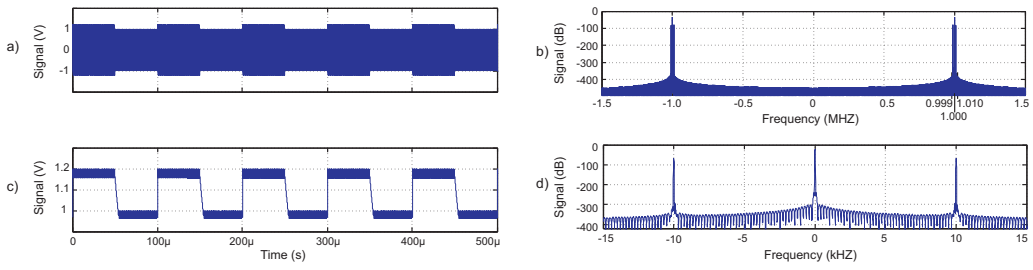


Figure 8.3: Envelope detection of an AM modulated signal.
(a) The AM modulated signal with $\omega_c = 1$MHz and $\omega_m = 1$kHz.
(b) The FFT analysis of the AM signal.
(c) The time space signal from the envelope detector.
(d) The FFT analysis of the envelope detector output.

The envelope detector is a simple diode connected MOSFET forming a peak detector with a decay time constant $\tau = R_{sc} C_{\text{MOS}}$. The capacitor, C_{MOS}, is a thick-oxide MOS

capacitor for reduced gate leakage, and the resistor is a switched capacitor resistor R_{sc}. The switched capacitor resistor, R_{sc}, is a circuit made up of two non-overlapping switches, S0 and S1, and a capacitor C_{sc} Fig. 8.4. The main idea is that when switch S0 is closed, C_{sc} gets loaded with charge $Q = V_0 C_{sc}$, and when S1 is closed, C_{sc} gets loaded with $Q = V_1 C_{sc}$ worth of charge. The total charge flow from V0 to V1 is $\Delta Q = \Delta V C_{sc}$ per S0→S1 cycle, and the resulting effective resistance is (8.6).

$$\frac{dQ}{dt} = \Delta V C_{sc} f_{sc} = I$$

$$\frac{\Delta V}{I} = \frac{(V_0 - V_1)}{(V_0 - V_1) C_{sc} f_{sc}} = R$$

$$R_{sc} = \frac{1}{C_{sc} f_{sc}} \tag{8.6}$$

The envelope detector cutoff frequency, f_{env}, is (8.7).

$$f_{3_{\mathrm{dB}}} = \frac{1}{2\pi R_{sc} C_{\mathrm{MOS}}}$$

$$f_{env} = \frac{f_{sc}}{2\pi} \left(\frac{C_{sc}}{C_{\mathrm{MOS}}} \right) \tag{8.7}$$

The SC resistor switching frequency is equal to the RF carrier frequency, $f_{sc} = f_{\mathrm{RF}}$, and if the message frequency, $f_{message}$, is some constant ratio for the carrier, here this carrier to message frequency ratio is called $k_{message}$, then the envelope detector cutoff frequency, f_{env}, can also be made some constant ratio, here it is called k_{env}, of the carrier. For envelope detection, the detector's f_{env} should be greater than the message's $f_{message}$, and less than the carrier's f_{RF}. The general idea is that the envelope detector cutoff frequency needs to be situated between the message and the carrier frequency, and the further away from both, the better (8.9).

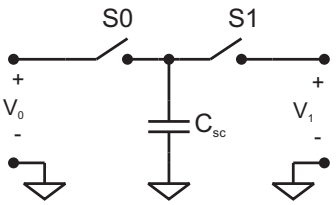


Figure 8.4: The switched capacitor resistor.

$$k_{message} = \frac{f_{message}}{f_{sc}}$$

$$k_{env} = \frac{f_{env}}{f_{sc}} \tag{8.8}$$

$$k_{message} < k_{env} < 1 \tag{8.9}$$

Choosing to give the envelope bandwidth twice the value of the message bandwidth

$$k_{env} = 2k_{message},$$

and substituting this value into (8.7) and (8.8) results in a value for setting the capacitor ratios according to the message bandwidth (8.10).

$$4\pi k_{message} = \left(\frac{C_{sc}}{C_{\text{MOS}}}\right) \tag{8.10}$$

According to (8.6), the smaller C_{sc} is, the greater the resistance, and according to (8.10), the smaller the C_{sc}, the smaller C_{MOS} needs to be. So, choosing the smallest available metal capacitor, choosing a value for k_{env} which fulfills (8.9), and rearranging (8.10) to solve for C_{MOS}, (8.11), will deliver an envelope detector with a cutoff frequency which is tuned by the AM carrier frequency.

$$C_{\text{MOS}} = \frac{C_{sc}}{4\pi k_{message}} \tag{8.11}$$

The risk associated with picking the smallest valued C_{sc} possible is the inaccuracy of the exact value of capacitance at the very small level. However, the data RX packet will have a carrier frequency which is 1024x as fast as the message carrier. This wide separation, and the strong signal coupling from sender to receiver will allow a fairly significant amount of mismatch without interfering too much with the data demodulation.

Fig. 8.5 shows the measured output signal from the envelope detector for a 1 MHz RF carrier modulated with a data bit pattern which is 1024x slower than the carrier.

8.1.2 The Clocked Comparator

The analog output of the envelope detector message signal is the large DC value of the high frequency AM carrier plus the AC signal of the lower frequency message data. The DC value will be about the same value as the rectified output voltage of the energy harvester, which should be quite a bit greater than the regulated 1.2 VDC core voltage which is the supply voltage of the clocked comparator. It would be possible to construct

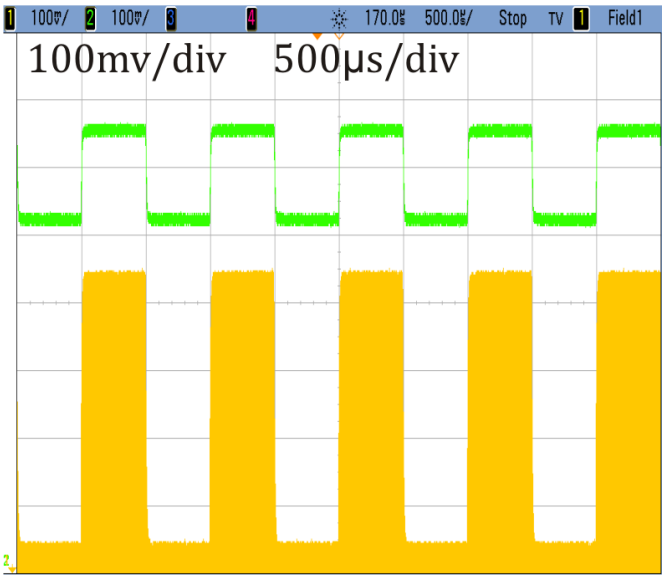


Figure 8.5: The measured waveform of the implant IC demodulating the AM modulated RF power carrier.

the comparator out of thick gate oxide devices, but the comparator itself is driving core logic blocks which are only available for 1.2 VDC supply voltage. The solution is fairly simple, and that is to remove the DC component from the signal, by configuring the comparator with a simple differentiator input.

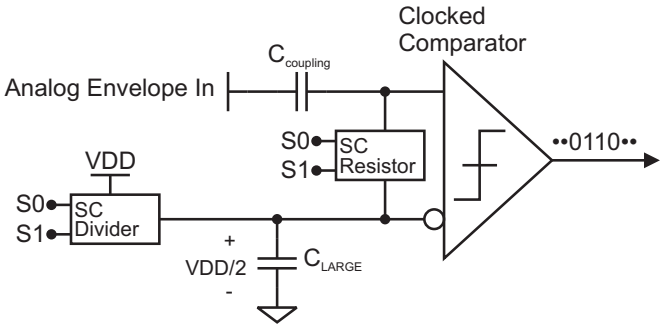


Figure 8.6: The RX signal clocked comparator with differentiating inputs.

The comparator in Fig. 8.6 is the same StrongARM comparator that was used for the ADC, but here it has a very low power differentiating input circuit. For the virtual ground, the SC divider takes the 1.2 VDC supply voltage and divides it down by 2 to 0.6 VDC. An SC divider has been chosen over a couple of SC resistors in a resistor

divider circuit because, except for the dynamic power consumption of the switches, an SC divider has no DC path to ground. The schematic for the SC divider is given in Fig. 8.7, and it shows how during phase S0, the capacitors are switched in a series configuration with $Q_1C_1 + Q_2C_2 = V_{\text{in}}$, and during phase S1 the capacitors are in parallel $(C_1+C_2)(Q_1+Q_2) = V_{\text{out}}$. This action essentially moves charge back and forth between V_{in} and V_{out} in an attempt to keep $V_{\text{out}} = V_{\text{in}}/2$ without sinking any of that charge to ground.

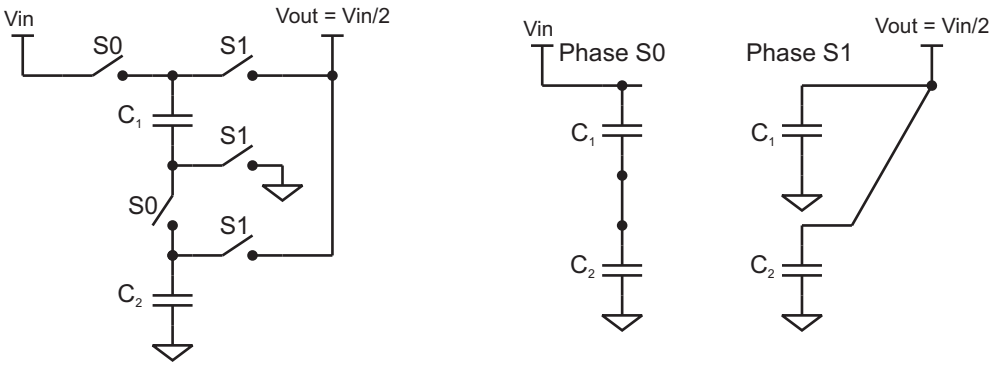


Figure 8.7: The schematic of the SC capacitive divider circuit.

The virtual ground output of the SC divider has a time constant from the effective resistance of the SC divider and the decoupling capacitance. Similar to the SC resistor, the effective resistance of the divider is a function of the charge movement across a potential drop per unit of time. The effective resistance of the SC divider is

$$\begin{aligned} Q_{\text{S0}} &= \frac{V_{in}}{2}C_1 + \frac{V_{in}}{2}C_2 \\ Q_{\text{S1}} &= V_{out}(C_1 + C_2) \\ \Delta Q &= \frac{V_{in}}{2}(C_1 + C_2) - V_{out}(C_1 + C_2) \end{aligned} \tag{8.12}$$

Assuming that $C_1 = C_2 = C_{sc}$, and substituting in $V_{out} = xV_{in}$

$$\begin{aligned} \Delta Q &= \frac{V_{in}}{2}(2C_{sc}) - V_{in}x(2C_{sc}) \\ \frac{\Delta Q}{dt} &= V_{in}\left(C_{sc} - 2xC_{sc}\right)f_{sc} \\ R &= \frac{1}{(1-2x)C_{sc}f_{sc}} \end{aligned} \tag{8.13}$$

Eq. (8.13) shows that the resistance is very similar to the SC resistor resistance (8.6), except that it is now also a function of the ratio of the output voltage against the input voltage. At $V_{out}/V_{in} = 0$, $1/2$, and 1, the resistance of the circuit is $1/(C_{sc}f_{sc})$, ∞, and $-1/(C_{sc}f_{sc})$, respectively. Luckily, because the device does not have any DC path to ground, there is no severe penalty for using large valued capacitors for C_{sc} which helps to keep the response time quick.

If the detector output will be compared against this virtual ground, then it is not enough to simply place the virtual ground on one of the comparator inputs, and the envelope detector output on the other comparator input. The virtual ground potential needs to be applied as a DC bias to the input signal from the envelope detector. This is accomplished by placing an SC resistor from virtual ground to the envelope detector node. The time constant at the comparator envelope input node is set by the AC coupling (DC decoupling) capacitor and the SC resistor. The data modulation from the sender to the receiver is performed using a Manchester encoded bit pattern. This means that the lowest frequency component of the data signal is at the same frequency as a single bit. The differentiation circuit is tuned to give a high pass cutoff at $1/4$ the baud rate. This gives a differentiator cutoff frequency, f_d, of

$$f_d = \frac{k_{message} f_{sc}}{4},$$

and just like the $f_{3_{\mathrm{dB}}}$ cutoff frequency for the envelope detector, (8.7), the time constant for the differentiator input is a function of the ratio of the coupling capacitor and the SC resistor capacitor. The ratio of the two capacitors can be calculated as the ratio of the switching frequency and the desired cutoff frequency (8.14).

$$\frac{\pi k_{message}}{2} = \frac{C_{sc}}{C_{coupling}} \tag{8.14}$$

Eqs. (8.10) and (8.14) show that by setting the message frequency and the carrier frequency at fixed ratios of each other, $k_{message}$, the capacitors of the data demodulation electronics can be sized in a way that it doesn't matter what carrier frequency is used so long as the ratio of RF carrier to message frequency stays the same.

8.1.3 Digital Data Demodulation

The digital data demodulator clocks in the decisions from the comparator and begins a search routine for the data packet. The requirements on the digital data demodulation

are pretty relaxed because there is no need to have a particularly fast data rate. Because the uplink from the base station to the implant only needs to send a few bytes of data just once on initialization, even data rates as low as just a few bits per second would be tolerable. The data bits from the base station to the implant are Manchester encoded [46] data bits, and the digital demodulation synchronizes itself with the data bit on every mid-bit logical transition (Fig. 8.8). Every bit of the Manchester coded data has at least one transition, marked with the arrows in Fig. 8.8. This midpoint transition is given the name "read_edge" in the software demodulation flow chart in Fig. 8.10. If the read_edge is a rising edge, then the data bit is 1'b1, and a falling edge means the data bit is 1'b0.

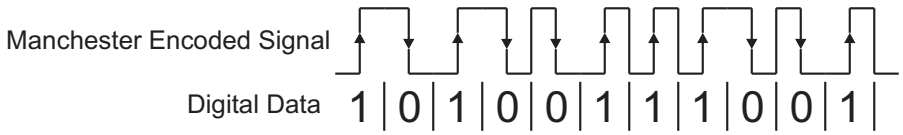


Figure 8.8: The RX data bit is Manchester encoded as per the IEEE 802.3 standard, and the digital demodulation synchronizes itself with the data bit on every mid-bit logical transition.

Fig. 8.9 shows the format of the RX data packet. It begins with a synchronization preamble which is a long stream of zeros, followed by a a 48 bit start of frame (SOF). After the SOF comes 4 data bytes and a 16 bit cyclic redundancy check (CRC) word. The data stream is continuously sampled, and as soon as a valid SOF and CRC are shifted into the RX read data buffer, called "dbuf" in the flow chart, then the IC_control registers are updated with the data packet.

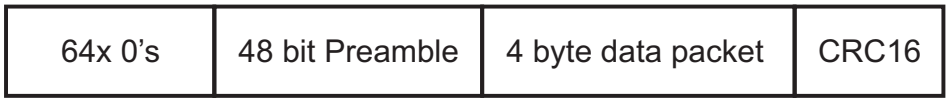


Figure 8.9: The RX data packet.

The flow chart in Fig. 8.10 shows the process used to extract the data packet from

the stream of 1's and 0's. The system oversamples each data bit by OS = 32, giving it a sampling bandwidth 16x the data baud rate. One note, in the flow chart, every increment or assignment is performed using a blocking statement, and does not occur until the next rising edge of the clock.

1. The clocked comparator decisions are clocked in with a rising clock edge
2. The period counter, PCNT, which keeps track of how many clock cycle occur between the edge transitions of din, is incremented.
3. If this sample is not a glitch, proceed with the demodulation. Glitches are detected by the presence of a single sample not being equal to the two adjacent sample such as 3'b010 or 3'b101.
4. If the 48 MSBs of the data receive buffer, dbuf, are equal to the SOF, then:
   - The synchronization counter, syncCNT, is cleared to zero, and the CRC16 is verified.
   - If the CRC fails, then drop the packet and restart. If the CRC is good, then either load the IC_control registers with the data packet, or transmit the contents of the IC_control words to the base station.
5. Shift the comparator decision into the edge detect shift register to decide if the data stream has experienced a rising or falling edge, or if it is between edge transitions.
   - A rising edge transition, $\uparrow = 1$, is 2b'01, and a falling edge, $\downarrow = 1$, is 2b'10.
6. If an edge transition has occurred, then clear PCNT to zero, (this is a blocking statement and PCNT retains its current value until the next rising edge) and handle the up or down transition.
7. If the routine is not synchronized with the initial string of 0's then:
   - Clear the RX data buffer and update read_edge and syncCNT according PCNT and the edge transition direction.
   - The routine is synchronized as soon as the syncCNT has counted up to 31.

8. If the routine is already synchronized to the initial string of 0's, test PCNT and force a restart if PCNT is out of its valid range.

9. If PCNT is the size of a whole bit period, then this edge must be a read_edge, so load din into the RX data buffer, and clear read_edge to zero.

10. If PCNT is too small for a whole bit period, determine, based on the value of read_edge, if this transition belongs to the beginning or middle of the bit. If this is a mid-bit transition, then load the data bit value into the RX data buffer and toggle the value of read_edge.

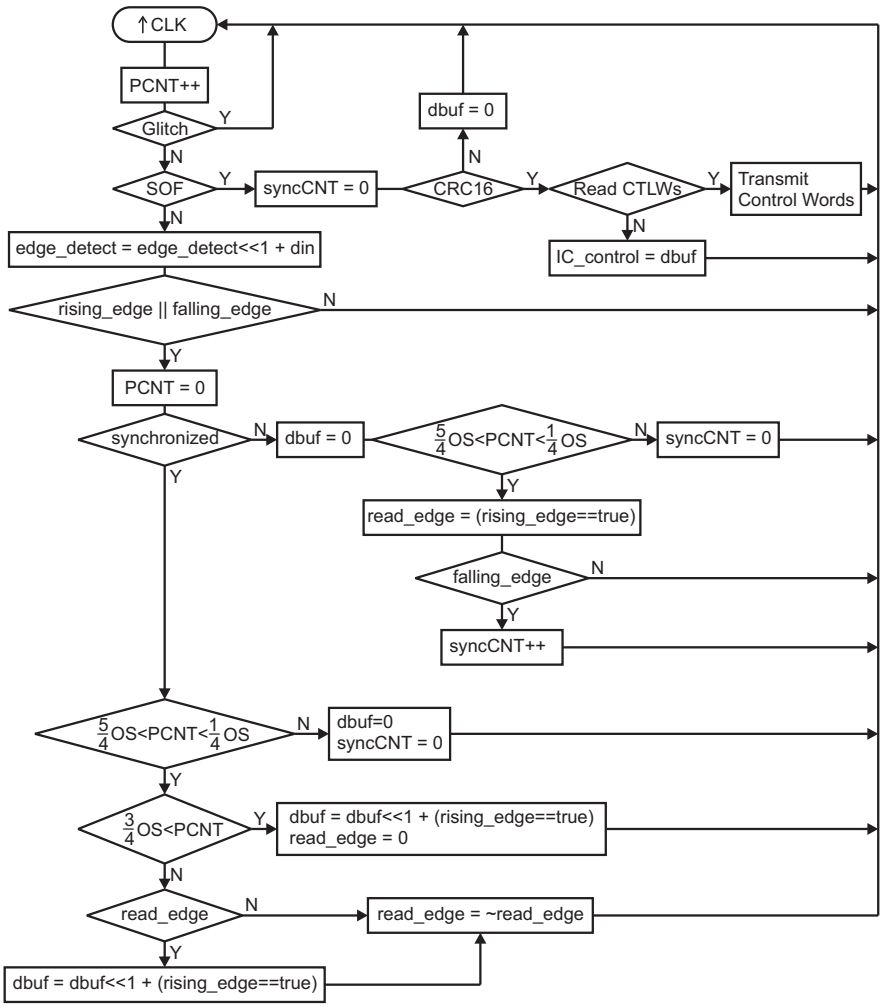


Figure 8.10: The digital demodulation flow chart.

The synchronization string of 0's is only there to let the comparator's differentiator circuit reach an equilibrium bias potential, and to synchronize the digital data demodulation routine with the bit's middle edge transition. The dbuf register will keep shifting in one bit after the other until the 48 MSBs of the 96 bit shifter are equal to the SOF, at which point it will force a demodulation routine reset by clearing syncCNT, check the CRC, and update the control registers if needed. Also, the base station can force a reset on the implant's RX circuit at will by transmitting a bit which has two edge transitions which are either too close together or too far apart.

The combination of the 48 bit SOF and the 16 bit CRC gives very robust protection against random writes to the register as a function of noise. The system automatically rejects bits which don't fit the baud rate of the AM signal, and even at a bit period of 1µs, it would take 8 years to go through every possible SOF combination. If the SOF is randomly triggered by noise, then it would also be necessary for the CRC to be correct for the control register to be updated with the erroneous information. As soon as a data packet is loaded into the IC control register, the chip will power up and start operation. The first indication to the base station that the data has been received is that the implant will become active and start transmitting conversion data, but the base station can also issue a command to read the device configuration register settings.

8.1.4 The Implant Configuration Registers

There are only a few device settings which need to be configured for the chip to operate. The control word 1, CTLW1, is made up of the 16 MSBs of the 32 bit IC control register, and it handles the data transmission system control register settings. The control word 2, CTLW2, handles the digital and analog systems. The register settings are held in volatile memory, and they are cleared to zero on every power on cycle. This means that as the implant's energy harvesting electronics are powered up, all of the systems which are controlled by the IC_control register are held in power down mode until the base station has issued the command for them to begin operation.

9

Wireless Data Transmission

The implant's data transmission electronics have been designed for very flexible output frequency selection. For some applications, the implant implementation will only need one or two sensors operating with a fairy low effective sample rate. In this situation, the transmitter can be programmed to use a lower data rate which allows for a lower data carrier frequency which can greatly reduce the transmitter power consumption. On the other hand, if the implant has all 128 sensors sampling at their full 4 ksps at 10 bits per sample, then the minimum data rate in this configuration is 5.12 Mbps, which would require a high frequency RF data carrier with a wide channel bandwidth.

Different country regions have different requirements on carrier frequencies, bandwidths, transmission power, and channel agility [1, 2]. To handle all of these different requirements would not only take up a lot of chip area on the implant's IC, it would also require quite a bit of extra power. To keep the operation and flexibility high, the base station performs all of the computationally intensive operations, such as listen before talk (LBT) and adaptive frequency agility (AFA). The implant uses an integer-N PLL (phase locked loop) to generate a 8-PSK (phase shift keying) modulated RF carrier frequency, and the reference for the PLL is the RF power carrier generated by the external base station.

This chapter will cover the design of the wireless data transmission system with special attention given to PLL loop stability and meeting the link transmission noise requirements while consuming as little power as possible.

9.1 The Phase Locked Loop

A PLL does exactly what its name suggests, it takes a reference phase, and it locks a second phase, the PLL's output, to the input reference. If the output phase is divided down by the integer value N, then the output phase would be N times as great as the input phase

$$\phi_{out} = N\phi_{ref},$$

and because frequency is the time derivative of phase, the input to output frequency ratio of the integer-N PLL is (9.1).

$$\begin{aligned} \frac{\partial \phi_{out}}{\partial t} &= N\frac{\partial \phi_{ref}}{\partial t} \\ \omega_{out} &= N\omega_{ref} \end{aligned} \tag{9.1}$$

Generating a stable, clean phase reference can be fairly power intensive. Luckily, the reference is generated externally by the base station, which, for all intents and purposes, has an unlimited power source. The power amplifier of the base station power transmitter is a crystal referenced, low jitter PLL, which is then further cleaned up by the band pass characteristics of the class E power amplifier's resonant tuned network and the high Q antenna. Because the PA can source a finely tuned, high resolution reference, the implant's PLL does not need very fine resolution for its divide by N feedback. Using the base station to generate the reference allows the implant to be able to step across very narrowly spaced RF spectrum channels even though its PLL is a simple integer-N divider with a relatively small (N=4 to 512) maximum divide ratio.

The desired operational flexibility of the PLL cause the requirements placed on its operation to be fairly complex. In a typical cellular phone or wifi modem, the system is built with the intent of taking a fixed reference and multiplying it up to a relatively constant output frequency. In the case of a wifi modem, the output frequency might only range from 2.4 to 2.5 GHz, or about a 5% output range, and its reference is a crystal oscillator with a good low phase noise oscillation frequency. In contrast, this implant has been designed to be able to operate at any of the various allowed ISM bands between 400 MHz and 1 GHz [1, 2] using a 2, 4, 8 or 16 MHz reference frequency. To ensure stability across this wide range of operating conditions, the PLL employs self biasing techniques [47, 48] so that it can dynamically adjust its feedback loop stability coefficients as necessary according to the N divider and the reference frequency.

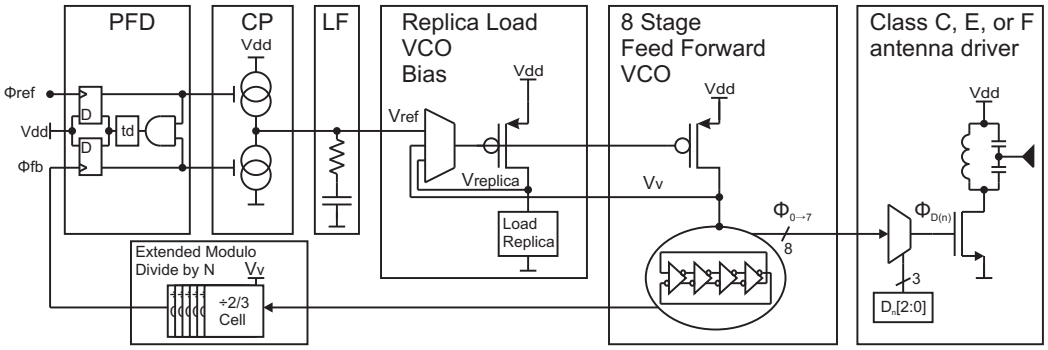


Figure 9.1: The PLL circuit diagram

The PLL circuit is given in Fig. 9.1. It uses a dual D Flip-Flop phase frequency detector (PFD) to drive a charge pump to sink or source current into a series RC loop filter load. The voltage across the loop filter is used as a reference voltage for the replica load VCO supply voltage regulator. The VCO is a phase forwarded 8 stage differential ring oscillator which generates the 8-PSK output modulation. The divide by N circuit is a low power, high speed circuit which can divide the output phase into integer divide ratios of 4 to 512, and the divide by N output is the feedback phase signal to the PFD input.

There are many different design considerations to be taken into account for the PLL, and one of the most significant is the PLL transfer function stability characteristics. The circuit in Fig. 9.1 has two poles (a third pole if you include the regulator) and feed forward gain which will make the loop unstable if the proper precautions are not taken. For the PLL loop transfer function derivation, the pole from the voltage regulator will, for now, be ignored with the assumption that when it is designed it will be given a bandwidth much greater than the bandwidth of the loop filter so that its output pole will not disrupt the normal loop behavior of the PLL. If it should become evident that the regulator cannot be made fast enough, there are methods for removing the regulator from the feed forward path [49].

A block diagram representation of the PLL circuit is given in Fig. 9.2, and this block diagram will be used to derive the PLL transfer function.

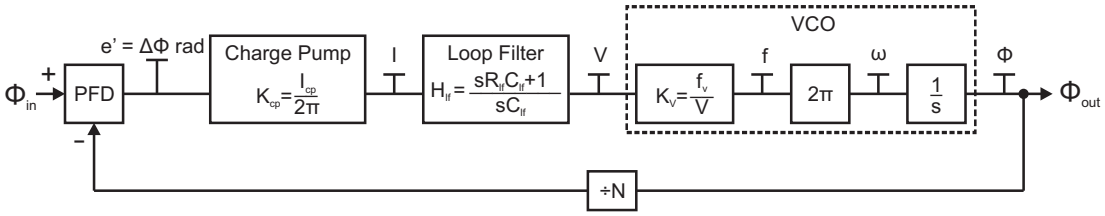


Figure 9.2: The PLL block diagram

The PLL transfer function can be derived as follows.

$$
\begin{aligned}
G(s) &= K_{\mathrm{cp}} H_{\mathrm{lf}} \frac{K_{\mathrm{v}} 2\pi}{s} \\
\Phi_{\mathrm{out}} &= e' G(s) \\
e' &= \Phi_{\mathrm{ref}} - \frac{\Phi_{\mathrm{out}}}{N_{\mathrm{div}}} \\
\Phi_{\mathrm{out}} &= \left(\Phi_{\mathrm{ref}} - \frac{\Phi_{\mathrm{out}}}{N_{\mathrm{div}}} \right) G(s) \\
\frac{\Phi_{\mathrm{out}}}{\Phi_{\mathrm{ref}}} &= \frac{G(s)}{1 + \frac{G(s)}{N_{\mathrm{div}}}} \\
H(s) &= N_{\mathrm{div}} \left(\frac{G(s)}{N_{\mathrm{div}} + G(s)} \right)
\end{aligned}
$$

Substituting $G(s) = K_{\mathrm{cp}} H_{\mathrm{lf}} K_{\mathrm{v}} 2\pi / s$, $K_{\mathrm{CP}} = I_{\mathrm{cp}} / 2\pi$, and $H_{\mathrm{lf}} = (sR_{\mathrm{lf}} C_{\mathrm{lf}} + 1)/sC_{\mathrm{lf}}$, gives the transfer function for the 2^{nd} order PLL loop (9.2).

$$
H(s) = N_{\mathrm{div}} \left(\frac{\left(\frac{I_{\mathrm{cp}}}{2\pi}\right) \left(\frac{1+sR_{\mathrm{lf}}C_{\mathrm{lf}}}{sC_{\mathrm{lf}}}\right) \left(\frac{K_{\mathrm{v}}2\pi}{s}\right)}{N_{\mathrm{div}} + \left(\frac{I_{\mathrm{cp}}}{2\pi}\right) \left(\frac{1+sR_{\mathrm{lf}}C_{\mathrm{lf}}}{sC_{\mathrm{lf}}}\right) \left(\frac{K_{\mathrm{v}}2\pi}{s}\right)} \right)
$$

$$
H(s) = N_{\mathrm{div}} \left(\frac{(1 + sR_{\mathrm{lf}}C_{\mathrm{lf}}) \left(\frac{I_{\mathrm{cp}} K_{\mathrm{v}}}{s^2 C_{\mathrm{lf}}}\right)}{N_{\mathrm{div}} + (1 + sR_{\mathrm{lf}}C_{\mathrm{lf}}) \left(\frac{I_{\mathrm{cp}} K_{\mathrm{v}}}{s^2 C_{\mathrm{lf}}}\right)} \right)
$$

$$
H(s) = N_{\mathrm{div}} \left(\frac{1 + sR_{\mathrm{lf}}C_{\mathrm{lf}}}{s^2 \left(\frac{C_{\mathrm{lf}} N_{\mathrm{div}}}{I_{\mathrm{cp}} K_{\mathrm{v}}}\right) + sR_{\mathrm{lf}}C_{\mathrm{lf}} + 1} \right) \tag{9.2}
$$

The PLL transfer function is a 2^{nd} order transfer function with 2 poles and 1 zero. It is often helpful to represent a 2^{nd} order transfer functions in its standard form

$$
H(s) = N_{\mathrm{div}} \left(\frac{1 + 2\zeta \frac{s}{\omega_n}}{\frac{s^2}{\omega_n^2} + 2\zeta \frac{s}{\omega_n} + 1} \right),
$$

where ω_n is the natural frequency of the loop, and ζ is the damping factor. Equating the derived transfer function (9.2) with the standard form results in values for ω_n and ζ which are functions of the PLL design variables.

$$\omega_n = \sqrt{\frac{I_{\text{cp}} K_{\text{v}}}{N_{\text{div}} C_{\text{lf}}}} \tag{9.3}$$

$$\frac{2\zeta}{\omega_n} = R_{\text{lf}} C_{\text{lf}}$$

$$\zeta = \frac{\omega_n}{2} R_{\text{lf}} C_{\text{lf}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{I_{\text{cp}} K_{\text{v}} R_{\text{lf}}^2 C_{\text{lf}}}{N_{\text{div}}}} \tag{9.4}$$

The loop bandwidth, ω_n as given in (9.3), assumes that the system is a linear time continuous function, but the reality is that the PLL loop is a discrete time system. It is a discrete time system because of the sampling action performed by the phase detector and charge pump. The phase detector and charge pump only perform phase error corrections on the rising edge of the reference or feedback clock. If the loop bandwidth had the same frequency as the reference clock, then, even if the phase error only required a tiny nudge for correction, the PFD could spend the whole clock period sourcing current to the loop filter before the next rising edge when it would learn that it has greatly overshot the necessary correction value. To smooth out the discrete nature of the error sampling, the loop bandwidth is designed to be only a small fraction of the reference frequency (usually less than 1/10). For loop stability, the system zero, $\omega_n/2\zeta$, is set equal to one half the loop bandwidth, or simply $\zeta = 1$.

The task at hand is to design the loop feedback system so that (9.3) and (9.4) are constant across a wide range of ω_{ref} and N_{div}. This is accomplished using the self biasing techniques proposed in [47, 48].

9.1.1 The Self Biased ω_n

The purpose of self biasing the PLL is to ensure that as the reference frequency and/or the divide ratio are changed, the loop bandwidth ω_n and the damping ratio ζ will automatically track these changes.

To have a constant loop bandwidth to reference frequency ratio, (9.3) needs to be manipulated in such a way that it will be linearly proportional to the reference frequency.

Looking at (9.3), K_{v} and C_{lf} will be design constants, and N_{div} is a design constraint. The remaining variable which will be used for self biasing the PLL is I_{cp}.

In CMOS design, it is relatively easy to design currents to be proportional to other currents. Because the PLL's VCO frequency is, by definition, proportional to the reference frequency, and the VCO drive current is proportional to the VCO frequency, then the VCO current is a natural choice for selecting a biasing reference which is proportional to ω_{ref}.

This self biasing technique is based upon the idea that making the charge pump current proportional to the VCO current will cause the PLL loop bandwidth to scale proportionally with the reference clock frequency. This will have the end effect that ω_n/ω_{ref} will always be a fixed ratio.

To begin with, the charge pump current, I_{CP}, is given a scaling variable N_{cp} which is used to scale it to the VCO current I_{v}

$$I_{\mathrm{cp}} = N_{\mathrm{cp}} I_{\mathrm{v}}.$$

Using this proportionality variable, the loop bandwidth is now

$$\omega_n = \sqrt{\frac{N_{\mathrm{cp}}}{N_{\mathrm{div}} C_{\mathrm{lf}}}} \sqrt{I_{\mathrm{v}} K_{\mathrm{v}}}. \tag{9.5}$$

Now, if it can be shown that the term $\sqrt{I_{\mathrm{v}} K_{\mathrm{v}}}$ is linearly proportional to the reference frequency, then the requirements for self biasing will be fulfilled. For this derivation, the following MOSFET drain current, transconductance, and delay time to ring oscillator frequency conventions are followed.

$$\begin{aligned} I_d &= k' V_{ov}^2 \\ k' &= \frac{\mu_0 C_{\mathrm{ox}}}{2} \frac{W}{L} \\ V_{ov}^2 &= (V_{gs} - V_{th}) \end{aligned} \qquad \begin{aligned} gm &= \frac{dI_d}{dV_{ov}} \\ gm &= 2k' V_{ov} \\ gm &= 2\sqrt{k'(k' V_{ov}^2)} \\ gm &= 2\sqrt{k' I_d} \end{aligned} \qquad \begin{aligned} t_d &= \frac{C_{\mathrm{v}}}{gm} \\ f_{\mathrm{v}} &= \frac{1}{2t_d} \\ f_{\mathrm{v}} &= \frac{gm}{2C_{\mathrm{v}}} \end{aligned}$$

The first column gives the characteristic MOSFET I_d behavior, the middle column gives a few different formulas for gm based on the V_{ov} overdrive voltage derivative of I_d, and the third column gives the VCO frequency as a function of the total inverter ring propagation delay which itself is a function of the device gm and total ring capacitance.

From these equations, two important formulas can be derived by substituting either $gm = 2k'V_{ov}$ or $gm = 2\sqrt{k'I_d}$ into $f_\mathrm{v} = gm/(2C_\mathrm{v})$. One formula equates the VCO frequency to the VCO drive current (9.6), and the other formula equates the VCO frequency to the overdrive voltage (9.7).

$$f_\mathrm{v} = \frac{\sqrt{k'I_\mathrm{v}}}{C_\mathrm{v}} \tag{9.6}$$

$$f_\mathrm{v} = \frac{k'V_{ov}}{C_\mathrm{v}} \tag{9.7}$$

For the ring oscillator, if the VCO supply voltage is taken as being the gate drive voltage $V_\mathrm{v} = V_{gs}$, this would mean that

$$d(V_\mathrm{v}) = d(V_\mathrm{v} - V_{th}) = d(V_{ov}).$$

With this identity, (9.6) can manipulated to solve I_v as a function of the VCO frequency and the VCO capacitance and manufacturing constant C_v and k' (9.8).

$$\sqrt{I_\mathrm{v}} = \frac{f_\mathrm{v}C_\mathrm{v}}{\sqrt{k'}} \tag{9.8}$$

Eq. (9.7) can be manipulated to solve for K_v, where K_v is the change in VCO output frequency per change in control voltage, as a function of k' and C_v (9.9).

$$\begin{aligned}\sqrt{K_\mathrm{v}} &= \sqrt{\frac{df_\mathrm{v}}{dV_{ov}}} \\ \sqrt{K_\mathrm{v}} &= \sqrt{\frac{d}{dV_{ov}}\left(\frac{k'V_{ov}}{C_\mathrm{v}}\right)} \\ \sqrt{K_\mathrm{v}} &= \sqrt{\frac{k'}{C_\mathrm{v}}}\end{aligned} \tag{9.9}$$

Combining (9.5), (9.8), and (9.9) will result in a function for the ratio of the loop bandwidth to the reference frequency (9.11).

$$\sqrt{I_\mathrm{v}K_\mathrm{v}} = \frac{f_\mathrm{v}C_\mathrm{v}}{\sqrt{k'}}\sqrt{\frac{k'}{C_\mathrm{v}}}$$

$$\sqrt{I_\mathrm{v}K_\mathrm{v}} = f_\mathrm{v}\sqrt{C_\mathrm{v}}$$

$$\omega_n = \sqrt{\frac{N_\mathrm{cp}}{N_\mathrm{div}C_\mathrm{lf}}}\, f_\mathrm{v}\sqrt{C_\mathrm{v}} \tag{9.10}$$

$$f_{\mathrm{v}} = N_{\mathrm{div}} \frac{\omega_{ref}}{2\pi}$$

$$\omega_n = \sqrt{\frac{N_{\mathrm{cp}}}{N_{\mathrm{div}} C_{\mathrm{lf}}}} N_{\mathrm{div}} \frac{\omega_{ref}}{2\pi} \sqrt{C_{\mathrm{v}}}$$

$$\omega_n = \frac{\omega_{ref}}{2\pi} \sqrt{\frac{C_{\mathrm{v}}}{C_{\mathrm{lf}}}} \sqrt{N_{\mathrm{div}} N_{\mathrm{cp}}}$$

$$\frac{\omega_n}{\omega_{ref}} = \frac{1}{2\pi} \sqrt{\frac{C_{\mathrm{v}}}{C_{\mathrm{lf}}}} \sqrt{N_{\mathrm{div}} N_{\mathrm{cp}}} \tag{9.11}$$

The result of the ω_n/ω_{ref} derivation is a function, (9.11), which shows that the loop bandwidth is proportional to the reference frequency as a function of a constant, $1/2\pi$, a ratio of design capacitances, C_{v} and C_{lf}, and the product of the PLL divider and N_{cp}.

The solution of (9.11) will keep the loop stable as the reference frequency changes, but the right hand side of the equation still has the design factor N_{div} which can change according to the desired output frequency. If the PLL divider, N_{div}, and the charge pump divider, N_{cp}, are made inversely proportional to each other with the scaling factor α

$$N_{\mathrm{cp}} = \frac{\alpha}{N_{\mathrm{div}}}, \tag{9.12}$$

then, substituting (9.12) into (9.11), will result in (9.13).

$$\frac{\omega_n}{\omega_{ref}} = \frac{\sqrt{\alpha}}{2\pi} \sqrt{\frac{C_{\mathrm{v}}}{C_{\mathrm{lf}}}} \tag{9.13}$$

Now, the right hand side is entirely composed of parameters which are design constants selected during the circuit design, meaning that the ω_n/ω_{ref} ratio will remain a fixed value across a wide range of input reference and output frequencies. Designing for constant ω_n/ω_{ref} is just a matter of choosing a few device parameter ratio values, and designing the charge pump current to be linearly proportional to the VCO current, and inversely proportional to the PLL divider ratio.

9.1.2 The Self Biased ζ

The damping factor ζ also needs to be made proportional to the reference frequency. The PLL design upon which this PLL is based used for its loop filter a dual charge pump,

switched capacitor, feed forward network into an actively biased replica feedback VCO control voltage generator. This PLL design uses a much simpler RC loop filter design which benefits from lower power consumption and simpler circuit design. Instead of using a dual charge pump, switched capacitor, feed forward network as its loop filter, this PLL uses a simple series RC loop filter as is shown in Fig. 9.1, and it has been designed to ensure that its time constant $\tau = RC$ remains a fixed ratio of the loop bandwidth ω_n.

Equating the loop transfer function (9.2) to the standard 2^{nd} order transfer function, the system zero time constant occurs at

$$R_{\text{lf}}C_{\text{lf}} = \frac{2\zeta}{\omega_n},$$

and solving for the ζ damping factor results in (9.14).

$$\zeta = \frac{1}{2}\omega_n R_{\text{lf}}C_{\text{lf}} \tag{9.14}$$

Substituting in the previously derived values for ω_n, (9.10), N_{cp}, (9.12), and f_{v}, (9.7) into (9.14) results in (9.15).

$$\zeta = \frac{1}{2}\left(\sqrt{\frac{N_{\text{cp}}}{N_{\text{div}}C_{\text{lf}}}}\, f_{\text{v}}\sqrt{C_{\text{v}}}\right) R_{\text{lf}}C_{\text{lf}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\frac{\alpha}{N_{\text{div}}}}{N_{\text{div}}C_{\text{lf}}}}\left(\frac{k'V_{ov}}{C_{\text{v}}}\right)\sqrt{C_{\text{v}}}\, R_{\text{lf}}C_{\text{lf}}$$

$$\zeta = \left(\frac{\sqrt{\alpha}}{2}\sqrt{\frac{C_{\text{lf}}}{C_{\text{v}}}}\right)\left(\frac{k'V_{ov}R_{\text{lf}}}{N_{\text{div}}}\right) \tag{9.15}$$

(9.15) is a function of a few design constants and the variables, V_{ov}, N_{div}, and R_{lf}. ζ will be self biasing if R_{lf} can be made inversely proportional to $k'V_{ov}$, and linearly proportional to N_{div}.

To get R_{lf} to be inversely proportional to $k'V_{ov}$, a MOSFET device biased in the deep triode linear region, where $V_{ov} \gg V_{ds}$, will be used as the loop filter resistor. The following drain current and drain conductance, g_d, conventions will be used when

deriving the ω_n and ζ self biasing formulas.

$$I_d = k'(V_{ov}V_{ds} - \frac{V_{ds}^2}{2}) \qquad gd = \frac{dI_d}{dV_{ds}}$$

$$V_{ds} \approx 0 \qquad gd = k'(V_{ov} - V_{ds})$$

$$V_{ov} \gg V_{ds} \qquad gd|_{\mathrm{V}_{ds} \approx 0} = k'(V_{ov})$$

Assuming that, at least in steady state, the voltage across the MOSFET is almost zero, then $gd_0 = k'V_{ov}$ and the resistance of the triode MOSFET is (9.16), which fulfills the condition that R_{lf} be inversely proportional to $k'V_{ov}$.

$$R_{\mathrm{lf}} = \frac{1}{k'V_{ov}} \tag{9.16}$$

Expanding k' into $k' = k(W/L)$ gives a triode resistance of

$$R_{\mathrm{lf}} = \frac{1}{k\frac{W_{\mathrm{lf}}}{L_{\mathrm{lf}}}V_{ov}} \tag{9.17}$$

Combining (9.15) and (9.17), and splitting the VCO's k' into $k' = kW_{\mathrm{v}}/L_{\mathrm{v}}$ results in (9.18)

$$\zeta = \frac{\sqrt{\alpha}}{2}\sqrt{\frac{C_{\mathrm{lf}}}{C_{\mathrm{v}}}}\left(\frac{\frac{W_{\mathrm{v}}}{L_{\mathrm{v}}}}{N_{\mathrm{div}}\frac{W_{\mathrm{lf}}}{L_{\mathrm{lf}}}}\right)\left(\frac{kV_{ov}}{kV_{ov}}\right). \tag{9.18}$$

Self biasing is achieved by making the loop filter's W/L aspect ratio proportional to the VCO device W/L aspect ratio. If the loop filter W/L ratio is set equal to the VCO's W/L ratio multiplied by the constant β and divided by N_{div}

$$\frac{W_{\mathrm{lf}}}{L_{\mathrm{lf}}} = \frac{W_{\mathrm{v}}}{L_{\mathrm{v}}}\frac{\beta}{N_{\mathrm{div}}}, \tag{9.19}$$

then substituting (9.19) into (9.18) results in a damping factor ζ function which is set entirely by the system design constants, (9.20).

$$\zeta = \frac{\sqrt{\alpha}}{2}\sqrt{\frac{C_{\mathrm{lf}}}{C_{\mathrm{v}}}}\left(\frac{\frac{W_{\mathrm{v}}}{L_{\mathrm{v}}}}{N_{\mathrm{div}}\frac{W_{\mathrm{v}}}{L_{\mathrm{v}}}\frac{\beta}{N_{\mathrm{div}}}}\right)$$

$$\zeta = \frac{\sqrt{\alpha}}{2\beta}\sqrt{\frac{C_{\mathrm{lf}}}{C_{\mathrm{v}}}} \tag{9.20}$$

From the PLL loop transfer function

$$H(s) = N_{\mathrm{div}}\left(\frac{1 + sR_{\mathrm{lf}}C_{\mathrm{lf}}}{s^2\left(\frac{C_{\mathrm{lf}}N_{\mathrm{div}}}{I_{\mathrm{cp}}K_{\mathrm{v}}}\right) + sR_{\mathrm{lf}}C_{\mathrm{lf}} + 1}\right),$$

the loop bandwidth and damping factor

$$\omega_n = \sqrt{\frac{I_{\text{cp}} K_{\text{v}}}{N_{\text{div}} C_{\text{lf}}}} \qquad \zeta = \frac{1}{2}\sqrt{\frac{I_{\text{cp}} K_{\text{v}} R_{\text{lf}}^2 C_{\text{lf}}}{N_{\text{div}}}}$$

have been derived in a way that makes the loop bandwidth a fixed multiple of the reference frequency, and the damping factor a constant value regardless of ω_{ref} or N_{div} (9.21) and (9.22).

$$\frac{\omega_n}{\omega_{ref}} = \frac{\sqrt{\alpha}}{2\pi}\sqrt{\frac{C_{\text{v}}}{C_{\text{lf}}}} \tag{9.21}$$

$$\zeta = \frac{\sqrt{\alpha}}{2\beta}\sqrt{\frac{C_{\text{lf}}}{C_{\text{v}}}} \tag{9.22}$$

It will be shown later in this chapter that the two major PLL output phase noise contributions are from the charge pump and the VCO, and that the amount of noise from both of these sources depends on their power consumption. The α factor lets the designer scale the charge pump current with the ω_n/ω_{ref} ratio and the loop filter capacitance will be determined by α and the VCO capacitance, C_{v}, (9.23). The β factor is given by the α factor and the relative loop bandwidth (9.24), and β is used to scale the loop filter resistance (9.26).

Prior to doing the PLL schematic and layout work, the PLL noise analysis described in Section 9.5 will allow the designer to pre-determine the approximate values for C_{v}, α, and ω_n/ω_{ref}. After choosing values for C_{v}, α, ω_n/ω_{ref}, and ζ, the rest of the loop

control variables can be derived as follows.

$$\sqrt{C_{\text{lf}}} = \left(\frac{\frac{\omega_n}{\omega_{ref}}}{2\pi}\right)\sqrt{\alpha\, C_{\text{v}}}$$

$$C_{\text{lf}} = \alpha\, C_{\text{v}} \left(\frac{\frac{\omega_n}{\omega_{ref}}}{2\pi}\right)^2 \tag{9.23}$$

$$\beta = \frac{\sqrt{\alpha}}{2\zeta}\frac{\sqrt{C_{\text{lf}}}}{\sqrt{C_{\text{v}}}}$$

$$\beta = \frac{\sqrt{\alpha}}{2\zeta\sqrt{C_{\text{v}}}}\left(\frac{\frac{\omega_n}{\omega_{ref}}}{2\pi}\right)\sqrt{\alpha\, C_{\text{v}}}$$

$$\beta = \frac{\alpha}{2\zeta}\left(\frac{\frac{\omega_n}{\omega_{ref}}}{2\pi}\right) \tag{9.24}$$

$$N_{\text{cp}} = \frac{\alpha}{N_{\text{div}}} \tag{9.25}$$

$$\frac{W_{\text{lf}}}{L_{\text{lf}}} = \frac{W_{\text{v}}}{L_{\text{v}}}\frac{\beta}{N_{\text{div}}} \tag{9.26}$$

It is important here to comment that the values given in (9.23) through (9.26) are not the exact ratios which were used in the final design. To arrive at the self-biasing equations, (9.21) and (9.22), several approximations were made concerning the I_d, gm, and f_{v}, and on top of those approximations, the device short channel effects have been totally ignored.

The self-biasing equations indicate that the general behavior of the PLL will be determined by the ratios of the design capacitances and the value chosen for α, and that the loop will remain stable if these design ratios are adhered to. The component values returned by the self-biasing formulas serve as an excellent starting point, but, as the designer, it is important to realize that these formulas might require some fine tuning to create a working system. Upon VCO design completion, the design ratios will need to be adjusted to account for the various non-idealities, and the PLL loop behavior of (9.2) at different output frequencies and divide ratios will need to be verified.

9.2 The PLL Control Blocks

The PLL loop incorporates 5 major design blocks, the phase frequency detector, the charge pump, the loop filter, the voltage controlled oscillator, and the divide by N

divider. Each of these blocks work together to form the PLL control loop which locks the PLL's output phase to the reference phase.

9.2.1 The Phase Frequency Detector

The error amplifier of the PLL loop is the PFD, shown in Fig. 9.3 with the charge pump and loop filter. The PFD uses two flip flops which drive the charge pump to either source current into the loop filter, which would pull the control voltage up, or to sink current from the loop filter which will pull the control voltage down.

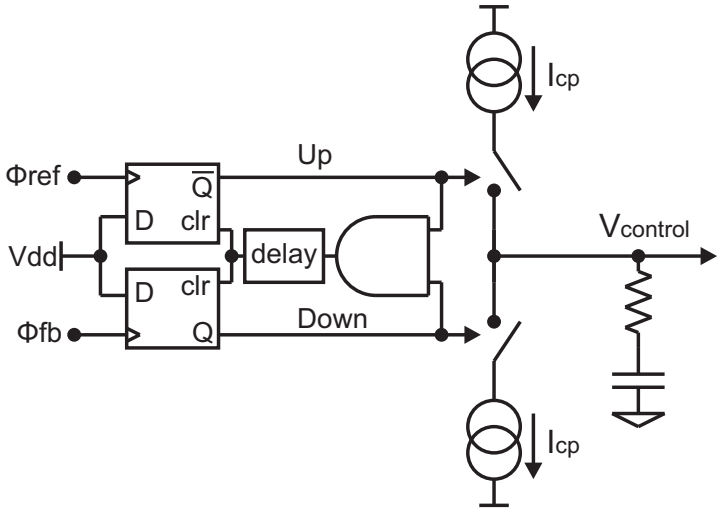


Figure 9.3: The Phase Frequency Detector and Charge Pump Circuit.

The timing diagram in Fig. 9.4 will be used to explain the PFD and charge pump operation. At the beginning, the two phase edges, reference and feedback, are arriving with two different frequencies where the reference has a faster rate than the feedback. At the first rising edge after a reset, the "up" D-Flip-Flop (DFF) output goes high, and the up switch of the charge pump is closed and current is sourced onto the loop filter which drives the VCO control voltage higher. As soon as the other DFF receives a rising edge, its output also goes high, which causes the AND gate to apply the DFF reset pulse which clears both DFF outputs to zero. The sourcing of current onto the loop filter causes VCO control voltage to ramp up which causes the output frequency to increase until the reference and output frequencies are equal. Depending on the loop transfer function damping factor, ζ, there might be a small amount of phase overshoot at which point the charge pump will start removing charge from the loop filter causing

the VCO control voltage to decrease which slows down the output frequency. If the loop is stable, then the reference and feedback signals will lock onto each other, and the output frequency will be N times the input frequency.

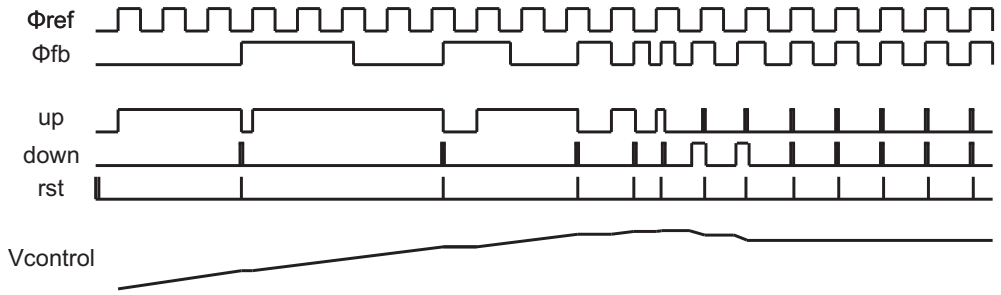


Figure 9.4: The Phase Frequency Detector and Charge Pump Circuit frequency locking timing diagram.

The design of the PFD is a fairly straight forward implementation of a couple of logic blocks taken from the foundry's process design kit (PDK). The actual implementation of the D Flip-Flops and the AND gate and delay are taken almost directly from the PFD design from [47]. The only modification from the reference design has to do with the added delay cell and inverter gate to get the proper polarity for driving the charge pump inputs, Fig. 9.5.

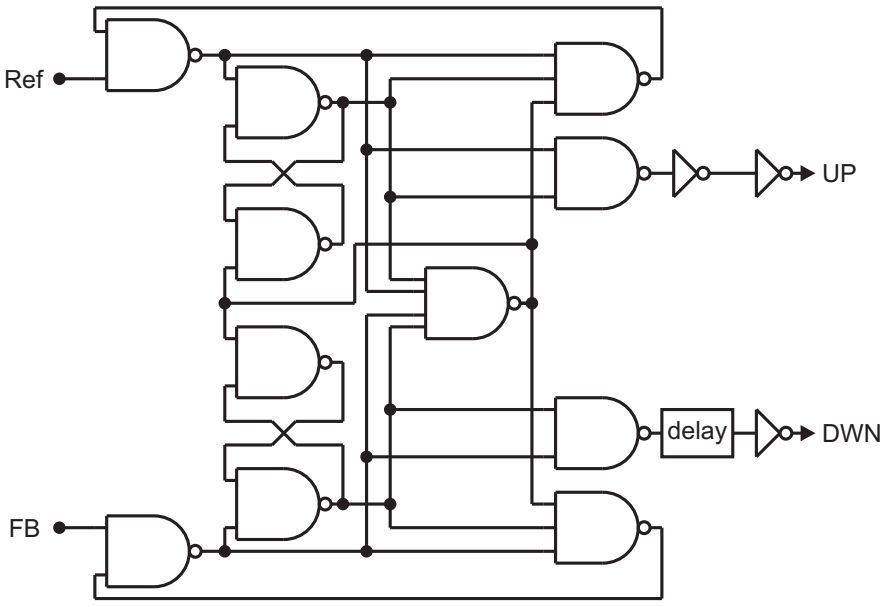


Figure 9.5: The gate level PFD circuit.

The considerations which need to be taken into account when designing the PFD is to realize that, much like an analog error amplifier, the gates inside the PFD will generate some output phase noise. This phase noise is the result of the random variance of the PFD output edge transitions with respect to time. If this timing jitter is not accounted for during the design process, it can be a sizable contributor to the VCO output jitter.

A more in depth noise analysis explaining the noise sources for the digital gates is given later in this chapter, but the end result of the noise analysis is that the digital gates in the PFD need to be big enough and powerful enough to drive the output transition with minimal gate delay. Choosing minimum size gates gates will increase the noise by having smaller gate capacitances which leads to greater kT/C noise. Also, if the gates are undersized for driving the intended load, then the gates will have slower edge transition rates, which adds even more timing variation.

9.2.2 The Charge Pump

The outputs from the PFD are used to tell the charge pump (CP) to either source or sink current into the loop filter. Fig. 9.6 is the circuit schematic of a common charge pump. The reference bias current is mirrored from the VCO drive current, and it is scaled according to the self biasing technique. Reference current from the VCO current supply is mirrored across both branches of the charge pump, and it is sourced or sank from the loop filter by switching the M1B and M4B switches on and off. To promote symmetry between the two current branches, transistors M1A and M4A have been added to the other CP current branch.

The CP operates as follows, when the M4B switch is open and the M1B switch is closed, then M2B is the current source which sinks current from the loop filter. On the other hand, when the M4B switch in closed and the M1B switch is open, then M2A is the current source, and its current is mirrored from M3A to M3B and out to the loop filter.

Looking at Fig. 9.3, after the PLL is locked, and "up" and "down" are being clocked at the same time by the reference and feedback phases, the up and down signals will both stay high for a short period of time caused by the gate propagation delay of the DFF output clear pulse. When the PLL is phase locked in its steady state, it is important that the net charge delivered to the loop filter is zero when both the up and down signal are active. Because the up and down signals will trigger with every reference cycle, then,

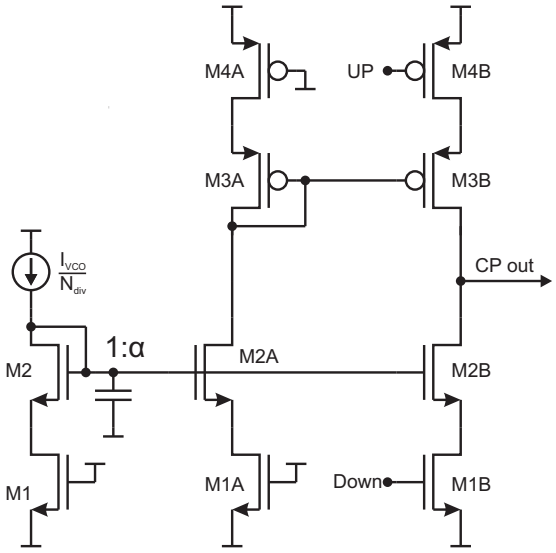


Figure 9.6: The charge pump circuit.

for the control voltage across the integrating loop filter to remain at its average locked value, then the total net charges sourced and sank from the charge pump need to be exactly equal to each other.

With the circuit in Fig. 9.6, M3A is diode connected, so its V_{ds} will always be equal to about the device V_{th}, whereas the M3B drain voltage is the output control voltage. Because of channel length modulation, if the V_{ds} voltages of the M2A:M2B mirror and the M3A:M3B mirror are not equal, this will cause a mismatch of current flow through the two branches. A problem arises if the unequal V_{ds} drain voltages cause the current mirrors M2A:M2B and M3A:M3B to sink and source unequal amounts of current to the charge pump output node.

If the current from the current references are not equal, then the up and down pulses will require two unequal on time durations so that equal amounts of charge will be sourced and sank from the loop filter. Fig. 9.7 shows how maintaining an average VCO control voltage, which will maintain an average input to output frequency ratio, will require a static phase offset $\Delta\phi$, and that at every reference period update, the unequal spike of current sourced and sank from the loop filter will cause a spike in the VCO control voltage V_{control} which gets modulated onto the output every reference period cycle.

To correct this mismatch in drain current, the charge pump in Fig. 9.8 uses a

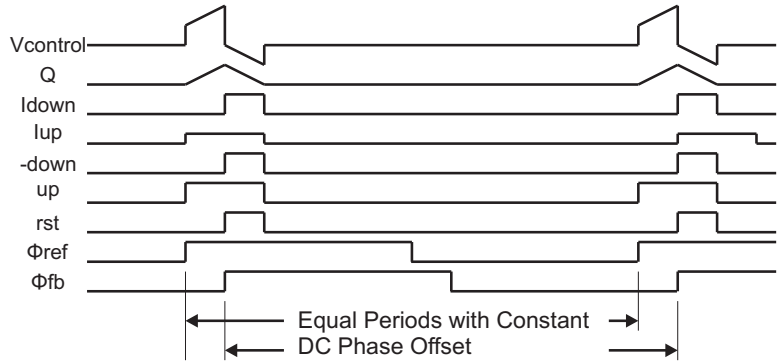


Figure 9.7: The VCO control voltage effects from unequal charge pump current biasing.

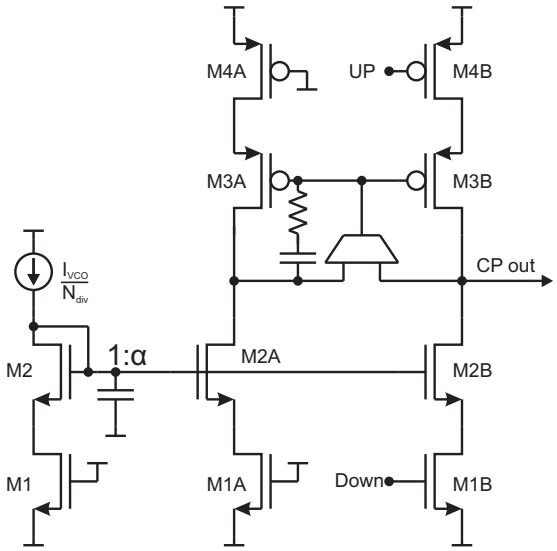


Figure 9.8: The improved charge pump circuit with active branch current matching.

feedback amplifier to drive the M3 gates to keep the M2A and M2B (and $M3_{AB}$) drain voltages at equal potential. By keeping the drain voltages equal, even with the effects of channel length modulation, because the M2 and M3 mirror devices have the same V_{ds}, V_{gs}, and V_{bs}, they should also have equal values for I_{ds}. In Fig. 9.8, as the CP output node potential goes up or down, a differential voltage will be generated across the OTA's input ports. This differential input voltage will cause the OTA to drive the gates of M3 up or down until the A and B side branch potentials are equal. The OTA is a single stage, single pole amplifier, and the feedback path has a second pole from the M3 output device. To ensure stability, a feedback capacitor and zero nulling resistor are used to split the OTA's output pole from the M3 device's pole.

9.2.3 The Divide by N Current Mirror

In Fig. 9.8, the M2 current mirrors are biased by a divide by N current mirror which uses the VCO drive current as the source reference. The divide by N current mirror reference used for this design is based on the circuit from [48], but several changes have been made to improve matching and reduce the power consumption.

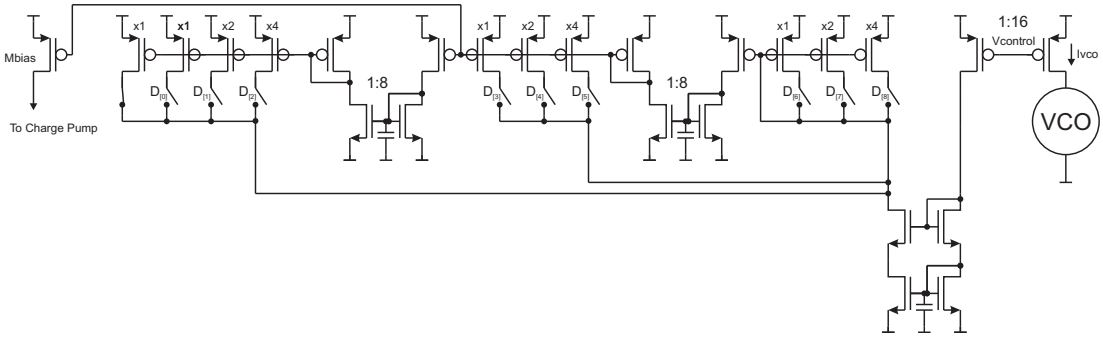


Figure 9.9: The charge pump's inversely linear current reference mirror.

To help improve matching between the current reference and the charge pump, the divide by N current mirror, Fig. 9.9, uses P devices as the current mirrors. This is done because of the M1 switch matching transistors of the charge pump (Fig. 9.8), which act like source degeneration resistors. For good current matching, the M2A and M2B device V_{gs} voltages need to be equal to each other, and this can only happen if the M1A and M1B devices have the same V_{ds}. If the inverse-linear bias generator were to use N-devices as the ratioed current mirrors to generate a bias voltage for the charge pump M2 devices, then each transistor of the inverse current mirror would need a source degeneration transistor to match the effect of the M1 device of the charge pump. On top of this, each of these source degeneration transistors would need to be proportional to N to get the appropriate voltage drop as different values of bias current flow through the charge pump.

The circuit from Fig. 9.9 ensures that the inverse linear switched current mirror is properly scaled to the VCO drive current reference source, and the output current is fed to the charge pump which has its own symmetrically matched current mirror. To reduce the power consumption, a current divider prescaler is used to divide down the VCO current by 16:1. This prescaled reference current of $I_{\mathrm{v}}/16$ is then mirrored over

to Mbias with a scale factor of 16/N (N=1 for D[8:0]=9'b000000000, and 16/512 for D[8:0]=9'b111111111)

The inverse linear current mirror works by sourcing the reference current through a variable width, diode connected, MOSFET. When the N-divider ratio is N=1, then only the always on transistor is flowing current which generates the greatest Mbias gate overdrive voltage which sources the greatest amount of current to the charge pump. When the divide ratio is N=512, then the effective channel W/L is the sum of all of the transistor widths. This wide transistor flowing the VCO reference current generates a smaller gate overdrive voltage which sources a smaller amount of current to the charge pump. In this fashion, the charge pump current, I_{cp}, is inversely related to the VCO current reference by the PLL divider ratio.

Using the previously derived current scaling factor, N_{cp} (9.25), the self biased PLL design requires the charge pump current to VCO drive current ratio to be

$$I_{\text{cp}} = \frac{I_{\text{v}}}{N_{\text{div}}}\alpha.$$

To verify the ratios of the divide by N current mirror, the transfer function from the VCO drive current to charge pump current I_{cp} for N=180 (D[8:0]=9'b010110011) is

$$I_{\text{cp}}\big|_{\text{D[8:0]=9'b010110011}} = \frac{I_{\text{v}}}{16}\left(\frac{1}{64(2)+8(4+2)+2+1+1}\right)16 = \frac{I_{\text{v}}}{180}.$$

9.2.4 The Loop Filter

The loop filter is a series RC network with a capacitance C_{lf}, and the resistor, R_{lf}, is a triode MOSFET device.

Starting with determining the value for C_{lf}, the dynamic power consumption of a ring oscillator VCO is

$$P = IV = fC_{\text{v}}V_{\text{v}}^2, \tag{9.27}$$

and this can be used to find the value for C_{v}. C_{v} is determined by designing the VCO to meet the system noise requirements, and then verified by post layout simulation results. After the VCO has been designed and layed out, a few quick post layout simulations which include the layout parasitics will supply the designer with the f, I, and V, which makes verifying the value for C_{v}, and therefore also C_{lf} quite trivial.

$$C_{\text{lf}} = \alpha C_{\text{v}}\left(\frac{\frac{\omega_n}{\omega_{ref}}}{2\pi}\right)^2$$

For finding the loop filter resistor W/L ratio, unlike the charge pump current which is supposed to be inverse-linear scaled with the divide ratio, the loop filter resistor is supposed to be scaled linearly with the divide by N ratio. The derivation of the self biased PLL calls for a triode MOSFET resistor with a W/L ratio which scales linearly with the divide by N ratio.

$$\frac{W_{\text{lf}}}{L_{\text{lf}}} = \frac{W_{\text{v}}}{L_{\text{v}}} \frac{\beta}{N_{\text{div}}}.$$

The strength of this loop filter resistor formula is that it shows that, once a suitable sized triode MOSFET is found for a particular V_{ov} and N_{div}, then to maintain self biased operation, the resistor only needs to be scaled by N to maintain self biased operation.

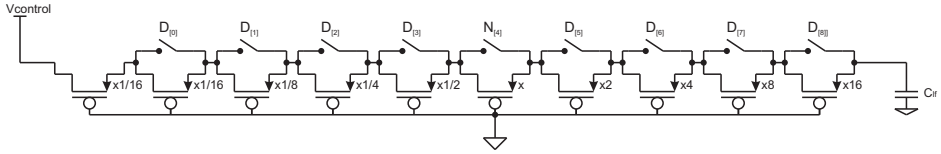


Figure 9.10: The loop filter resistor.

Because the VCO uses standard threshold voltage devices, and R_{lf} uses a low threshold voltage device, the R_{lf} W and L will not be scaled directly from the VCO devices. Instead, setting $\zeta = 1$ and combining (9.10), (9.14), and (9.27), the value for R_{lf} as a function of the VCO's I_{v}, V_{v}, and C_{v}, and the C_{lf} and N_{div} is derived (9.28).

$$\begin{aligned}
\omega_n &= \sqrt{\frac{N_{\text{cp}}}{N_{\text{div}} C_{\text{lf}}}} f_{\text{v}} \sqrt{C_{\text{v}}} \\
R_{\text{lf}} &= \frac{2}{\omega_n C_{\text{lf}}} \\
R_{\text{lf}} &= \frac{2}{C_{\text{lf}}} \frac{1}{f_{\text{v}}} \frac{\sqrt{N_{\text{div}} C_{\text{lf}}}}{\sqrt{N_{\text{cp}} C_{\text{v}}}} \\
R_{\text{lf}} &= \frac{2 N_{\text{div}}}{f_{\text{v}}} \sqrt{\frac{1}{\alpha C_{\text{v}} C_{\text{lf}}}}
\end{aligned} \tag{9.28}$$

Whichever value is used for N_{div}, the resistance of the ladder in Fig. 9.10 must equal the calculated R_{lf} when programmed with the same N_{div}.

9.2.5 Replica Bias Feedback Regulator

TODO: describe the replica bias and the PSRR benefits

9.2.6 The Phase Forwarding Ring Oscillator

The ring oscillator used for this design is an 8 stage ring oscillator which uses phase forwarding to achieve high speed oscillation with low power supply requirements. This method of generating precise delays, in this case 8 discrete phase values for 8-PSK data modulation, comes from [50]. This VCO is based on [50], but the individual delay cells have been made from simple supply regulated CMOS inverters instead of delay cells which require a supply voltage plus two bias control voltage potentials.

Most times, a ring oscillator is constructed using an odd number of stages so that the ring will start oscillating. This is because an inverter ring with an even number of stages will usually latch to its stable state of alternating 1's and 0's. Unfortunately, using an odd number of stages does not lend itself very well to creating an even number of phase steps. So, the design goal was to get an inverter ring oscillator with an even number of stages to oscillate by effectively turning it into a bunch of interleaved 3 stage ring oscillators like in Fig. 9.11. The inverter in Fig. 9.11 is an 8 stage oscillator, but the architecture can be applied to any ring oscillator with an even number of stages.

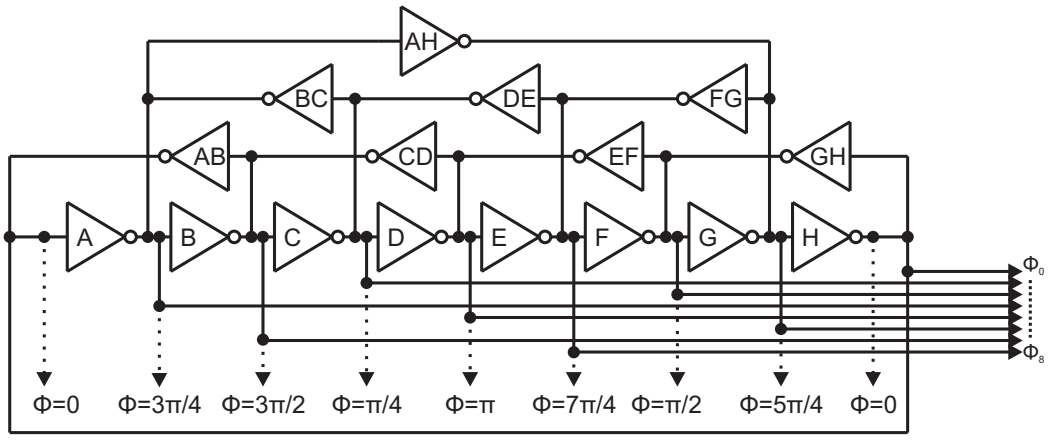


Figure 9.11: The phase forwarding 8-stage ring oscillator will generated 8 accurately spaced phase steps.

The phase delay at each stage of an N count inverter ring oscillator is $2\pi/N$, which means that there is a rising edge and a falling edge circling around the the ring oscillator evenly spaced N/2 stages apart. This makes the ring oscillator an N stage differential ring oscillator. For symmetric load matching around the ring oscillator, each oscillator stage has an output buffer for driving the clock fanout. The 8 differential stage outputs

are applied to a multiplexer for digital data symbol to 8-PSK phase modulation of the RF transmit LC oscillator, and one stage output is fed back to the PFD for phase error correction.

9.2.7 The Extended Modulus Divider

The circuit used for the PLL's divide by N block is a modulus ÷2/3 divider [51], which is made up of 8 divider blocks which can each be programmed to divide its input clock by either 2 or 3 counts. The first two divider cells do not have the added loop shortening control logic which the last 6 stages have, and these cells determine the lowest divide ratio of 2^2, and the maximum divide ratio of the 8-cell divider is $2^{8+1} - 1 = 511$. The implant's sampling electronics have been designed to work with reference frequencies of 2, 4, 8, and 16 MHz, so using divide ratios from 4 to 511 gives a possible PLL output frequency range of 8 to 8176 MHz, but there is no intention of having the chip operate at frequencies much less than 100 MHz of much greater than 1 GHz.

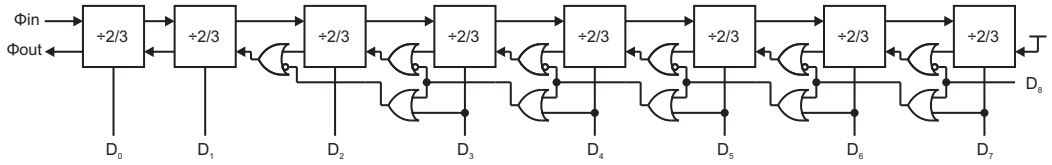


Figure 9.12: The 6 stage, extended modulus 2/3 divider block. The divide range is from $2^2 = 4$ to $2^{8+1} - 1 = 511$.

The ÷2/3 cell structure and schematic are given in Fig. 9.13. The block diagram of the ÷2/3 cell is given in Fig. 9.13a. DFF1 from the ÷2/3 cell divides the input clock by 2. If the MOD_IN signal is high, then DFF2 will clock the result of the DFF1 divide by 2 operation out onto MOD_OUT. As long as the ÷2/3 cell's D_n input is low, then DFF1 will toggle every input clock cycle. However, when the D_n input is high, then, when MOD_OUT goes high, DFF1's AND gate logic will disable the toggle operation for one clock cycle, which results in the ÷2/3 cell having a divide by 3 ratio.

The schematic of the ÷2/3 cell is given in Fig. 9.13b. Fast divider circuits are often constructed using common mode logic (CML) latches because of their higher speed and lower power consumption at very high frequencies when compared to latches implemented with digital logic [51]. However, this PLL is expected to operate at frequencies up to only about 1 GHz, and, for this reason, the StrongARM latch [27] has been

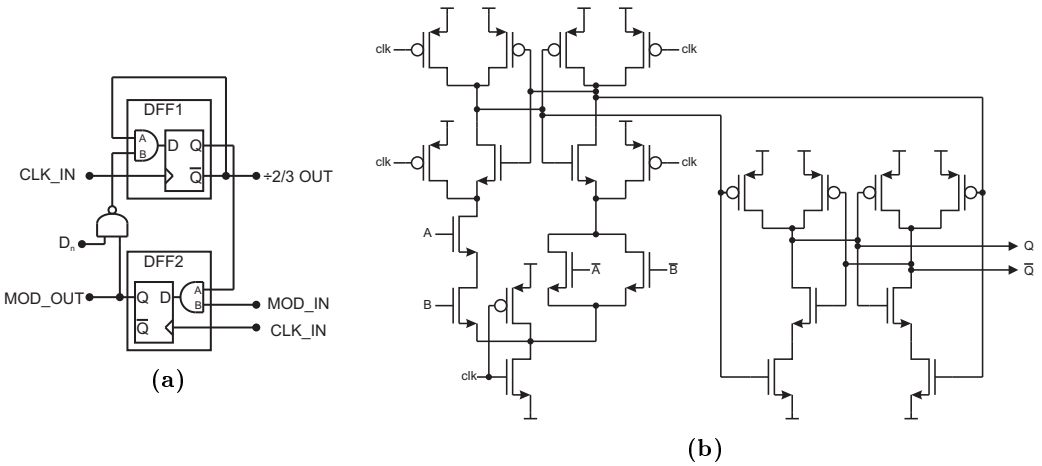


Figure 9.13: The PLL divider divide by 2 or 3 cell.
a) The block diagram of the $\div 2/3$ cell.
b) The schematic of the AND gate input StrongARM latch.

chosen instead of the CML latch. A CML latch would have a constant static power consumption regardless of its operating frequency, but the StrongARM latch's power consumption is linearly proportional to the switching frequency and can be quite low at low frequencies. The AND gate and the latch logic are integrated together into a single combined device by integrating an NMOS logic AND gate into the StrongARM latch's differential pair input decision circuitry.

9.3 The PLL Phase Noise Analysis

The PLL block diagram with the various noise sources is given in Fig. 9.14.

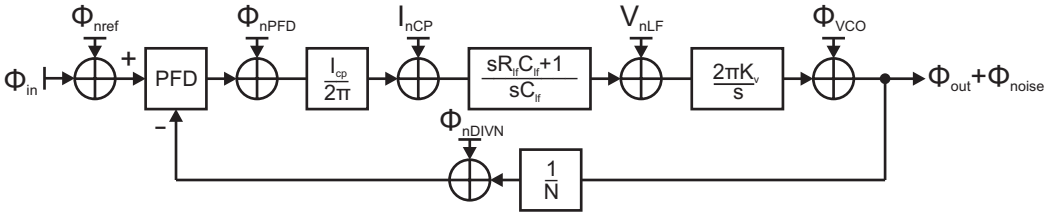


Figure 9.14: The PLL block diagram

Starting with the PLL's transfer function,

$$H(s) = \frac{\Phi_{\text{out}}}{\Phi_{\text{in}}} = \frac{G(s)}{1 + \frac{G(s)}{N}},$$

where

$$G(s) = \frac{I_{\text{CP}}}{2\pi}\left(\frac{sR_{\text{lf}}C_{\text{lf}} + 1}{sC_{\text{lf}}}\right)\left(\frac{2\pi K_{\text{v}}}{s}\right)$$

is the forward gain and N is the divide ratio, the various noise transfer functions are:

$$\frac{\Phi^2_{\text{out}_{\text{nref}}}}{\Phi^2_{\text{nref}}} = H^2(s) \tag{9.29}$$

$$\frac{\Phi^2_{\text{out}_{\text{nPFD}}}}{\Phi^2_{\text{nPFD}}} = H^2(s) \tag{9.30}$$

$$\frac{\Phi^2_{\text{out}_{\text{nDIVN}}}}{\Phi^2_{\text{nDIVN}}} = -H^2(s) \tag{9.31}$$

$$\frac{\Phi^2_{\text{out}_{\text{nCP}}}}{I^2_{\text{nCP}}} = H^2(s)\left(\frac{2\pi}{I_{\text{CP}}}\right)^2 \tag{9.32}$$

$$\frac{\Phi^2_{\text{out}_{\text{nLF}}}}{V^2_{\text{nLF}}} = H^2(s)\left(\frac{2\pi}{I_{\text{CP}}}\right)^2\left(\frac{sC_{\text{lf}}}{sR_{\text{lf}}C_{\text{lf}} + 1}\right)^2 \tag{9.33}$$

$$\frac{\Phi^2_{\text{out}_{\text{nVCO}}}}{\Phi^2_{\text{nVCO}}} = H^2(s)\left(\frac{2\pi}{I_{\text{CP}}}\right)^2\left(\frac{sC_{\text{lf}}}{sR_{\text{lf}}C_{\text{lf}} + 1}\right)^2\left(\frac{s}{2\pi K_{\text{v}}}\right)^2 = \frac{1}{\left(1 + \frac{G(s)}{N}\right)^2} \tag{9.34}$$

The first four noise sources, (9.29) through (9.32), have the same bandwidth characteristics as the PLL loop itself, except that (9.32) is scaled by the inverse of the charge pump gain. These PLL source looking transfer functions are plotted in Fig. 9.15 for $N = 125$ and $2\pi/I_{\text{CP}} = 3.2$ (the value chosen for $2\pi/I_{\text{CP}}$ was purely arbitrary, just to create a nicely scaled plot). The transfer functions are effectively a low pass filter with bandwidth ω_n, so reducing the loop bandwidth will reduce the bandwidth integrated noise from these noise sources.

The transfer function for the loop filter noise is the charge pump transfer function multiplied by the inverse of the loop filter impedance (9.33). The loop filter's inverse impedance is of the form $s/(s+1)$ which is essentially a high pass filter. The resulting loop filter noise transfer function, (9.33), is simply a bandpass filter with center frequency around ω_n as in Fig. 9.16.

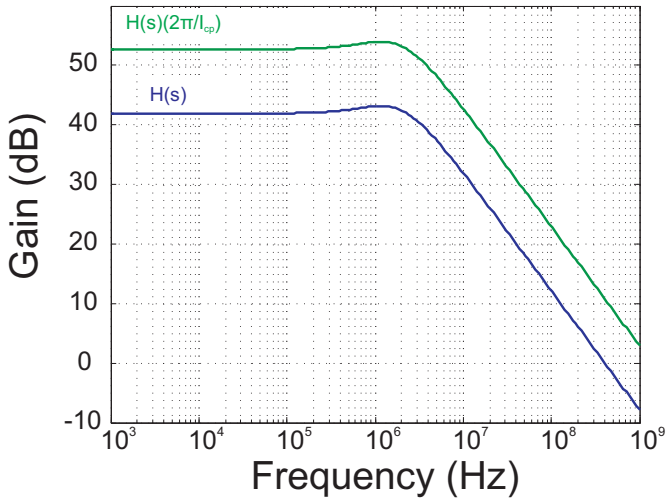


Figure 9.15: The PLL source looking noise transfer functions (9.29) through (9.32).

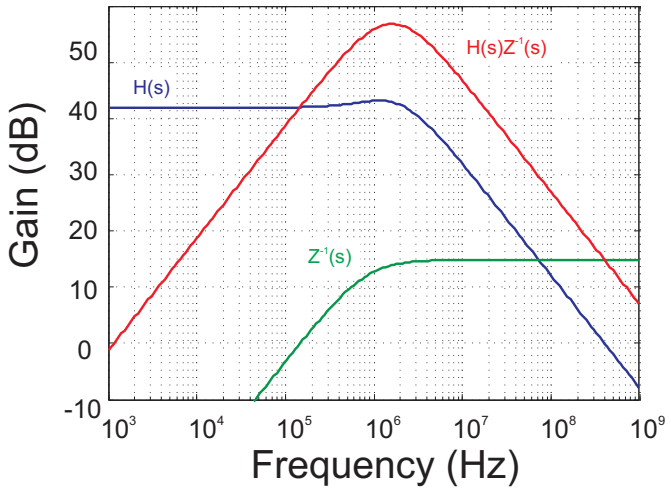


Figure 9.16: The PLL loop filter noise transfer function.

The VCO noise transfer function is the loop filter transfer function multiplied by the inverse gain of the VCO block 9.34. The VCO block's inverse gain, $s/(2\pi K_{\rm v})$, is a 20dB/decade ramp with a zero at DC indicating infinite DC feedback. When the VCO inverse gain block is multiplied with the loop filter noise transfer function, the resulting VCO noise transfer function, (9.34), is a ramp rising at 40dB/dec until about ω_n where the loop filter's bandpass transfer function gain starts to fall at 20dB/dec. After ω_n, the VCO noise transfer function flattens out, Fig. 9.17, and all phase noise from the VCO makes it to the PLL output.

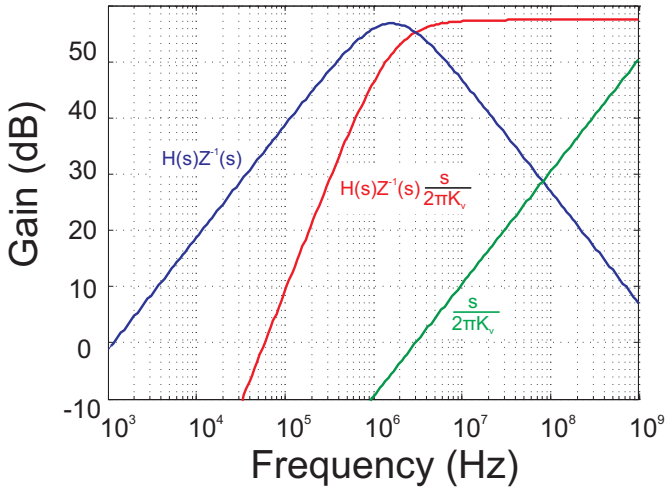


Figure 9.17: The PLL VCO noise transfer functions.

In contrast to how the reference phase noise sources' total integrated noise output can be reduced by reducing the loop bandwidth, the loop filter transfer function looks bandpass in nature with a center frequency at the PLL loop's $1/R_{\text{lf}}C_{\text{lf}} = \omega_n/2$ frequency, and its noise is not greatly effected by the overall loop bandwidth. Contrary to the reference noise sources, reducing the PLL bandwidth by making the $G(s)$ smaller, will allow more of the VCO noise to make it to the PLL output (9.34). This is the required compromise when allocating the available noise budget to the various PLL components, reducing ω_n reduces the source looking noise, but increases the VCO noise and vica versa.

The reference source is a low jitter crystal reference, and its phase noise can be pretty much ignored because it is small and consists mostly of low frequency phase noise occurring at frequencies much less than the PLL loop's ω_n. Also, because the PLL transmitter and the external base station use coherent data modulation/demodulation which are both referenced from the same crystal oscillator, the effects from the low frequency reference phase noise will be greatly suppressed by the PLL's infinite DC gain. The phase noise from the crystal reference will be approximated to zero, and the PLL active electronics will be designed to meet the phase noise requirements of the wireless link.

9.3.1 The Digital Gate Noise Sources

The phase noise generated by the PFD, divider, and VCO is a result of the variance in the edge crossings of the digital gates inside each of those blocks. The digital gate white noise comes from two different mechanisms. For the CMOS gate, one source of timing noise comes from the device when it is in its on or off state, and the other source of noise is the 4ktγgm noise when the gate is switching from high to low [52]. To be able to calculate how much phase noise each of these blocks will produce at the PLL's output node, it is first necessary to derive formulas which characterize the amount of timing jitter variance each of the respective noise sources will produce.

9.3.1.1 kT/C Gate Noise

The kT/C noise when the gate is either on or off doesn't affect the digital output while the device is on or off, but it does have an impact as to when exactly the gate output crosses the switching threshold. Fig. 9.18 shows how the kT/C noise voltage variance, σ_v^2, affects the actual point in time where the gate output crosses the switching threshold for the next gate. The main point to take away from Fig. 9.18 is that in the on or off state, the noise from the triode MOSFET is the typical kT/C noise, where C is the output load capacitance.

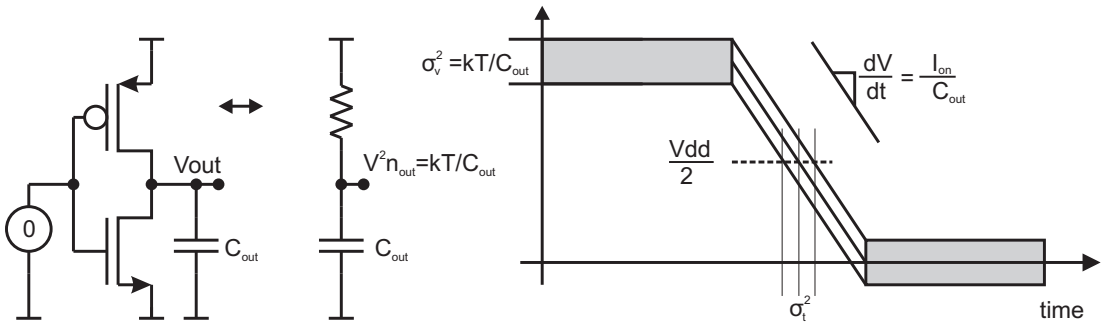


Figure 9.18: The digital gate on or off state noise contribution.

Using Fig. 9.18, a noise analysis can be performed which will help to characterize the timing jitter versus dynamic power consumption as a function of the digital gate size. Frequency jitter arises from the timing variance, σ_t^2, when the output actually crosses the switching threshold. The timing variance for one edge transition, $\sigma_{t_{edge}}^2$, is

caused by the voltage variance, σ_v^2, divided by the square of the fall time slope I_{on}/C_{out}.

$$\sigma_v^2 = \frac{kT}{C_{out}}$$
$$\sigma_{t_{edge}}^2 = \frac{\sigma_v^2}{\left(\frac{I_{on}}{C_{out}}\right)^2}$$
$$\sigma_{t_{edge}}^2 = \frac{\frac{kT}{C_{out}}}{\left(\frac{I_{on}}{C_{out}}\right)^2}$$
$$\sigma_{t_{edge}}^2 = \frac{kT}{I_{on}}\left(\frac{C_{out}}{I_{on}}\right)$$

The factor C_{out}/I_{on} is the reciprocal of the slope, dt/dV, and if dt is the total the fall time, t_{fall}, for the entire gate output voltage swing $V_{dd} \to 0$ transition, then $dV = V_{dd}$ and

$$\frac{C_{out}}{I_{on}} = \frac{t_{fall}}{V_{dd}}$$
$$\sigma_{t_{edge}}^2 = \frac{kT}{I_{on}V_{dd}}t_{fall}.$$

So far, the timing variance for one edge transition of a single gate has been has been derived, but the goal is to calculate the time variance for the frequency jitter of the CMOS inverter gate ring oscillator. Because 1 Hz requires two edge transitions per timing period, the jitter timing variance of an oscillator is 2 times the edge jitter of the single gate (9.35).

$$\sigma_t^2 = 2\frac{kT}{I_{on}V_{dd}}t_{fall} \tag{9.35}$$

(9.35) is the jitter noise which is caused by the thermal noise which is sampled onto the output capacitance at the time when the gate is told to switch states. What the formula shows is, the timing variance is inversely proportional to the amount of power the gate consumes during switching, and it is linearly proportional to the transition fall time. This is the generally expected result, reducing the noise requires more power.

9.3.1.2 4kTγgm Gate Noise

There is also timing variance which comes from the transistors during the switching transition. Fig. 9.19 will be used for determining the amount of jitter noise caused by the MOSFET noise current as it is switching.

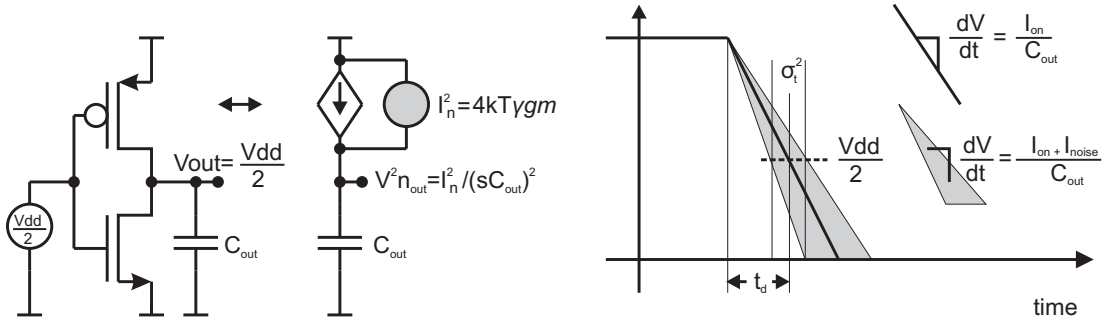


Figure 9.19: The digital gate on or off state noise contribution.

Unlike the noise from Fig. 9.18 which had all of the noise from the very beginning of the high to low transition, the slewing noise in Fig. 9.19 starts out with zero noise, and the noise current is integrated onto the output cap as the device transitions from high to low.

Starting by finding the transition slopes for both the noisy and the noiseless transitions, then finding the difference between the noise and the noiseless slope, and then normalizing that slope difference against the nominal noiseless slope gives the amount of impact the noise current has on the noise free slope (9.36). The result is that the relative amount of time variance that the noise current has on the amount of time it takes for the output voltage to cross the $V_{dd}/2$ transition threshold is just the ratio of noise current to the nominal gate current.

$$\frac{dV_{noisy}}{dt} = \frac{I_{on} + I_{noise}}{C_{out}}$$

$$\frac{dV_{noiseless}}{dt} = \frac{I_{on}}{C_{out}}$$

$$\Delta\left(\frac{dV}{dt}\right) = \frac{I_{noise}}{C_{out}}$$

$$\frac{\Delta\left(\frac{dV}{dt}\right)}{\frac{dV_{noiseless}}{dt}} = \frac{I_{noise}}{I_{on}} \tag{9.36}$$

Multiplying the amount of fall time slope impact (9.36) with the ideal time delay, t_d, and moving into the variance space, gives the total amount of jitter variance (9.37).

$$\sigma^2_{t_{edge}} = \frac{I^2_{noise}}{I^2_{on}} t^2_d \tag{9.37}$$

To find the amount of timing jitter variance, σ_t^2, the saturation noise current needs to be derived. The noise current of a MOSFET in saturation is

$$I_n^2 = 4kT\gamma gm\Delta f,$$

where $gm = 2I_d/V_{ov}$, and Δf is the bandwidth of the noise.

The noise bandwidth is derived from the amount of time that the noise is being sampled onto the load capacitor. The noise sample period is from the transition start time to the $V_{dd}/2$ CMOS switching point. This transition sample period is marked t_d in Fig. 9.19, and in Nyquist terms, a sample period of t_d gives a bandwidth frequency of $1/2t_d$. Starting with the MOSFET saturation noise current, the total jitter variance is for a single edge transition is (9.38).

$$\begin{aligned} I_{noise}^2 &= 4kT\gamma gm\Delta f \\ gm &= \frac{2I_d}{V_{ov}} \\ \Delta f &= \frac{1}{2t_d} \\ \sigma_{t_{edge}}^2 &= 4kT\gamma \frac{2I_{on}}{V_{ov}} \frac{1}{2t_d} \frac{1}{I_{on}^2} t_d^2 \\ \sigma_{t_{edge}}^2 &= 4kT\gamma \frac{1}{V_{ov} I_{on}} t_d \end{aligned} \tag{9.38}$$

Just like with (9.35), the total timing noise per period is two times the edge noise, resulting in a total gm thermal timing noise per oscillation period (9.39).

$$\sigma_t^2 = 8kT\gamma \frac{1}{V_{ov} I_{on}} t_d \tag{9.39}$$

The slewing noise (9.39) is very similar to (9.35) in the sense that the noise is a function of the kT thermal energy, inversely proportional to power, and linearly proportional to the time delay.

Making the assumption that the ring oscillator gates will be sized to give equal delays from the pull-up and pull-down actions of the P and N-type transistors, and substituting $t_{fall} = 2t_d$ and $t_d = 1/(2f_{\mathrm{v}})$, where f_{v} is the oscillator center frequency, then (9.35) and (9.39) can be combined to give the total period jitter (9.40).

$$\sigma_\tau^2 = \frac{2kT}{I_{\mathrm{v}} f_{\mathrm{v}}} \left(\frac{1}{V_{\mathrm{v}}} + \frac{2\gamma}{V_{ov}} \right) \tag{9.40}$$

9.4 The PLL Control Block Phase Noise Contributions

Each control block of the PLL loop generates noise which adds to the total output phase noise of the PLL. The current noise from the charge pump, I^2_{nCP}, and the voltage noise from the loop filter, V^2_{nLF}, can be calculated using the standard $4kTR$ thermal noise energy calculations. The other three blocks of the PLL, the PFD, divider, and the VCO, each generate noise on their rising and falling edges, and their phase noise contribution will be calculated by determining how much edge jitter is generated by their gate device thermal noise.

9.4.1 The PFD Phase Noise

The PFD phase noise comes from phase propagation through the digital gates of the of the PFD (Fig. 9.20).

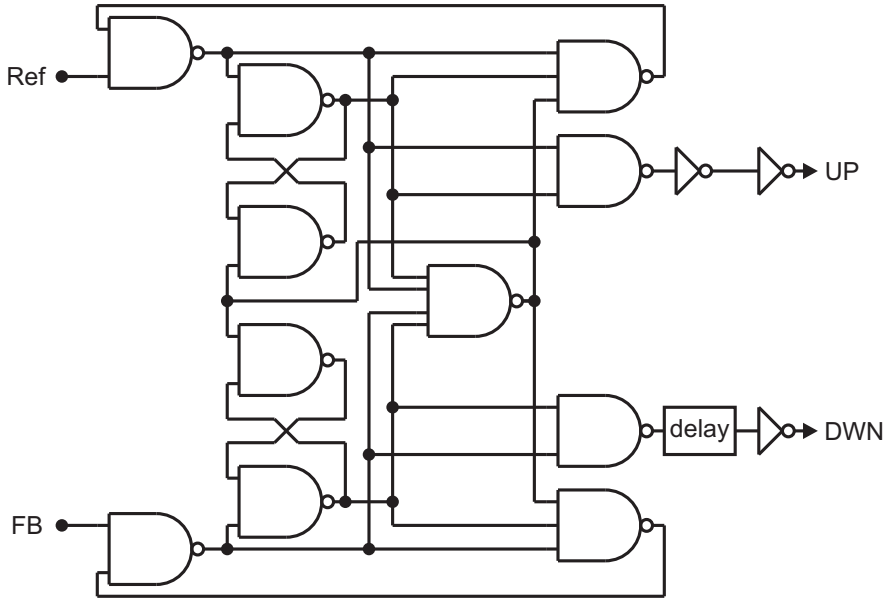


Figure 9.20: The gate level PFD circuit.

A noise analysis could be used to determine the amount noise jitter that the gates would produce based on the number of edge propagations from input to output. However, this PFD uses gates from the standard cell library, and it was deemed more time effective to construct the PFD and measure the phase noise of the constructed circuit. Using this method, the drive strength of the gates of the PFD circuit can be increased

as necessary, until the phase noise of the PFD is small enough to have only a negligible effect on the overall PLL output phase noise.

9.4.2 The Charge Pump Phase Noise

The noise from the charge pump comes mostly from the thermal noise of two current sourcing transistors, M2 and M3, when they are sourcing current to the loop filter node. The M1 and M4 devices are either full on or full off and do not source significant noise current when compared to M2 and M3. The noise from M2 and M3 is the usual MOSFET $4kT\gamma gm$ white noise plus the flicker noise current (9.52).

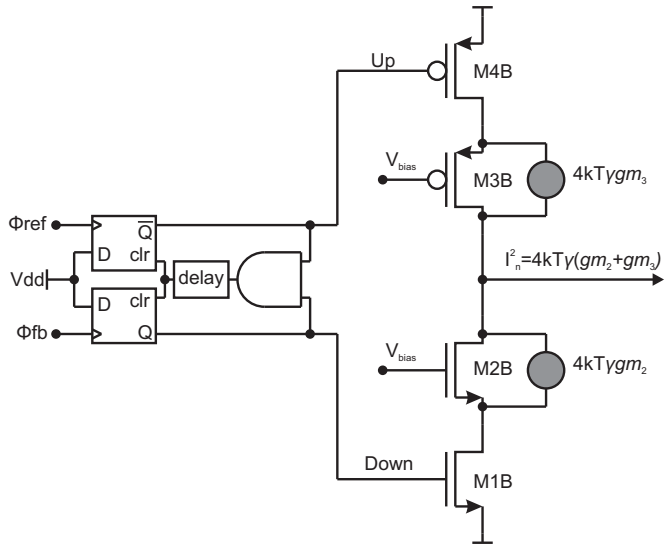


Figure 9.21: The charge pump schematic with noise sources.

As the PLL is bringing itself into lock, the current source transistors source current and noise to the CP output. But, because the PLL is not yet locked, the noise current generated during this mode of operation is not of much concern. Instead, the noise generated under the steady state PLL locked condition will be evaluated.

The charge pump is driven by a phase frequency detector which employs a reset pulse delay for reducing the dead-zone period. When the PLL is in lock and both the reference and the feedback signals are reaching the PFD at the same time, then the Up and Down signals will both be active for a short period of time (Fig. 9.4). For this short period of time, the charge pump current, I_{CP}, is sourced by M3 and sank by M2, for

a net output current of zero Amperes plus the sum of the two uncorrelated MOSFET noise currents. The value of the charge pump white noise current during the delay is

$$I^2_{\mathrm{nCP\,white}} = 4kT\gamma(gm_2 + gm_3)\Delta f. \tag{9.41}$$

The delay period is t_{on}, and if both of the source transistors are operating with equal transconductance efficiency values of $\eta_{gm_{2,3}} = gm/I_{\mathrm{cp}}$ (the MOSFET gm efficiency normally ranges between 10 and 30), then, for $\Delta f = 1/(2t_{\mathrm{on}})$, the charge pump noise current can be given as a function of I_{CP} (9.42).

$$I^2_{\mathrm{nCP\,white}} = 4kT\gamma(2\eta_{gm}I_{\mathrm{CP}})\frac{1}{2t_{\mathrm{on}}} \tag{9.42}$$

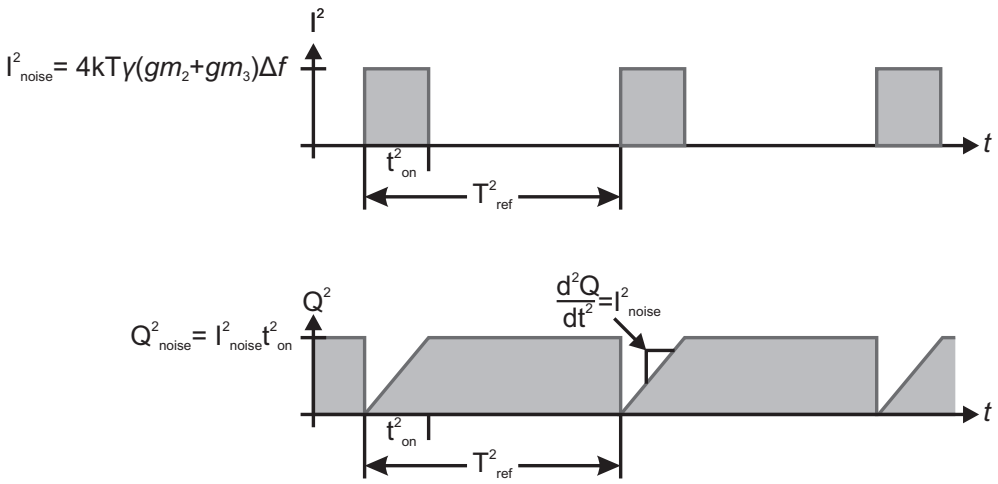


Figure 9.22: The charge pump noise generation mechanism

The term t_{on} is the length of time that the locked PLL charge pump is conducting current, and is determined through simulation (this PFD has 400ps of dead time). This creates a noise current pulse with (9.42) amount of noise current occurring once every PLL reference clock cycle. In Fig 9.22, each pulse of noise current results in the generation of a packet of noise charge every reference clock cycle. The noise charge per reference period divided by the reference period duration, T_{ref}, gives an average charge pump noise current of (9.43).

$$
\begin{aligned}
I^2_{\mathrm{nCP}_{\mathrm{pulse}}} &= 4kT\gamma(\eta_{gm}I_{\mathrm{CP}})\frac{1}{t_{\mathrm{on}}} \\
I^2_{\mathrm{nCP}_{\mathrm{white}}} &= I^2_{\mathrm{nCP}_{\mathrm{pulse}}}\left(\frac{t^2_{\mathrm{on}}}{T^2_{\mathrm{ref}}}\right) \\
I^2_{\mathrm{nCP}_{\mathrm{white}}} &= 4kT\gamma(\eta_{gm}I_{\mathrm{CP}})\left(\frac{t_{\mathrm{on}}}{T^2_{\mathrm{ref}}}\right)
\end{aligned} \tag{9.43}
$$

The charge pump flicker noise current can be modeled with the empirically derived formula (9.52) (the derivation is given in Sec. 9.4.4.2). Integrating the flicker noise current up to the the flicker noise corner, and averaging the noise current from the t_{on} pulse over the T_{ref} duration results in the total integrated flicker noise current of (9.44).

$$
I^2_{\mathrm{nCP}_{\mathrm{flicker}}} = \frac{16}{3}\frac{KF(\eta_{gm}I_{\mathrm{CP}})^2}{C_{gs_{\mathrm{NP}}}}\ln(f_{\mathrm{hi}})\left(\frac{t^2_{\mathrm{on}}}{T^2_{\mathrm{ref}}}\right) \tag{9.44}
$$

Combining (9.32), (9.43), and (9.44) results in the total integrated charge pump noise current induced PLL phase noise (9.45).

$$
\Phi^2_{\mathrm{out}_{\mathrm{nCP}}} = H^2(s)(2\pi)^2\left(\frac{4kT\gamma\eta_{gm}}{I_{\mathrm{CP}}}\left(\frac{t_{\mathrm{on}}}{T^2_{\mathrm{ref}}}\right) + \frac{16}{3}\frac{KF\eta_{gm}}{C_{gs_{\mathrm{NP}}}}\ln(f_{\mathrm{hi}})\left(\frac{t^2_{\mathrm{on}}}{T^2_{\mathrm{ref}}}\right)\right) \tag{9.45}
$$

The end result of (9.45) is that to reduce the phase noise from the charge pump, it is necessary to:

- Increase I_{CP}, which consumes more system power.
- Decrease t_{on}, which requires faster gates in the PFD, which requires more system power.
- Increase T_{ref}, which will, however, reduce the reference frequency which will in turn require greater PLL phase multiplication.
- Reduce η_{gm}, which will increase the device saturation voltage thereby reducing the effective operating range of the charge pump.

9.4.3 The Loop Filter Noise

The noise voltage from the loop filter is simply the $4kTR$ noise of the loop filter's resister. The noise equivalent circuit for the loop filter is given in Fig. 9.23.

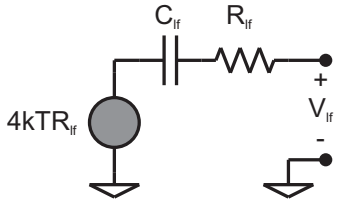


Figure 9.23: The loop filter equivalent noise circuit

When the resistor noise voltage is driving an infinite impedance, the loop filter noise voltage is either zero at DC, or $4kTR_{\text{lf}}$ (9.46).

$$V_{\text{lf}}^2 = 4kTR_{\text{lf}} \left(\frac{\infty}{\infty + \left(\frac{sR_{\text{lf}}C_{\text{lf}}+1}{sC_{\text{lf}}} \right)} \right)^2$$

$$V_{\text{lf}}^2 = 4kTR_{\text{lf}} \left(\frac{sC_{\text{lf}}\infty}{sC_{\text{lf}}\infty + sR_{\text{lf}}C_{\text{lf}} + 1} \right)^2$$

$$V_{\text{lf}}^2 = \begin{cases} 0 & \text{if } j\omega = 0 \\ 4kTR_{\text{lf}} & \text{if } j\omega \neq 0 \end{cases} \tag{9.46}$$

9.4.4 The VCO Phase Noise

The VCO phase noise is usually characterized using two different frequency zones as in Fig. 9.24. There is a white noise component which follows a $1/f^2$ slope, and it is the dominant noise at higher offset frequencies. There is also a flicker noise component which follows a $1/f^3$ slope, and it is the dominant frequency at lower values of offset frequency.

9.4.4.1 The VCO $1/f^2$ Phase Noise Content

To determine how much phase noise the oscillator will produce, it is necessary to convert the jitter timing variance, σ_τ^2, into an expression for the phase noise variance. According to [52], the single sideband (SSB) phase noise power spectral density (PSD) can be derived from the jitter variance as (9.47).

$$\mathcal{L}(f) = \sigma_\tau^2 \frac{f_{\text{v}}^3}{f^2} \tag{9.47}$$

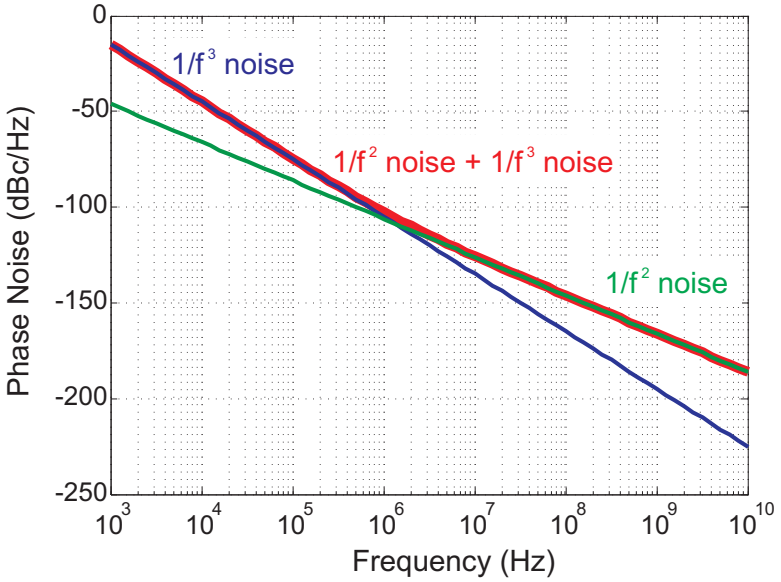


Figure 9.24: The VCO phase noise composition.

Combining (9.40) and (9.47), and setting the gate overdrive voltage equal to the VCO control voltage $V_{gs} = V_{\mathrm{v}}$, results in an inverter ring oscillator SSB phase noise of (9.48).

$$\mathcal{L}(f) = \left(\frac{f_{\mathrm{v}}}{f}\right)^2 \left[\frac{2kT}{I_{\mathrm{v}}V_{\mathrm{v}}}\left(1 + \frac{2\gamma}{1 - \frac{V_{th}}{V_{\mathrm{v}}}}\right)\right] \tag{9.48}$$

This PSD function shows that the amount of phase noise from the white noise jitter is a function of the VCO frequency, f_{v}, the amount of power consumed by the ring, $I_{\mathrm{v}}V_{\mathrm{v}}$ and the process parameters γ and V_{th}. The result of this conclusion is that increasing the number of stages while decreasing the load per stage does not affect the phase noise as long as the center frequency and power consumption remain constant.

9.4.4.2 The VCO $1/f^3$ Phase Noise Content

The flicker noise component of the gate jitter noise causes low frequency shifts in the oscillator frequency which lasts for several oscillation periods. This low frequency multiplicative phase noise is modeled using the narrow band FM expression [53, 54]

$$\mathcal{L}(f) = \frac{1}{4f^2}K_{\mathrm{v}}^2 S_c(f) \tag{9.49}$$

which gives the phase noise PSD as a function of the VCO gain, K_{v}, and the control signal variance, $S_c(f)$. To find the phase noise from the flicker noise current, the VCO

control signal variance is equated to the flicker noise current

$$S_c(f) = I^2_{flicker}.$$

To know how much phase noise comes from the flicker noise current requires first deriving the VCO's transfer function with respect changes in its supply current (9.50).

$$\begin{aligned} K_{\mathrm{v_I}} &= \frac{df_{\mathrm{v}}}{dI_{\mathrm{v}}} \\ K_{\mathrm{v_I}} &= \frac{d}{dI_{\mathrm{v}}}\left(\frac{I_{\mathrm{v}}}{C_{\mathrm{v}}V_{\mathrm{v}}}\right) \\ K_{\mathrm{v_I}} &= \frac{1}{C_{\mathrm{v}}V_{\mathrm{v}}} = \frac{f_{\mathrm{v}}}{I_{\mathrm{v}}} \end{aligned} \tag{9.50}$$

Substituting (9.50) into (9.49) results in the phase noise PSD expression as a function of the flicker noise current (9.51)

$$\mathcal{L}(f) = \frac{1}{4f^2}\left(\frac{f_{\mathrm{v}}}{I_{\mathrm{v}}}\right)^2 I^2_{flicker} \tag{9.51}$$

Empirical measurement results are used to model the MOSFET device flicker noise current with the following flicker noise model formula [53].

$$I^2_{flicker} = \frac{KF_{\mathrm{NP}}\, gm^2_{\mathrm{NP}}}{C'_{ox}WL\, f} \tag{9.52}$$

Using this flicker noise formula and Spectre AC/.Noise simulations, the values for KF_{N} and KF_{P} for this technology under the expected operating conditions were found to be about $4(10^{-24})$ and $6(10^{-24})$ respectively.

For each VCO oscillation cycle, there is flicker noise generated by both the N devices and the P devices

$$I^2_{flicker} = \frac{KF_{\mathrm{N}}\, gm^2_{\mathrm{N}}}{C_{gs_{\mathrm{N}}} f} + \frac{KF_{\mathrm{P}}\, gm^2_{\mathrm{P}}}{C_{gs_{\mathrm{P}}} f}.$$

Making the following approximations helps to simplify the noise calculations.

$$\begin{aligned} KF_{\mathrm{N}} &= KF_{\mathrm{P}} = KF \approx 6(10^{-24}) \\ gm_{\mathrm{N}} &= gm_{\mathrm{P}} = gm \\ C_{gs_{\mathrm{N,P}}} &= C'_{ox}W_{\mathrm{N,P}}L_{\mathrm{N,P}} \end{aligned}$$

Designing the VCO stages so that the pull up and pull down drive strengths are equal, the P and N-Type devices will have their gate areas scaled to a roughly 3:1 ratio.

$$C_{gs_{\mathrm{P}}} = 3C_{gs_{\mathrm{N}}}.$$

For minimum channel length devices operating in velocity saturation, the C_{gs_P} to C_{gs_N} scaling would be closer to 1:1, but, as will be shown at the end of the derivation, using longer channel length devices, even though they reduce the MOSFET f_t, help to reduce the 1/f flicker noise.

Applying these approximations to the flicker noise formula, (9.52), results in a flicker noise current of (9.53)

$$\begin{aligned} C_v &= C_{gs_P} + C_{gs_N} \\ C_{gs_N} &= \frac{C_v}{4} \\ C_{gs_P} &= \frac{3C_v}{4} \\ I^2_{flicker} &= \frac{KFgm^2}{f}\left(\frac{1}{\frac{C_v}{4}} + \frac{1}{\frac{3C_v}{4}}\right) \\ I^2_{flicker} &= \frac{16}{3}\frac{KFgm^2}{C_v f} \end{aligned} \tag{9.53}$$

Substituting (9.53) into (9.51) gives the phase noise PSD from the flicker noise jitter as (9.54).

$$\begin{aligned} \mathcal{L}(f) &= \frac{1}{4f^2}\left(\frac{f_v}{I_v}\right)^2 \frac{16}{3}\frac{KFgm^2}{C_v f} \\ \mathcal{L}(f) &= \frac{4}{3}\frac{KF}{C_v}\left(\frac{gm^2}{I_v^2}\right)\frac{f_v^2}{f^3} \end{aligned} \tag{9.54}$$

The insight gained from (9.54) is that the phase noise from the flicker jitter is reduced by either driving a larger capacitance, which costs more power, or by reducing gm/I_v transconductance efficiency (smaller W/L ratios), which will also cost more power to get the same VCO speed. Substituting $I_v = C_v V_v f_v$ and deriving (9.54) a little bit further results in a function for the flicker phase noise PSD which is a function of operating frequency and the VCO power consumption.

$$\mathcal{L}(f) = \frac{4}{3}\frac{KF}{C_\mathrm{v}}\frac{gm^2}{(C_\mathrm{v}V_\mathrm{v}f_\mathrm{v})I_\mathrm{v}}\frac{f_\mathrm{v}^2}{f^3}$$

$$\mathcal{L}(f) = \frac{4}{3}\frac{KF}{I_\mathrm{v}V_\mathrm{v}f_\mathrm{v}}\left[\left(\frac{gm}{2C_\mathrm{v}}\right)^2 4\right]\frac{f_\mathrm{v}^2}{f^3}$$

$$\text{substituting } f_\mathrm{v} = \frac{gm}{2C_\mathrm{v}}$$

$$\mathcal{L}(f) = \frac{16KF}{3}\left(\frac{f_\mathrm{v}}{I_\mathrm{v}V_\mathrm{v}}\right)\frac{f_\mathrm{v}^2}{f^3} \tag{9.55}$$

Summing (9.48) and (9.55) results in the VCO phase noise PSD given as a function of oscillation frequency and the VCO power consumption, $P_\mathrm{v} = I_\mathrm{v}V_\mathrm{v}$, (9.56).

$$\mathcal{L}(f) = \left[\left(\frac{f_\mathrm{v}}{f}\right)^2\frac{2kT}{I_\mathrm{v}V_\mathrm{v}}\left(1+\frac{2\gamma}{1-\frac{V_{th}}{V_\mathrm{v}}}\right)\right] + \left[\frac{16KF}{3}\left(\frac{f_\mathrm{v}}{I_\mathrm{v}V_\mathrm{v}}\right)\frac{f_\mathrm{v}^2}{f^3}\right]$$

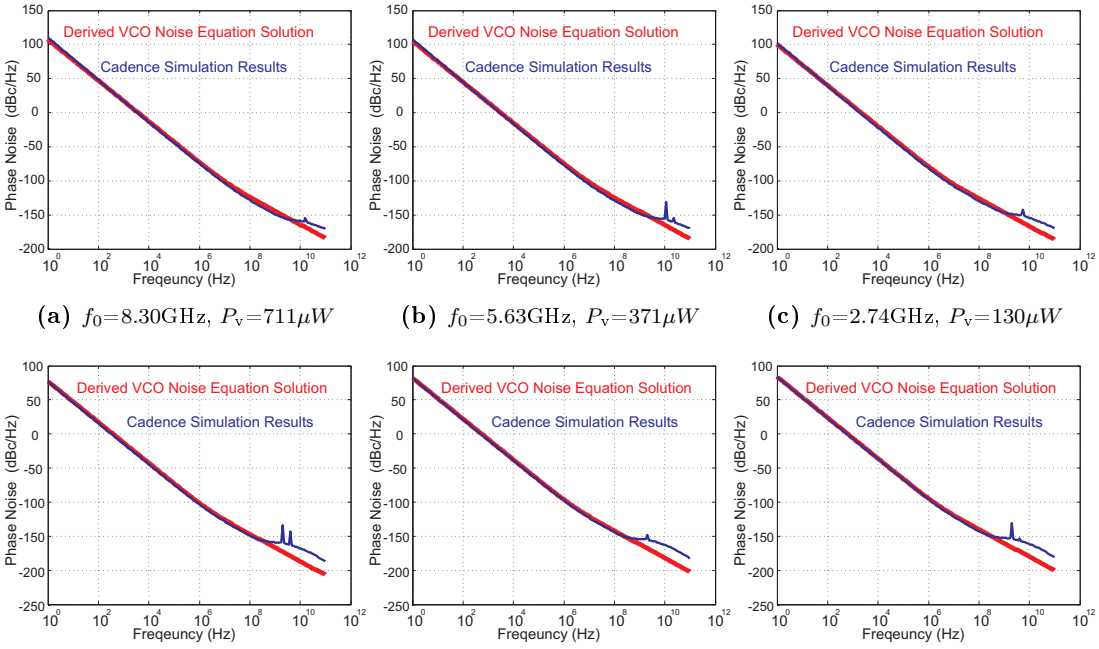
$$\mathcal{L}(f) = \frac{1}{P_\mathrm{v}}\left[\left(\frac{f_\mathrm{v}}{f}\right)^2\left(2kT\left(1+\frac{2\gamma}{1-\frac{V_{th}}{V_\mathrm{v}}}\right)+\frac{16KF}{3}\left(\frac{f_\mathrm{v}}{f}\right)\right)\right] \tag{9.56}$$

The PSD equation can also be used to find the $1/f$ noise corner frequency by equating the white noise and flicker noise to each other and solving for f.

$$\left(\frac{1}{f}\right)_{corner} = \frac{8KF\ f_\mathrm{v}}{3kT\left(1+\frac{2\gamma}{1-\frac{V_{th}}{V_\mathrm{v}}}\right)}$$

The solution to (9.56) requires knowing the value for KF, V_{th}, and γ prior to solving for the phase noise. If these values are unknown, a fairly decent starting point is to assume that KF is at most 10^{-23}, $V_{th} \approx 1/4V_{dd}$ of the technology, and that γ is 2/3 for long channel up to about 1 for short channel (120nm) devices. With these initial starting value approximations, an iterative process of designing a test VCO and performing AC/.Noise analysis on devices biased under the VCO operating conditions will quickly produce the KF, γ, and V_{th} coefficients which can be used in subsequent noise analyses.

Fig. 9.25 shows a few plots where a VCO has been constructed in Cadence design framework, and a pss./pnoise simulation has been run to generate a PSD plot of the



(a) f_0=8.30GHz, P_v=711μW **(b)** f_0=5.63GHz, P_v=371μW **(c)** f_0=2.74GHz, P_v=130μW

(d) f_0=1.0GHz, P_v=1.2mW **(e)** f_0=1.0GHz, P_v=385μW **(f)** f_0=1.0GHz, P_v=258μW

Figure 9.25: VCO noise simulations comparing the Cadence Spectre simulation results with the derived VCO noise solution to (9.56).

VCO simulation results. In Fig. 9.25, the Spectre PSD simulation results and the solution to (9.56) for various VCO's are plotted together for comparison. The first three simulations are the same VCO at different operating frequencies, and the last three simulations are three different VCO's at about the same frequency but with three different power consumption levels.

9.4.5 The Divider Phase Noise

The divider phase noise comes from the digital gate switching noise. The extended modulus divider has several daisy chained $\div 2/3$ cells to perform the divide operation, but MOD_OUT's result is stored in a register and it is clocked out by the VCO output. The reduces the gate propagation from the VCO output to the PFD input to only one gate. Having only one gate of propagation delay helps to keep the divider phase noise down to very small values.

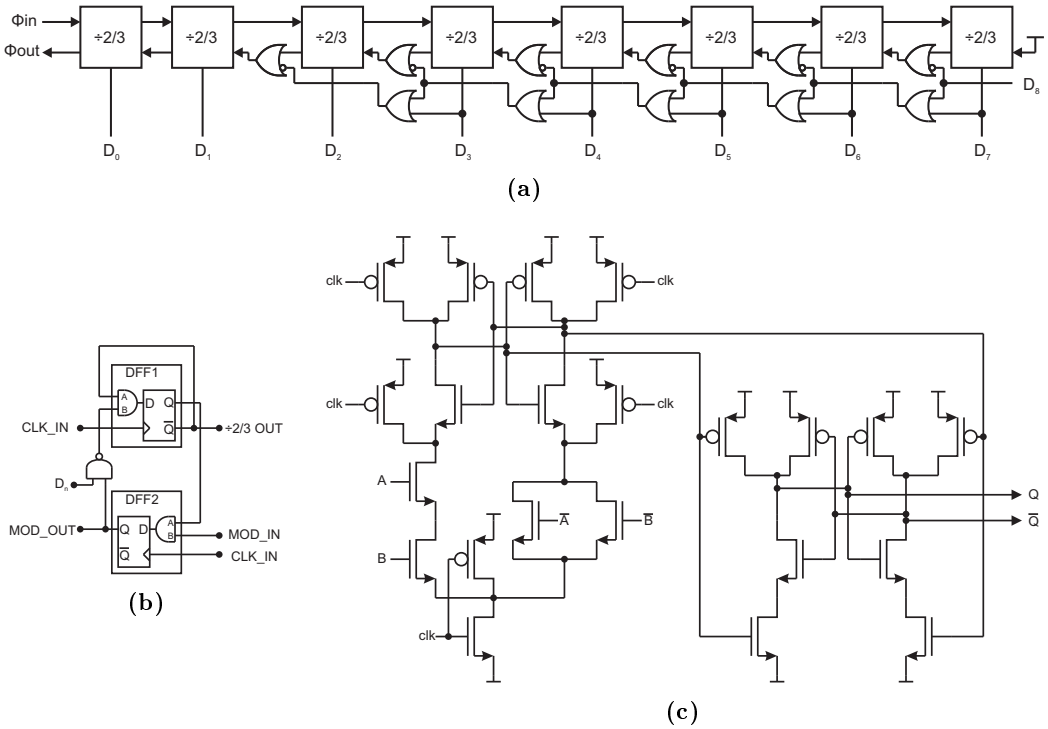


Figure 9.26: The PLL Divider Circuit.
a) The modulus divider.
b) The ÷2/3 divider cell.
c) The StrongARM latch based DFF.

9.4.6 RF Link Noise Budgeting

To know how much phase noise the PLL is allowed to produce, the minimum signal to noise ratio at the receive electronics must be derived. The goal is to transmit 8 Mbps of data from the implant to a receiver located 3 meters away using 8-PSK modulation. The first step is to determine how much signal to noise is required for the receiver to be able to demodulate the data from the carrier.

To be able to extract information from the signal, the received signal energy needs to be greater than the noise floor of the receiver, and how much greater depends on the modulation scheme which is employed. The data transmission scheme employed by the implant is a 8-ary phase shift keying (8-PSK) modulation [55]. This modulation scheme is not the most spectrally efficient, but because of the circuit structure of the PLL's VCO, it is one of the most easily implemented methods of modulation. The function

which describes the probability of symbol error versus the signal to noise ratio of the received signal is:

$$P_{\mathrm{E}} = \frac{1}{\sqrt{2\pi}} \int_{u}^{\infty} e^{-\frac{u^2}{2}} du \quad \text{where } u = \sqrt{2\frac{E_s}{N_0}}\, sin\left(\frac{\pi}{M}\right).$$

The term E_s/N_0 is the signal to noise ratio (SNR) of the transmitted signal as a function of the energy per symbol, E_s, to the received signal's noise content, N_0.

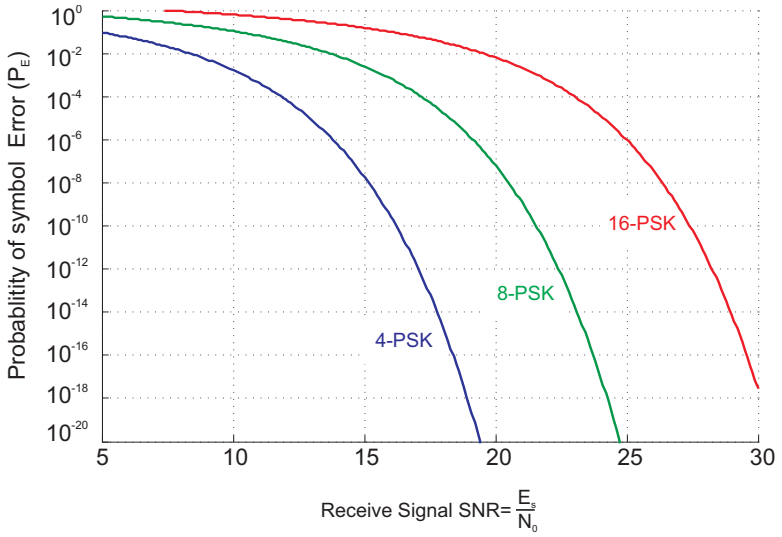


Figure 9.27: The probability of symbol transmission error for 4, 8, and 16 M-ary PSK modulation vs. SNR.

Plotting P_{E} vs. E_s/N_0, Fig. 9.27, will give the received power signal to noise ratio required for various M-ary modulation types for differing levels of bit error probability rates. According to Fig. 9.27, an SNR of about

$$\frac{E_s}{E_0} = 20dB$$

will give about 1 symbol error for every 10^7 symbol transmissions. From the required receiver E_s/N_0 ratio, the RF carrier energy to noise energy ratio, C/N, for the expected bandwidth will be

$$10\log_{10}\left(\frac{C}{N}\right) = 10\log_{10}\left(\frac{E_s}{N_0}\right) + 10\log_{10}\left(\frac{f_s}{B}\right),$$

where f_s is the symbol rate, and B is the channel bandwidth. The implant's RF carrier maximum expected symbol rate to its required channel bandwidth will add about 3dB

of signal to noise ratio requirement. This results in an RF carrier to noise ratio, C/N, of (9.57).

$$f_s = \frac{8 \text{ Mbps}}{3 \text{ bits per symbol}} \approx 2.67 \text{ Msymbols per second}$$

$$B = 2f_s$$

$$10\log_{10}\left(\frac{C}{N}\right) = 20\text{dB} - 10\log_{10}\left(\frac{1}{2}\right)\text{dB} = 23dB \tag{9.57}$$

The received signal to noise ratio will be further degraded by the noise factor, NF, of the receiver electronics. This noise factor can be as low as 3dB, and most receiver's noise factors are much less than 10dB. To be on the safe side, the receiver's noise factor for this link will be set at

$$NF = 10dB.$$

The last step in determining what signal strength needs to be received by the receiver is to calculate the kTB thermal noise energy. This thermal noise floor energy is the amount of noise power that the signal will have to overcome to be able to be demodulated by the receiver. The thermal noise floor energy is the product of Boltzmann's constant $k = 1.38(10^{-23}J/K)$, the temperature in Kelvin, $T = 300K$, and the bandwidth, $B = 2f_s$

$$N_{kTB} = 10\log_{10}\left[1.38(10^{-23})(300)(2 * 2.67(10^6))\right] \approx -144\text{dBW} = -114\text{dBm}$$

For the signal to be demodulated, it must have a signal power which is $C/N + NF$ greater than N_{kTB}, so the minimum received power must be greater than

$$P_{rx_{\min}} = -114 + 23 + 10 = -81dBm$$

Starting with an expression of Friis' transmission equation [55],

$$P_{tx_{\text{dBm}}} = P_{rx_{\text{dBm}}} - \left(G_{tx_{\text{dB}}} + G_{rx_{\text{dB}}} + 20\log_{10}\left(\frac{\lambda}{4\pi R}\right)\right),$$

a value for the minimum transmitter power, $P_{tx_{\min}}$, can be found as a function of the minimum receive power, $P_{rx_{\min}}$, the antenna gains, G_{tx} and G_{rx}, and the propagation loss caused by the the carrier wavelength and transmission distance, λ and R.

The receive antenna gain, $G_{rx_{\text{dB}}}$, for a simple dipole antenna is usually around 1 to 2dB, but for this calculation, it be given a value of 0dB. The transmitter antenna,

$G_{tx_{\mathrm{dB}}}$, because of its small size and location, will probably lose about 90% of its energy for an antenna gain of -10dB. The read range will be set to 3m, and the maximum operating frequency will be set at 1 GHz for a wavelength of 0.30m. The resulting minimum required $P_{tx_{\mathrm{dBm}}}$ for signal detection is

$$P_{tx_{\mathrm{dBm}}} = -81 - \left(-10 + 0 + 20\log_{10}\left(\frac{0.3}{12\pi}\right)\right) \approx -29dBm.$$

This requires an absolute minimum transmission power of about 1μW.

9.5 Meeting the noise requirements

The required SNR, Fig. 9.27, carrier to noise ratio (9.57), and the receive electronics noise factor all sum together to about 33dB. To ensure that this noise requirement is met by the transmitting electronics, the PLL will be designed so that its output integrated phase noise will be less than -33dBc. The PLL output phase noises comes from the summation of all of the PLL phase noise sources, Fig. 9.28, and each PLL control block will need to be designed in a way that optimizes its power consumption vs. phase noise output ratio.

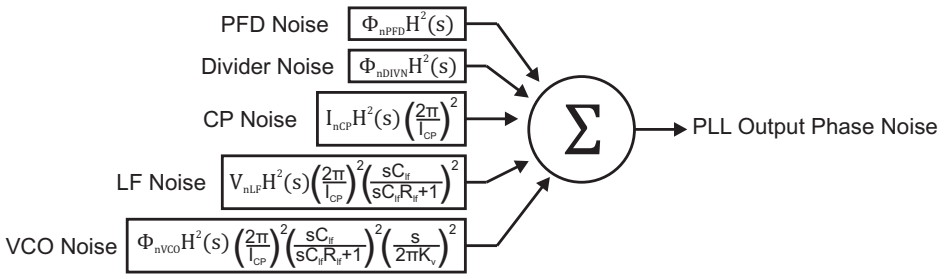


Figure 9.28: The summation of the PLL phase noise sources.

9.5.1 The PFD and the Divider

The PFD and divider are digital logic devices, and as was stated earlier, a noise analysis could determine the required gate sizing and power consumption to meet the noise requirements. However, these devices, even when using minimum sized devices, contribute relatively insignificant amounts of noise when compared to the noise from the VCO and the charge pump.

The PFD and the divider were constructed using minimum sized devices, and then noise simulations were run to get an idea of how much phase noise they will contribute. The results of the noise simulations, and the PLL output phase noise resulting from each device's noise contribution is plotted in Fig. 9.29. The total integrated PLL output phase noise from the PFD and Divider circuits is well below 100dBc.

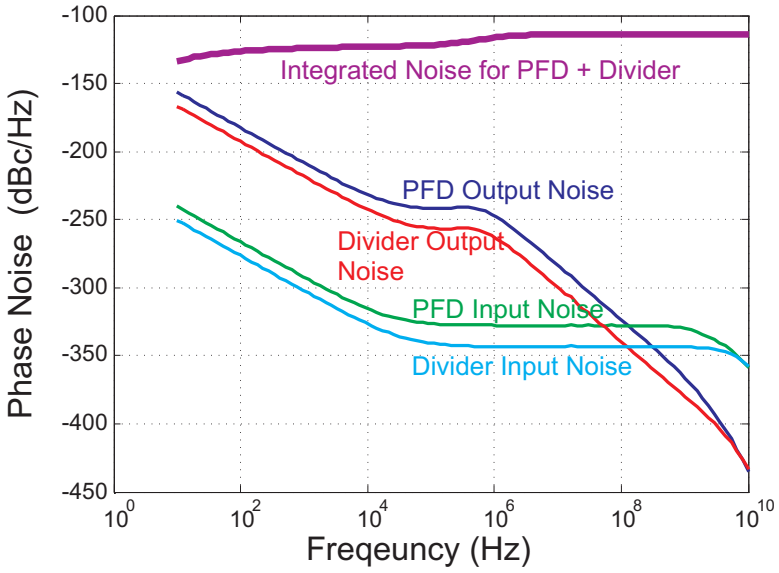


Figure 9.29: The PLL output phase noise from the PFD and divider noise sources.

9.5.2 The VCO, Charge Pump, and Loop Filter

The loop filter noise voltage is

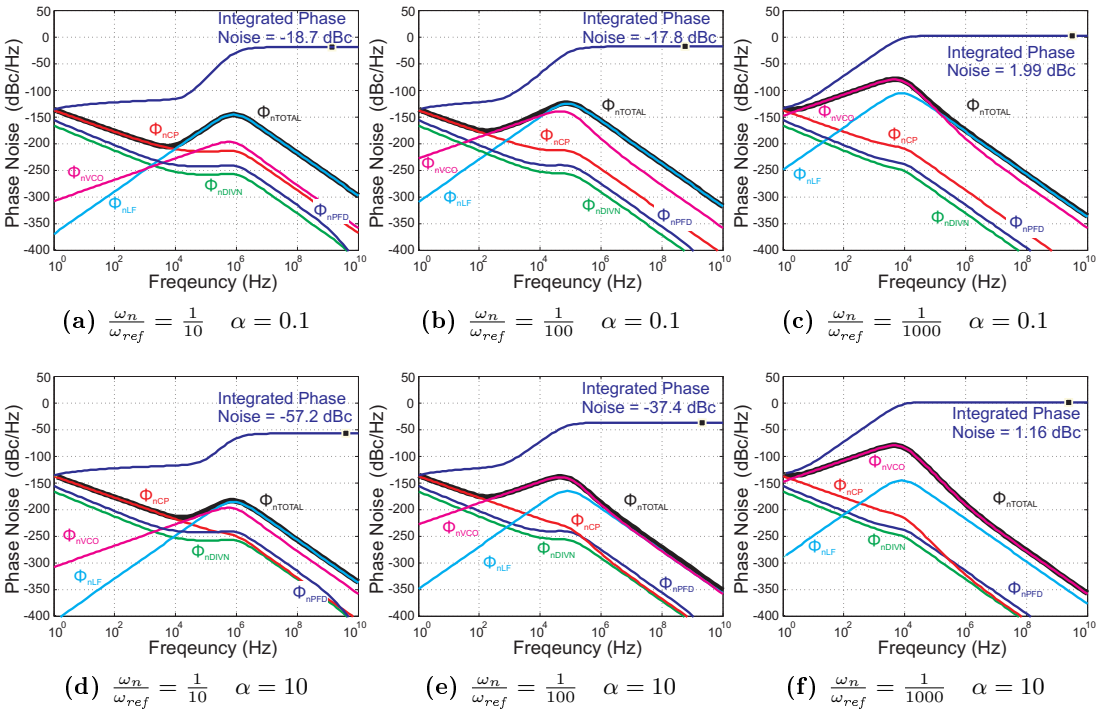
$$V_{\text{lf}}^2 = \begin{cases} 0 & \text{if } j\omega = 0 \\ 4kTR_{\text{lf}} & \text{if } j\omega \neq 0 \end{cases},$$

and the charge pump noise current is

$$I_{\text{nCP}}^2 = 8kT\gamma(\eta_{gm} I_{\text{CP}}) \left(\frac{t_{\text{on}}}{T_{\text{ref}}^2} \right).$$

Both of these noise formulas require prior knowledge of R_{lf} and I_{CP}. Because the PLL is a self-biased design, the actual values of R_{lf} and I_{CP} will be determined by the VCO design. After a VCO design has been chosen according to its I_{v}, V_{v}, C_{v}, and f_{v}, then the R_{lf} and I_{CP} will be calculated, and the noise impact from the charge pump and loop filter can be determined.

Most of the PLL output noise comes from the charge pump and the VCO. Increasing the loop bandwidth decreases the VCO noise while increasing the charge pump noise, and reducing the loop bandwidth decreases the charge pump noise while increasing the VCO noise which makes it to the PLL output. To demonstrate this point, a few Matlab noise analysis simulations were performed with a PLL designed according to the self biased design methodology using a VCO running at 1 GHz consuming 200μW of power referenced from an 8 MHz source. The simulations ran the noise analysis with different values of ω_n/ω_{ref} and different values of the charge pump current ratio self biasing factor α (9.13).



(a) $\frac{\omega_n}{\omega_{ref}} = \frac{1}{10}$ $\alpha = 0.1$ **(b)** $\frac{\omega_n}{\omega_{ref}} = \frac{1}{100}$ $\alpha = 0.1$ **(c)** $\frac{\omega_n}{\omega_{ref}} = \frac{1}{1000}$ $\alpha = 0.1$

(d) $\frac{\omega_n}{\omega_{ref}} = \frac{1}{10}$ $\alpha = 10$ **(e)** $\frac{\omega_n}{\omega_{ref}} = \frac{1}{100}$ $\alpha = 10$ **(f)** $\frac{\omega_n}{\omega_{ref}} = \frac{1}{1000}$ $\alpha = 10$

Figure 9.30: PLL noise simulation results across varying bandwidths and charge pump currents for $f_{ref} = 8\ MHz$.

The plots show that:

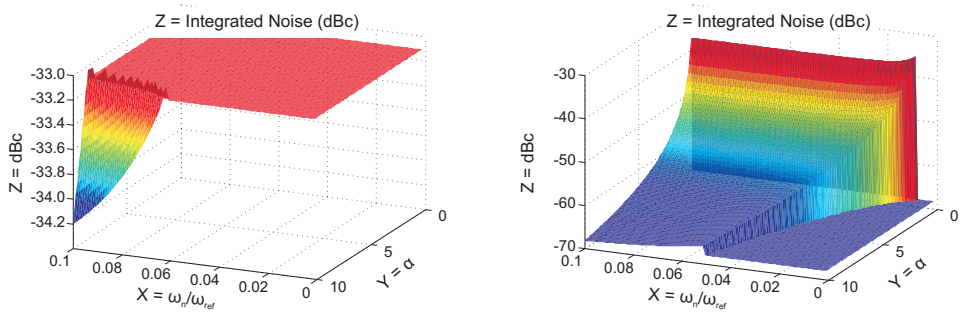
- For wide bandwidth loops ($\omega_n/\omega_{ref} = 1/10$), the total output noise is dominated by the charge pump and loop filter noise contributions.
- For wide bandwidth loops, increasing the charge pump current (which also reduces the loop filter resister value) greatly reduces the PLL noise.

- As the loop bandwidth is made narrower ($\omega_n/\omega_{ref} = 1/100$), the noise from the PLL starts to dominate.
- For very small bandwidth loops ($\omega_n/\omega_{ref} = 1/1000$), VCO noise dominates, and increasing charge pump current has very little effect.

Table 9.1: PLL noise simulation results across varying bandwidth and α ratios showing the charge pump current and required loop filter capacitance.

$\frac{\omega_n}{\omega_{ref}}$	α	dBc	I_{cp}	C_{lf}
10	0.1	-18.7	160nA	51.6fF
10	10	-57.2	16µA	5.16pF
100	0.1	-17.8	160nA	5.16pF
100	10	-37.4	16µA	516pF
1000	0.1	1.99	160nA	516pF
1000	10	1.16	16µA	51.6nF

The goal is to design a low power VCO, and to choose an α design factor and a PLL loop bandwidth which results in a total integrated noise of less than 33 dBc when oscillating at 1 GHz referenced from a 2 MHz clock. Using the PLL noise formulas (Eqs. (9.29) through (9.34)), Matlab was used to generate a couple of 3D surface maps, Fig. 9.31, for a VCO running at 1 GHz consuming 200μW of power. The output of each plot has been limited to display values for dBc < -33, and $C_{\text{lf}} < 12$ pF.



(a) 2 MHz reference **(b)** 16 MHz reference

Figure 9.31: 3D surface plot of the solution of the summation of all of the PLL noise sources.

The 3D surface plot in Fig. 9.31a shows the integrated noise of the PLL when it is referenced from a 2 MHz clock, and Fig. 9.31b is for a PLL with a 16 MHz reference. From the plots, a value for the self biasing factors, α and ω_n/ω_{ref}, can be quickly determined as a function of the integrated output noise and the loop bandwidth tuning parameters. When choosing a value for both of these factors, the compromise for reducing the noise with larger α is a linear increase in charge pump current, and a linear increase in C_{lf}. The noise from the VCO is a dominant noise source for the PLL, so the PLL should be designed with wide bandwidth.

Fig. 9.31a shows that a VCO which consumes 200μW of power at 1 GHz referenced from a 2 MHz clock should meet the noise requirements of the wireless data transmission system.

10

Conclusion

In conclusion, the goal of this project work was to develop a system capable of measuring pressure levels from inside a living body. During the beginning of the project work, a wireless power transmission system capable of transmitting several hundred microwatts of wireless power into the abdominal aorta of a 100kg swine was demonstrated. In February 2012, following the successful in vivo animal test demonstration of proof of concept, work began on the design of a fully integrated system on chip for measuring pressure using capacitive pressure sensors. Now, as the project is nearing completion, the project goal of developing a method for wireless power and data transmission to a medical implant situated inside a living body has been demonstrated. Also, the first prototype of the fully integrated system on chip pressure sensor has been delivered and tested. The chip is capable of sampling pressure with a 0.75 mmHg pressure resolution at 4 ksps while consuming only 5 μA of current per channel. The signal conditioning electronics have been measured and verified that the 10-bit noise accuracy has been achieved, and when sampling at 16 samples per second, the chip is able to resolve altitude differences in the sum 1 meter range. To measure this small pressure differential, the implant electronics are able to measure the capacitive pressure sensor with a capacitive pressure resolution of less than 100 aF.

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