# Receiver Components and Frontends for Wideband Communications at W-Band

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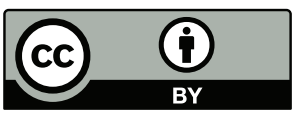

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# Abstract

In this work, an active receiver array is developed and characterized in terms of its far-field characteristics. It supports two circular polarizations, covers the entire W-band from 75 GHz to 110 GHz, and is capable of beam steering. Equipped with the appropriate antennas, the receiver serves the three proposed application scenarios with data rates beyond 100 Gbps.

The array receiver consists of several components, all of which are first designed and analyzed individually. Key requirements for all the components are the high frequency and the large bandwidth while maintaining compact dimensions. The former leads to small geometries requiring tight manufacturing tolerances. The latter calls for innovative concepts especially due to the required compactness.

For each scenario, individual circular horn antennas are designed, adapted to the respective requirements. An advanced septum polarizer with a triangular waveguide enables full W-band coverage with an axial ratio below 1.3 dB. Compact transitions provide the connection between the antennas and the PCB on which the active down converter chip is mounted. The latter amplifies and converts the received signals to the baseband, which ranges from 1 GHz to 36 GHz. The outputs of multiple chips are combined with an integrated power combining network.

The waveguide part of the receiver is built using two different manufacturing processes, both based on 3D printing technologies, and compared in measurements. A single-element receiver and a 2x2 antenna array demonstrate the full complexity of the developed system. Both show good agreement with the values expected from simulations and previous measurements.

# Contents

# 1 Introduction

Wireless communications have experienced dramatic growth in speed and total data usage over the past few decades [1] and are expected to continue to grow [2]. This leads to even higher data rates required with each new generation of communication devices. Modern coding schemes allow bandwidth efficiency close to the channel capacity [3]. According to the Shannon-Hartley theorem [4], the maximum data rate $R$ for an additive white Gaussian noise channel with bandwidth $B$ and signal-to-noise ratio SNR is given by

$$R = B \log_2(1 + \mathrm{SNR}). \tag{1.1}$$

Thus, there are two basic methods of increasing data rate: maximizing the SNR and increasing the bandwidth. All components present in the channel affect its SNR, with the receiver low noise amplifier (LNA) and transmit power being the most important. The transmit power can be increased to improve SNR. However, technological challenges, such as the efficiency of the power amplifier (PA) used in the transmitter, as well as the effective isotropic radiated power (EIRP) and absolute power limits specified by local spectrum agencies, limit this approach, e.g. [5]. Using multiple transmit (TX) and receive (RX) antennas, resulting in an array configuration, improves the antenna gain by the array factor (AF). This is a viable measure to increase the EIRP and thus improve the SNR.

In the receiver, the noise figure of the LNA has the greatest impact on the total SNR. State-of-the-art, low-noise components must be used here. The best noise figures down to 2 dB in the W-band are achieved with devices based on materials such as gallium arsenide (GaAs), gallium nitride (GaN) or indium phosphide (InP) [6–8]. Compared to complementary metal-oxide-semiconductor (CMOS), devices based on the former materials are relatively expensive. When targeting the mass market, CMOS is usually

the technology of choice. Recent CMOS-based W-band LNAs achieve noise figures as low as 4.6 dB [9, 10].

The second approach, increasing the bandwidth, is somewhat difficult to apply to systems operating at low frequencies, such as a wireless local area network (WLAN) operating at 2.4 GHz. Here, only a few hundred MHz around the center frequency can be occupied. The logical consequence is that an increase in bandwidth is usually accompanied by an increase in carrier frequency. This work focuses on the W-band from 75 GHz to 110 GHz, which is particularly well suited for broadband communications due to the absence of atmospheric absorption peaks [11]. Here, 35 GHz of raw bandwidth is available, allowing for enormous data rates. However, the increased path loss and tight manufacturing tolerances due to the small wavelength pose a major challenge. In addition, the relative bandwidth of 37.8 % requires well-designed broadband components throughout the signal path.

The use of multiple-input multiple-output (MIMO) strategies also allows higher data rates without occupying a larger spectrum, but by using multiple spatial channels, providing in total more data rate than a single traditional channel [12]. This technique requires more signal processing effort in the digital domain, especially when large bandwidths are involved.

In this work, the classical approach to increase the bandwidth while optimizing the SNR is carried out. Making the developed system MIMO compatible requires some design changes. However, for MIMO at millimeter-wave frequencies, hybrid architectures can be advantageous [13]. Here, large parts of the system developed in this thesis could be reused.

### Structure of this Work

This work focuses on the development of active receivers covering the entire W-band from 75 GHz to 110 GHz using CMOS down-converters.

Chapter 2 describes the basic concept for a W-band receiver with a potential data rate of more than 100 Gbps as well as possible application scenarios. The general transmission chain is described and the receiver architecture is explained.

Chapter 3 gives detailed descriptions of the components involved in the receiver design, i.e., antenna, polarizer, transition, down converter, and power combiner. For all components, broadband performance is a key requirement within the design process.

Individual components are fabricated and characterized. Conventional manufacturing techniques such as precision metal milling and PCB etching are used, as well as new processes, such as integrated carbon resistors or copper waveguide components based on 3D printed molds.

In Chapter 4 the developed components are combined to a dual-polarized receiver. First, the passive circularly polarized antenna with transition to PCB is designed and characterized in an anechoic chamber. Two different antenna realizations are presented and compared. One is fabricated in-house using a low-cost process, while the other is fabricated using a commercially available high-precision metal 3D printing process. The active receiver, including the CMOS down-converter, is first developed with a single antenna. Then, a 2x2 array receiver with an integrated power combining network is built. Detailed descriptions of the measurement setup and the results themselves for the far-field characteristics of the active receivers, such as realized gain, axial ratio, and radiation patterns, are given.

Finally, Chapter 5 concludes this work and gives an outlook on further interesting aspects that are not treated in detail here.

# System Overview 2

This work focuses on the communication system concept proposed in [14] with an expected data rate of 100 Gbit/s. With two circular polarizations, two separate channels only need to cover half the data rate each. When beam steering is used individually in an array configuration, the two polarizations can be targeted to different users. In a multiuser scenario with more than two users, the full 100 Gbit/s capacity is shared via time division multiplexing. The selected frequency range from 75 GHz to 110 GHz requires a direct line-of-sight connection. Therefore, the application scenarios based on this approach are short to medium range indoor links. Three main scenarios, illustrated in Fig. 2.1, are identified in [14]. These scenarios are defined in detail as:

Scenario 1: Short distance single-user link
The use case is wireless connections between two devices that are closer than 1 m. This replaces cables for high-speed interfaces such as USB, HDMI, or Ethernet used for hard drives and other accessories connected to a personal computer (PC). Alignment over such short distances is not critical. Therefore, this scenario requires only a narrow angular coverage of ±15°.

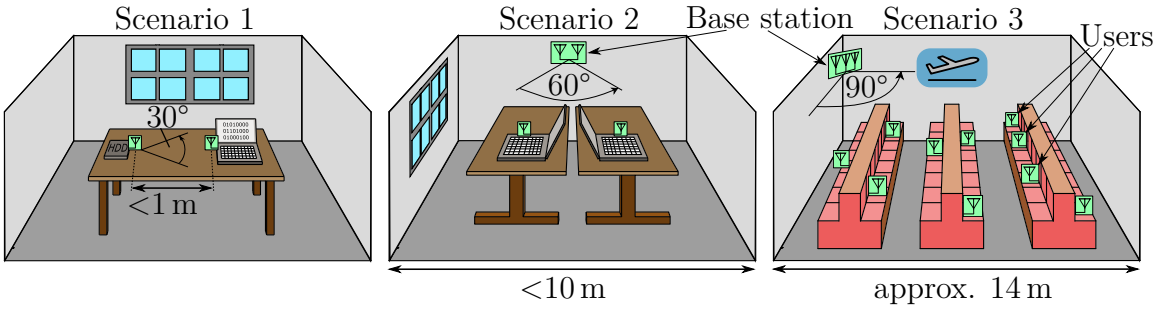



Figure 2.1: Illustrated application scenarios for a high data rate indoor line-of-sight communication system.

Scenario 2: Short distance multiuser link
This scenario occurs in small offices where several fixed users are provided with a high-speed connection at a maximum distance of 10 m. Dark spots are accepted because the system is coarsely aligned during setup. The required scan angle is ±30°.

Scenario 3: Medium distance multiuser link
The most challenging scenario is a multiuser airport or train station concourse. Here, the base station serves a large number of users in a large area, resulting in a long range of up to 20 m and a wide angular coverage of ±45°.

Table 2.1 summarizes the scenarios and their constraints. The number of array elements required on both sides of the link is calculated assuming the use of horn antennas. For high element count arrays, the use of planar antennas, such as slot or patch antennas, is usually the most cost effective choice. A multilayer PCB is required in most cases anyway, and in the stack high performance laminates can be combined with cheaper FR4 to have the expensive material only where it is needed [15]. Although planar antennas achieve high relative bandwidth [16], they have higher losses and lower gain compared to horn antennas [17]. However, due to their 3D structure, horn antennas are typically manufactured using serial manufacturing processes such as milling. Modern manufacturing techniques such as high-precision 3D-printed polymers with integrated electronics [18–20] allow the realization of complex systems with 3D structures in batch processes suitable for the consumer market targeting mass production. New 3D printing and metallization processes are particularly useful for waveguide components such as horn antennas [21, 22]. They can be cheaply printed and metallized

Table 2.1: Scenario-specific system properties, according to [14].

| | **Max. dist.** | **Scan angle** | **Link type** | **Antenna array size**[a] | **Antenna array size**[b] |
|---|---|---|---|---|---|
| **Scenario 1** | 1 m | ±15° | single-user | 2 | 2 |
| **Scenario 2** | 10 m | ±30° | multiuser | 10 | 5 |
| **Scenario 3** | 20 m | ±45° | multiuser | 19 | 8 |

[a] For 100 Gbit/s with QPSK modulation and a single receive element.
[b] For 100 Gbit/s with QPSK modulation and the same array topology for TX and RX.

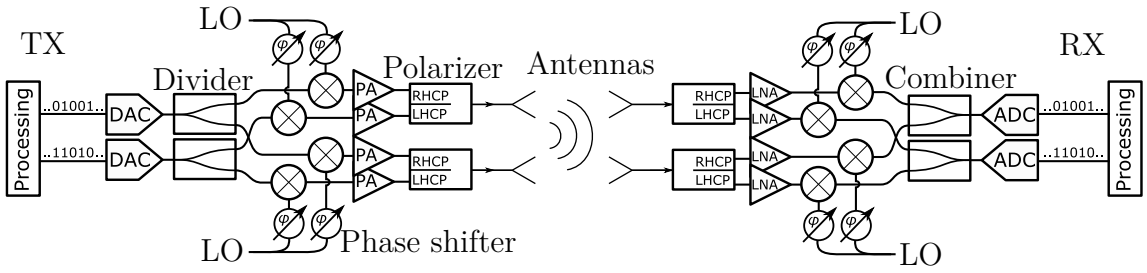



Figure 2.2: Block diagram of the components involved in the high-speed wireless link. Exemplary for the transmitter as well as the receiver a two element array is drawn.

in mass production. This work takes a hybrid approach, with the active components on a regular PCB and the more complex shaped components, such as polarizers and antennas, 3D printed and mounted on the PCB.

Figure 2.2 outlines the block diagram of the complete communication link, with the transmitter on the left and the receiver on the right. A processing unit generates the bit sequences to drive the digital-to-analog converters (DACs). The analog output signals are split and routed to the up-converting mixers. A local oscillator (LO) signal with an individual phase shifter in each path drives the mixers. This provides beam steering capabilities in the array configuration. After the mixer, the up-converted signal passes through a PA as the final amplification stage at the transmit end. Next, a polarizer produces the right and left hand circular polarizations (RHCP & LHCP), which are ultimately radiated by a common antenna. At the receiver end, the process is reversed. The antennas receive the signals and the polarizer separates the RHCP and LHCP components. An LNA provides some amplification before down-conversion to keep the receiver noise figure low. Again, each mixer LO has a phase shifter to allow beam steering at the receiver end, too. The baseband signals of the two polarizations are combined separately and then fed to individual analog-to-digital converters (ADCs), which output a bit stream to a processing unit. This block diagram shows only the main components. In practice, additional amplifiers and transitions are required.

The scope of this work includes only the analog part of the receiver of the proposed communication system, i.e. all components up to the ADC. However, as can be seen from the block diagram, all passive components, i.e. power divider, polarizer and antenna, are used for both the receiver and the transmitter. Therefore, basically only the active components need to be replaced to develop a transmitter based on the passive components developed in this work.

# Wideband Receiver Components 3

This chapter describes all the components required for the receiver in the order in which they appear in the signal path, starting with the antenna. Fig. 3.1 shows an exemplary receiver array with two antennas as a block diagram. The first component in the receiver chain, starting from the left, is the antenna followed by the polarizer. The antenna must cover the entire solid angle of choice (see scenario definition in Chapter 2) with a maximum gain. The design must also ensure that it does not alter the two received circular polarizations, as this would degrade the axial ratio. The next component is the polarizer. It must separate the two polarizations with the best possible cross-polar discrimination. The antenna and polarizer are designed in waveguide technology, while the CMOS receiver chip is mounted on a PCB. Consequently, transitions must be designed from the polarizer waveguide output to the PCB and from the PCB to the chip. On the chip, the received signal is amplified and downconverted to the intermediate frequency (IF) using an external local oscillator (LO). In an ar-

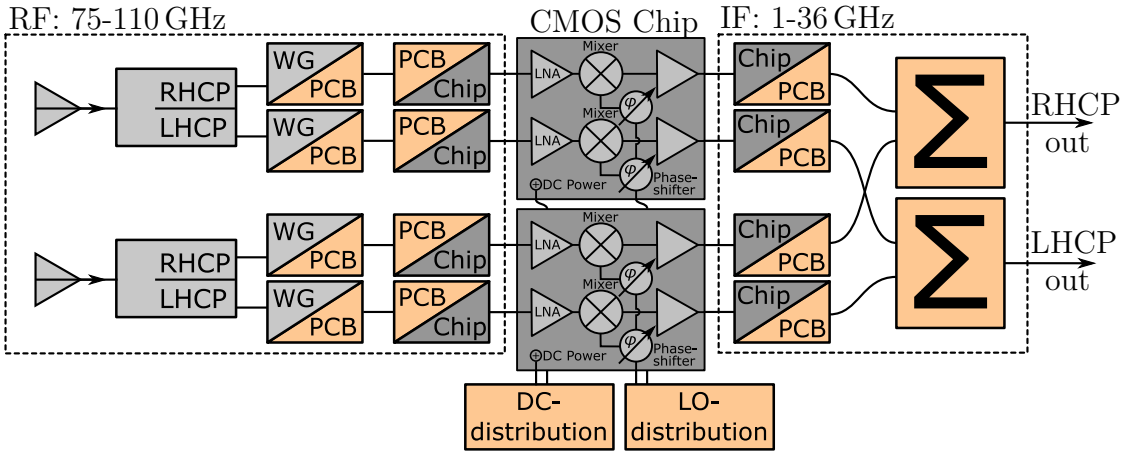



Figure 3.1: Simplified block diagram of an exemplary receiver with two receiving antennas and all components involved in the down-conversion process.

ray scenario, multiple antennas and down-converters operate in parallel and a power combining network sums up the IF signals. Directly after the polarizer, a path for each polarization is provided for each antenna element. Thus, many components have multiple occurrences in the design. The final outputs of the complete receiver are the combined IF signals for RHCP and LHCP.

## 3.1 Antenna

For each of the three scenarios a separate antenna is optimized for gain and axial ratio versus frequency over its corresponding solid angle, as shown in Fig. 3.2 [14].

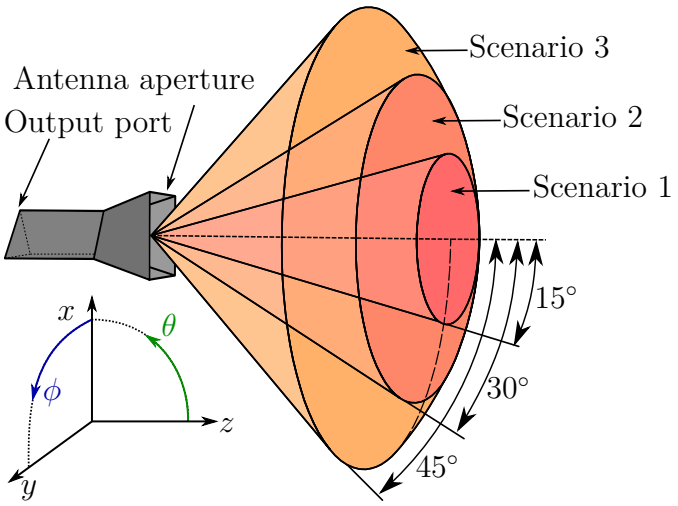



Figure 3.2: Definition of solid angles for the three analyzed scenarios: Scenario 1 with $|\theta| \leq 15°$, Scenario 2 with $|\theta| \leq 30°$, and Scenario 3 with $|\theta| \leq 45°$. The horn antenna is given for visualization purpose only and does not represent the actual designed antennas.

### 3.1.1 Antenna Aperture

The first step is to define the aperture of the antenna. Three different shapes are considered: triangular, square, and circular. The output port of the antenna is chosen as an equilateral triangular waveguide because of the higher available bandwidth between fundamental and higher order modes [23], which is advantageous in combination with a polarizer. Thus, a triangular radiating aperture would facilitate the tapering from

the triangular output port. On the other hand square and circular horns are widely used and well understood.

To define the ideal aperture, the minimum gain $G$ and the maximum axial ratio $AR$ are evaluated for all three scenarios and shapes over the scenario specific solid angle and frequency range. While $\phi$ ranges from 0° to 360°, $f$ ranges from 75 GHz to 110 GHz, and $\theta$, depending on the scenario, from 0° to 15°, 0° to 30°, or 0° to 45°. In the simulation there are no performance differences between RHCP and LHCP due to the perfect symmetry. Therefore, only one polarization needs to be studied.

Figure 3.3 shows the minimum gain and the maximum axial ratio for the three aperture shapes for a perfect circular polarized excitation of the antenna aperture. To get a fair comparison for different shapes, both the gain and the axial ratio are plotted against the aperture area. The evaluation starts with the antenna area for which the fundamental mode cutoff is at 75 GHz. However, operation close to cutoff is not desirable because it leads to higher losses, deteriorates the antenna matching, and introduces strong dispersion.

In terms of the minimum achieved gain, the three shapes perform quite similarly, with a slight advantage for the circular shape. This is due to the higher aperture efficiency associated with this shape [24]. In terms of axial ratio, the circular aperture clearly outperforms the other two apertures for all three scenarios. Therefore, the circular aperture is chosen for the following antenna designs.

Regarding the diameter for each scenario, a compromise must be found between maximum gain and minimum axial ratio.

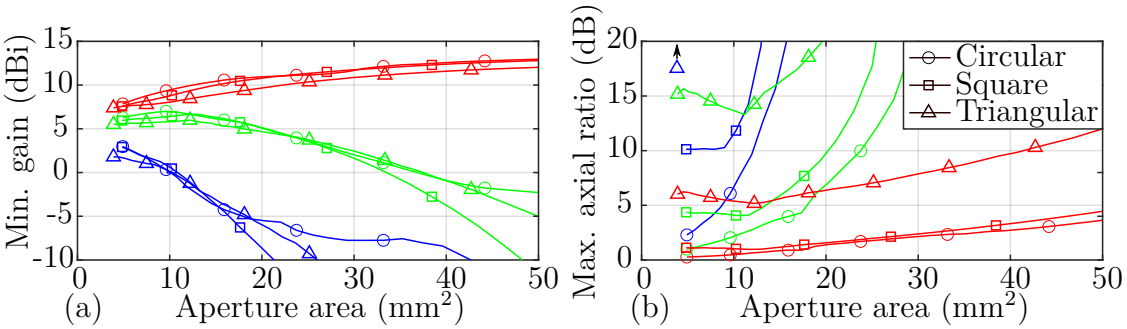



Figure 3.3: (a) Minimum gain and (b) maximum axial ratio over the solid angle of interest and frequency for Scenario 1 (red), Scenario 2 (green), and Scenario 3 (blue). Triangular, square, and circular aperture plots are marked with corresponding line markers.

Table 3.1: Resulting minimum gain and maximum axial ratio for circular apertures of chosen parameters.

| | **Min. gain (dBi)** | **Max. $AR$ (dB)** | **Area ($mm^2$)** | **Diameter (mm)** |
|---|---|---|---|---|
| **Scenario 1** | 10.7 | 0.9 | 17.3 | 4.7 |
| **Scenario 2** | 7.0 | 2.0 | 9.6 | 3.5 |
| **Scenario 3** | 2.5 | 2.7 | 5.7 | 2.7 |

Table 3.1 summarizes the parameters obtained from the aperture analysis. For Scenario 1, the gain increases monotonically even beyond 50 $mm^2$. Therefore, the largest possible aperture should be chosen. However, the axial ratio also increases with the aperture size. An aperture area of 17.3 $mm^2$ (corresponding to a diameter of 4.7 mm) is chosen because the axial ratio remains below 1 dB, which is considered as acceptable here.

For Scenario 2, a minimum gain of 7.0 dBi is achieved for an aperture of 9.6 $mm^2$ (corresponding to a diameter of 3.5 mm), while the axial ratio is 2.0 dB. Reducing the aperture size improves the axial ratio only slightly. Thus, a diameter of 3.5 mm is used for the second scenario.

The axial ratio rises steeply even for small apertures for Scenario 3. Therefore, an aperture of 5.7 $mm^2$ (corresponding to a diameter of 2.7 mm) is chosen. In this case, the cutoff is at 65 GHz, which provides a sufficient distance to the W-band. The resulting minimum gain is 2.5 dBi and the maximum axial ratio is 2.7 dB

### 3.1.2 Antenna Taper

The taper is the waveguide section that connects the antenna aperture to the triangular output port. To receive two circularly polarized waves from a transmitter, the antenna must allow two degenerate modes to propagate to the output. Figure 3.4 depicts the electric fields of the two fundamental modes in the triangular waveguide. If both modes have the same magnitude and are 90° out of phase, a circular polarization is present. The antenna taper is designed using the fundamental modes. This is a valid approach because the combination of both can realize both circular and elliptical polarizations, depending on the phase and magnitude difference.

The taper has to meet two requirements, i.e., to match the different waveguide sections and to prevent the excitation of higher order modes. For both requirements, a

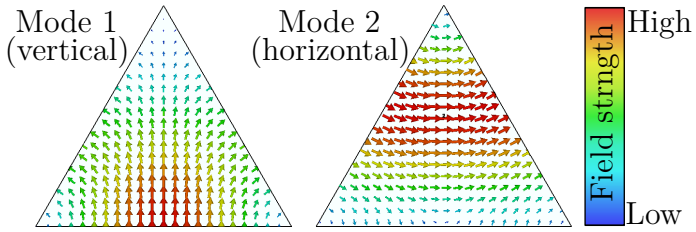



Figure 3.4: Electric field of fundamental modes in an equilateral triangular waveguide.

long and smooth taper is advantageous. However, a longer taper also results in higher losses and increased manufacturing costs. Therefore, the shortest taper with sufficient matching and higher mode suppression must be found. A maximum reflection coefficient of $-15\,\mathrm{dB}$ and a transmission into higher modes of $-20\,\mathrm{dB}$ are considered to be sufficient for the application and are the target values for the taper. A simulation with waveguide ports at both ends of the taper evaluates the performance of the taper. The triangular port (Port 1) is excited with the two fundamental modes and the transmission to all higher order modes at the second port (Port 2) is calculated to

$$S_{\text{higher modes},M} = \sqrt{\sum_{i=3}^{\infty} S_{2(i),1(M)}^2} \quad , \qquad M = 1, 2 \tag{3.1}$$

where $S_{2(i),1(M)}$ is the scattering parameter that defines the transmission from mode $M$ at Port 1 to mode $i$ at Port 2. To include the contribution of all higher order modes, an infinite number of modes must be considered. In practice, however, only the first 20 modes are summed, because even more higher modes do not make a significant contribution due to their small amplitude.

The taper from the equilateral triangular waveguide to the circular aperture is realized in this work by means of an exponential taper. Therefore, the equilateral triangular waveguide is first expressed in cylindrical coordinates by

$$r_{\text{tri}}(\alpha) = \frac{h_{\text{WG}}/3}{\cos(60° - (\alpha \bmod 120°))}, \tag{3.2}$$

with the parameter definitions according to Fig. 3.5. The height of the waveguide $h_{\text{WG}}$ is 2.54 mm. The value originates from the polarizer design in Section 3.2. The equation that defines the shape of the exponential taper is

$$r_{\text{taper}}(\alpha, z) = r_{\text{tri}}(\alpha) + \left(\frac{D_{\text{out}}}{2} - r_{\text{tri}}(\alpha)\right) \frac{\mathrm{e}^{\frac{z}{l_{\text{t}}} t_{\text{exp}}} - 1}{\mathrm{e}^{t_{\text{exp}}} - 1}, \tag{3.3}$$

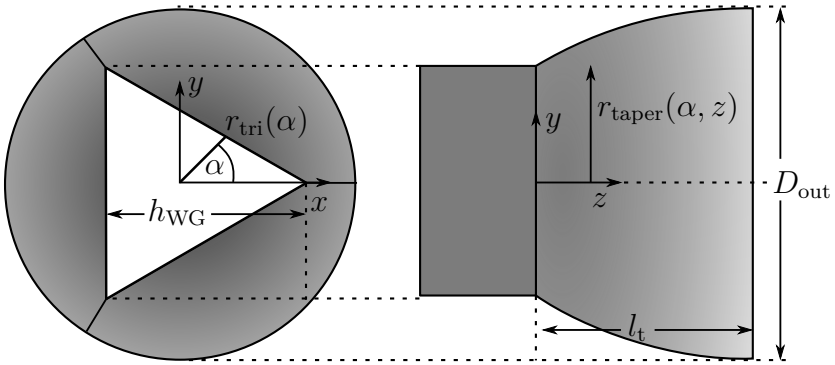



Figure 3.5: Definition of the exponential triangular to circular taper.

Table 3.2: Taper parameters for the three scenarios with resulting reflections and higher order mode transmission.

| | $D_{\mathrm{out}}$ | $l_{\mathrm{t}}$ | $t_{\mathrm{exp}}$ | $S_{1(1),1(1)}, S_{1(2),1(2)}$ | $S_{\text{higher modes},M}$ |
|---|---|---|---|---|---|
| **Scenario 1** | 4.7 mm | 9.7 mm | -1.4 | $\leq -26$ dB | $\leq -20$ dB |
| **Scenario 2** | 3.5 mm | 5.7 mm | -1.2 | $\leq -24$ dB | $\leq -20$ dB |
| **Scenario 3** | 2.7 mm | 3.2 mm | -2 | $\leq -13$ dB | $\leq -20$ dB |

where $t_{\mathrm{exp}}$ is the exponential factor. In this way, each point of the triangular waveguide is exponentially tapered towards the circular radiating aperture.

The three aperture sizes from Table 3.1 are simulated to find the parameters given in Table 3.2 for the taper length $l_{\mathrm{t}}$ and the exponential factor $t_{\mathrm{exp}}$. Note that in this simulation, $S_{1(1),1(1)}$ and $S_{1(2),1(2)}$ are not the reflection coefficients of the antenna radiating into free space. They denote the reflection caused by the taper connecting the circular aperture to the triangular waveguide. All targets are met except for the matching in the case of Scenario 3. However, the matching misses the target only in a very small frequency range from 75 GHz to 77 GHz. Beyond that, the target of 15 dB is met, so the performance of the taper is considered acceptable. The critical factor in the design of the taper, which mostly determines its length, is the transmission to higher modes. For Scenario 1 and Scenario 2, matching better than 15 dB could be achieved with a much shorter taper, but to meet the higher mode transmission goal, the specified length is required.

### 3.1.3 Complete Antenna

To evaluate the performance of the complete antenna shown in Fig. 3.6, antenna simulations are conducted. Therefore, a perfect circular polarization feeds the triangular

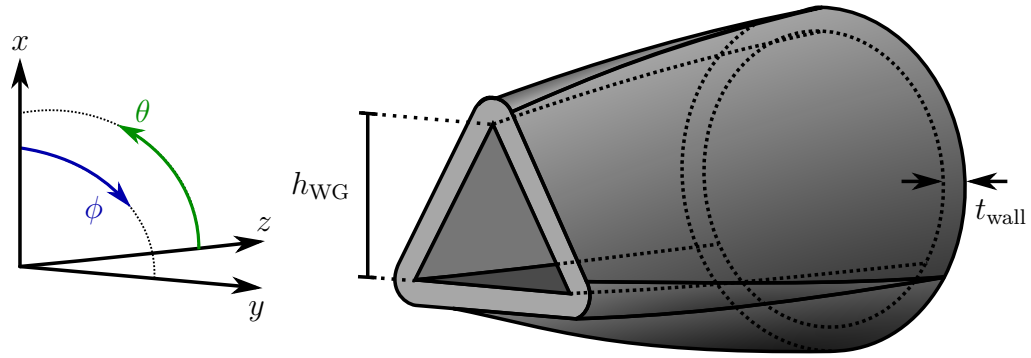



Figure 3.6: 3D view of the antenna with triangular feed and exponential taper.

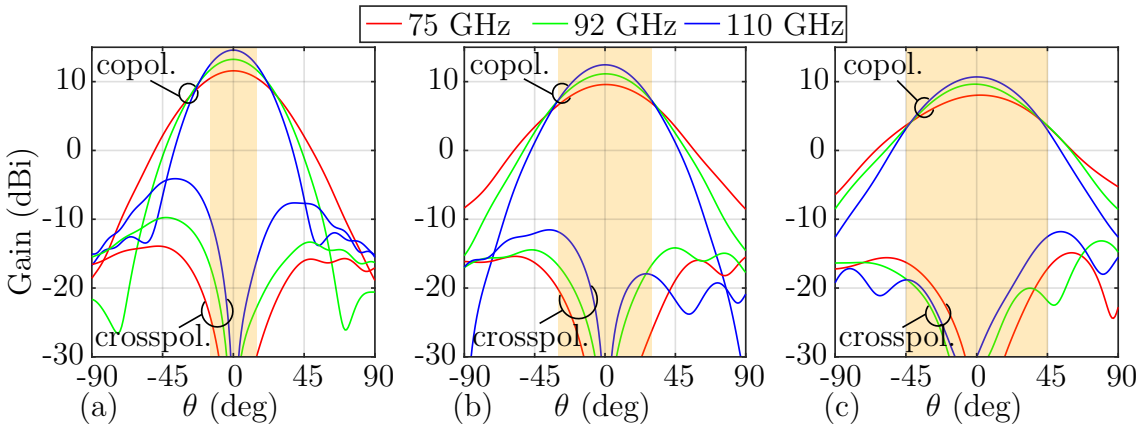



Figure 3.7: Gain of the co- and cross-polarization given exemplary in the $xz$-plane ($\phi = 0°$). (a) Scenario 1, (b) Scenario 2, and, (c) Scenario 3. The respective azimuthal range of interest is highlighted in orange.

waveguide port. The wall thickness of the antenna $t_{wall}$ is 0.4 mm, as this is a realistic value for an additive manufacturing approach.

Figure 3.7 depicts the circular polarized gain for the three designed antennas. A good discrimination of co- and cross- polarized waves in the angular range of interest is achieved for all three scenarios. The main lobe width also adapts well to the respective scenario.

Figure 3.8 shows the properties of the three antennas versus frequency for a circular polarized excitation at the triangular port. The matching at this port is better than 20 dB in all cases except at 75 GHz in Scenario 3, where only 13 dB is achieved in a small fraction of the bandwidth. The worst case axial ratio over frequency and solid angle is slightly increased compared to the aperture-only simulation due to the influence of the taper. The highest values over frequency are 1.7 dB for Scenario 1, 2.3 dB for

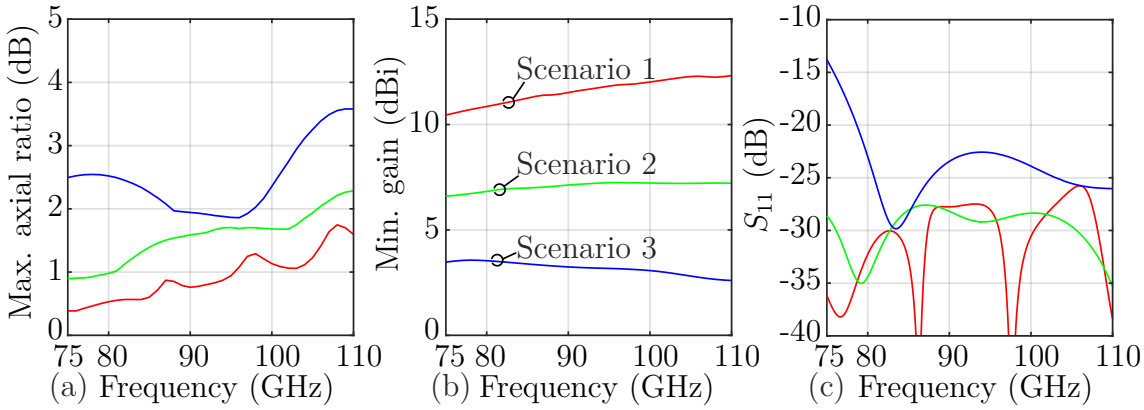



Figure 3.8: (a) Maximum axial ratio, (b) minimum gain, and (c) reflection coefficient of the antenna radiating in free space over the solid angle of interest and frequency for Scenario 1 (red), Scenario 2 (green), and Scenario 3 (blue).

Scenario 2, and 3.6 dB for Scenario 3. Compared to the aperture-only simulation, the gain is not significantly changed by the taper.

## 3.2 Polarizer

The purpose of the polarizer is to separate the two circular polarizations received by the antenna and direct them to two separate ports. It consists of a common port where at least two fundamental modes can propagate, an output section with two single mode ports, and an intermediate transition region. There are several ways to realize such a device.

Turnstile orthomode transducers (T-OMT) are widely used for dual-polarized applications requiring high cross polar discrimination. Such polarizers have been demonstrated in several frequency bands covering more than 56 % of relative bandwidth [25–28]. The integration of T-OMTs into a large antenna array is not possible due to the complex and large structure. The Bøifot junction and its derivatives [29, 30] achieve similar performance, while being more compact, making array integration feasible but still requiring complex waveguide structures [31]. However, these polarizer types usually separate only two linear polarizations and require an additional polarizing element such as a quad-ridged or double-ridged polarizer [32, 33].

Septum polarizers, on the other hand, are very compact and can be used in large antenna arrays due to their simple structure [34]. They directly support two circular polarizations instead of just two linear polarizations. Septum polarizers are well un-

derstood and have been continuously improved in terms of bandwidth and polarization purity. The first septum polarizers used a sloping septum [35]. A stepped septum [36] gave a strong improvement in terms of isolation for the two monomode ports. Modern realizations typically use stepped or functionally shaped septa in square waveguides [37–39]. However, their achievable bandwidth is limited to about 30 % due to the propagation of higher order modes in the common waveguide [40]. Square waveguides offer 34 % and circular waveguides 27 % of relative bandwidth between the fundamental and next higher order modes [41]. In a realistic design, the operating frequency range must have some margin to the fundamental and higher order cutoff to reduce losses and keep dispersion low. Thus, designs based on square or circular waveguides can hardly achieve more than 30 % bandwidth. The advanced design presented here was previously published in [23].

### 3.2.1 Bandwidth-Enhanced Septum Polarizer

A septum polarizer requires a waveguide that allows the propagation of two spatially orthogonal modes with the same propagation constant to support circularly polarized waves. Complex cross sections such as quad-ridged square waveguides can be used to change the cutoff frequencies, but will not provide more relative bandwidth between the fundamental cutoff and the higher mode cutoff [42]. Using a regular polygon as the waveguide cross section, the relative bandwidth can be increased to 53.5 % for an equilateral triangle. Figure 3.9 shows the bandwidth for polygons with three to twelve edges. It turns out that the equilateral triangular waveguide is the best choice in terms of bandwidth for designing a septum polarizer [23]. The two fundamental modes in an

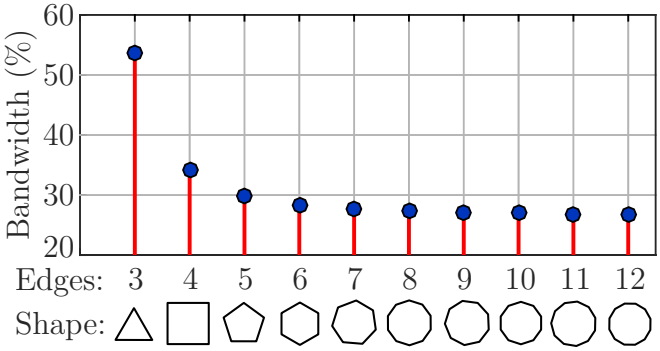



Figure 3.9: Relative bandwidth between fundamental and higher order mode cutoff for regular polygonally shaped waveguides.

equilateral triangular waveguide are shown in Fig. 3.4. The first mode has its fields oriented mostly vertically and the second mostly horizontally, so they are referred to as vertical and horizontal modes in the following. A detailed description of the electric fields in a triangular waveguide can be found in [43].

The analysis of equilateral triangular waveguide cavities for wide spurious-free filters in [44] reveals higher losses in triangular waveguides compared to square or circular cavities. Thus, for a septum polarizer based on an equilateral triangular waveguide the additional bandwidth comes at the expense of slightly higher losses.

Inserting an infinitesimally thin septum at the bottom edge or in the top corner of the triangular waveguide affects the propagation constant of the vertical mode but not that of the horizontal mode. Figure 3.10 faces the two possibilities for the ridge placement. The green shaded area marks the region where the full waveguide bandwidth is usable without propagable higher order modes. If the septum is placed in the corner (Fig. 3.10a), the fifth mode's cutoff decreases rapidly above a ridge height of 20 %. At a ridge height of 40 % the usable bandwidth decreases to 26 %. A septum placed at the edge (Fig. 3.10b) allows for a much larger design space of up to 50 % septum height while maintaining a large usable bandwidth. More important for the design is to have different propagation constants of the two fundamental modes in order to accomplish a 90° phase shift at the common port of the septum polarizer. Since the propagation constant is directly related to the cutoff frequency, an unequal cutoff for the two fundamental modes is indispensable. This is only the case when the septum is placed at the bottom edge.

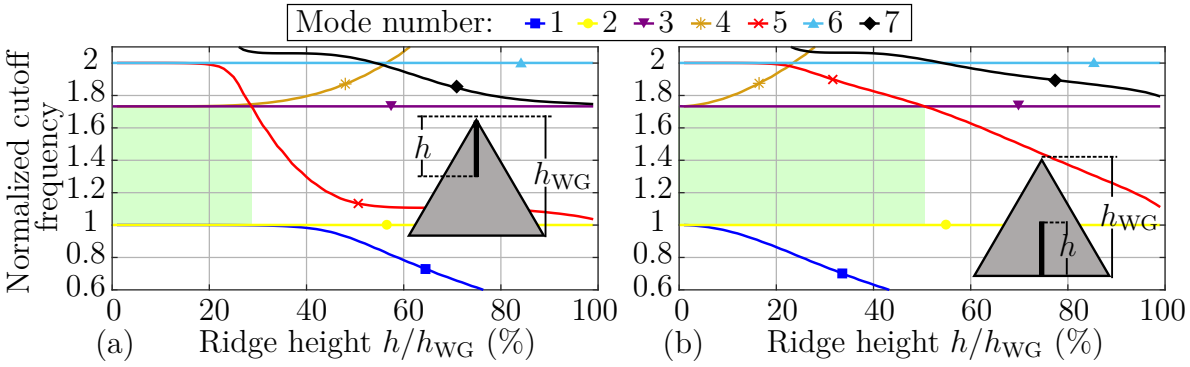



Figure 3.10: Influence of the height and position of the septum on the cutoff frequency of the relevant fundamental and higher order modes in the triangular waveguide. (a) Septum placed at the corner, (b) septum placed at the edge.

### 3.2.2 Polarizer Design

For a manufacturable design, the septum must have a certain thickness. Inserting a thick septum at its full height into an equilateral triangular waveguide leads to a decreased effective waveguide height. This, in turn increases the cutoff frequency for the fundamental mode in both halves of the waveguide, as shown in Fig. 3.11.

To circumvent this problem and also to provide ports matching the measurement equipment, a transition from the WR10 rectangular waveguide to the triangular output port of the polarizer is introduced in the septum region. As demonstrated in [23], a two step taper is sufficient to achieve full W-band matching of better than 20 dB. The WR10 waveguide has a height of 2.54 mm. The same height is used for the triangular waveguide to simplify the interface. This results in a fundamental cutoff frequency of 68.1 GHz and a cutoff at 118 GHz for the higher order modes in the triangular waveguide. This choice maintains sufficient distance to the upper and lower ends of the W-band. In simulation, the thinnest possible septum performs best, but it also complicates fabrication. As a compromise, a septum width of 0.35 mm is used in this design. The inner corners of the two transition steps have a radius $r_0$ of 0.4 mm. This allows for machining with milling tools.

Figure 3.12 depicts the designed septum polarizer with the parameters defining the geometry. Constrained optimization in full-wave simulation yields the parameters given in Table 3.3. For the full W-band, the axial ratio is less than 0.8 dB. Matching and port isolation are better than 15 dB.

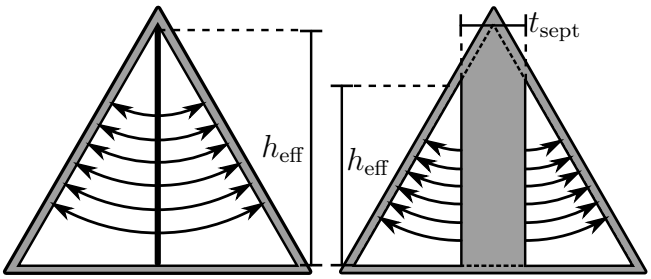



Figure 3.11: Effective height reduction due to the insertion of a thick septum in a triangular waveguide.

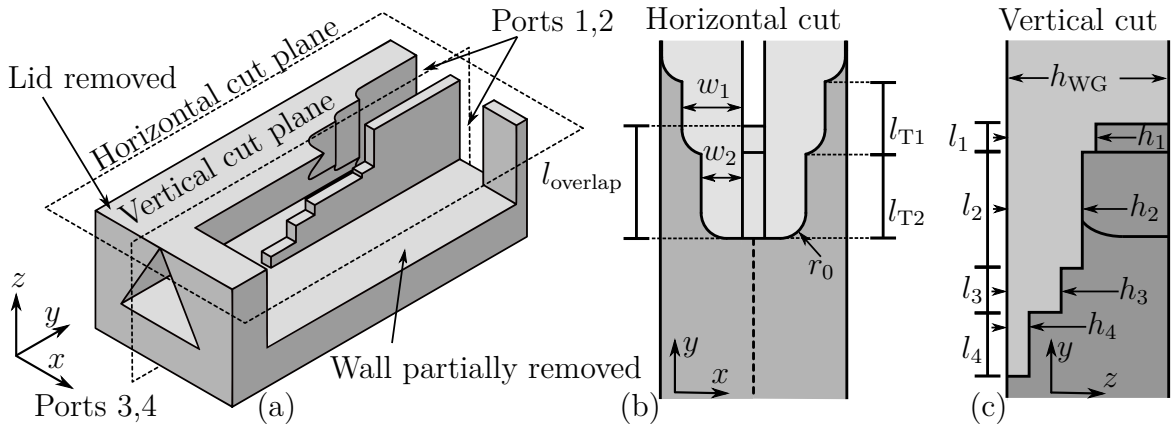



Figure 3.12: (a) 3D view of the triangular polarizer with walls partially removed. (b) Horizontal and (c) vertical cuts of the polarizer with definition of the parameters.

Table 3.3: Parameters of the designed septum polarizer. All dimensions are given in mm.

| $l_1$ | $l_2$ | $l_3$ | $l_4$ | $l_{\text{T1}}$ | $l_{\text{T2}}$ | $l_{\text{overlap}}$ |
|---|---|---|---|---|---|---|
| 0.430 | 1.835 | 0.692 | 1.004 | 1.144 | 1.312 | 1.766 |
| $h_{\text{WG}}$ | $h_1$ | $h_2$ | $h_3$ | $h_4$ | $w_1$ | $w_2$ |
| 2.54 | 1.397 | 1.183 | 0.851 | 0.348 | 0.951 | 0.649 |

### 3.2.3 Manufacturing and Measurements

Figure 3.13 shows the realized W-band polarizer, manufactured as a split block by means of conventional micro machining. It provides a triangular common port with a custom flange to which different terminations can be applied for the measurements. The output ports are bent sideways to facilitate connection to the WR10 measurement equipment. The galvanic contact of the three parts is critical in terms of losses and unwanted phase shifts in the polarizer region. To enhance the pressure at the waveguide walls and ensure reliable electrical contact while reducing losses, a recess is milled into all critical faces.

The measurements are executed with a vector network analyzer[1] (VNA) equipped with W-band measurement extensions[2]. For the full characterization of the manufactured polarizer, the method proposed in [45] is applied. The required measurements

[1]Keysight Technologies *E8361A PNA Network Analyzer, 10 MHz to 67 GHz*
[2]Keysight Technologies *N5260A Millimeter-Wave Controller - Option 120*

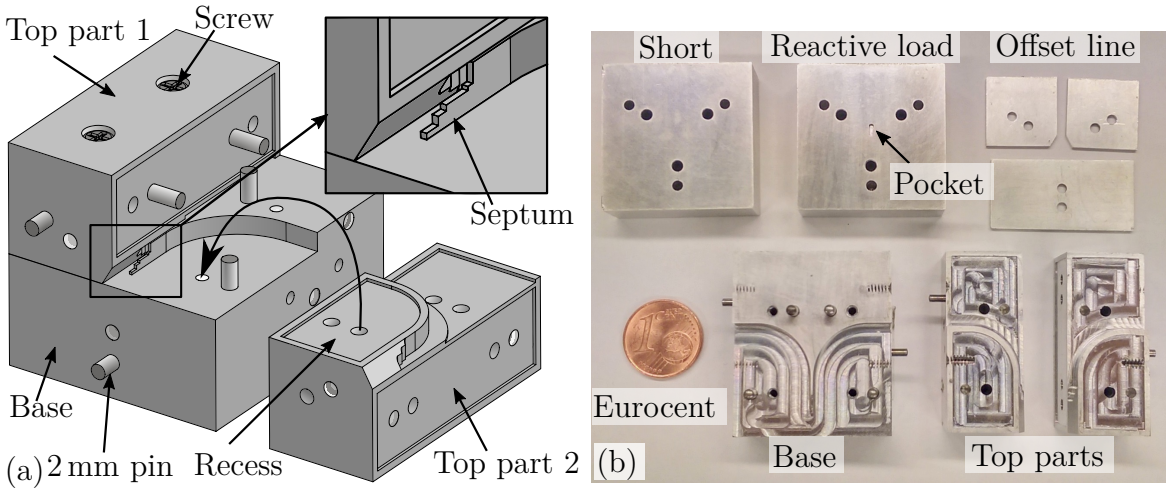



Figure 3.13: (a) 3D view on the triangular polarizer model for manufacturing. (b) Manufactured polarizer parts together with additional common port terminations required for the measurements.

are: back-to-back, offset back-to-back, short, offset short, reactive load, and offset reactive load. The actual calculation of the polarizer characteristics is done in the post-processing. The back-to-back measurements require a second polarizer. The offset is realized by three pieces of 1 mm thick aluminum that have the same split planes as the polarizer. Three 2 mm-pins at the interface provide accurate alignment. Short and reactive load are similar metal plates that mate with the triangular waveguide flange. However, the reactive load has a small pocket in the center. This pocket affects the horizontal and vertical mode differently and thus, fulfills the requirements for the measurement procedure from [45]. For the measurements, the calibration planes are set to the WR10 port planes of the split block polarizer. Thus, the waveguide bends inside the split block, which are not part of the polarizer itself, are not calibrated out of the measurements.

The measured return loss of Port 1 and Port 2 given in Fig. 3.14 is better than 15 dB over the whole W-band and compares well with the simulation. The same holds for the isolation, which is even better than 30 dB over a wide frequency range. By design, the polarizer is absolutely symmetrical with respect to Port 1 and Port 2. This symmetry is largely reproduced by the measurements.

Evaluation of the axial ratio requires the transmission coefficients of the two modes at the common port to the output ports shown in Fig. 3.15a. Ideally, both have $-3$ dB in magnitude and are 90° out of phase. The magnitude is slightly lower than

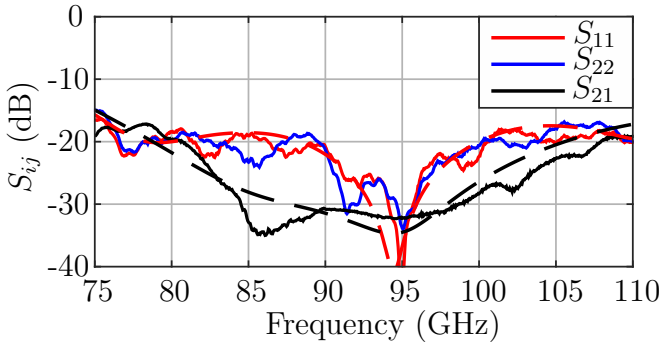



Figure 3.14: Reflection and coupling coefficients of the output ports. Simulated and measured curves are dashed and solid, respectively.

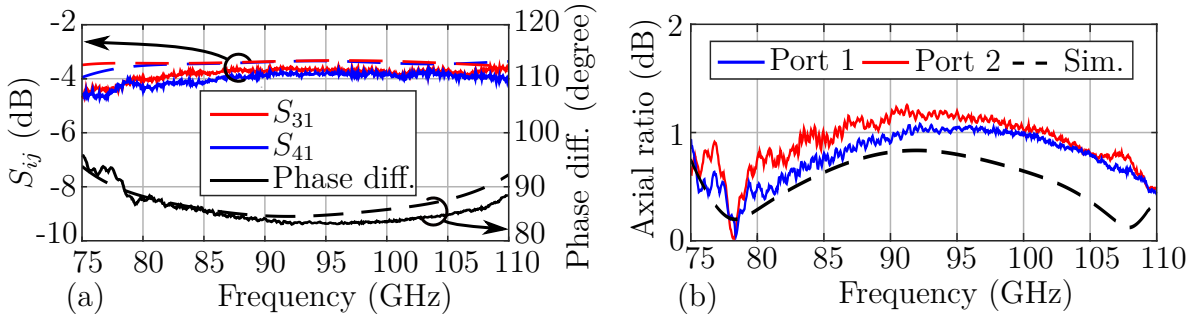



Figure 3.15: (a) Transmission coefficients from the horizontal and vertical mode at the common port to the output ports and the phase difference. (b) Axial ratio calculated for a transmission from common port to Port 1 and Port 2. Simulated and measured curves are dashed and solid, respectively.

predicted by the simulation, especially in the lower frequency range. These higher losses are caused by the slots introduced in the split block construction. However, the phase difference is close to 90° and the resulting axial ratio in Fig. 3.15b is below 1.3 dB throughout the W-band. Also, the difference between the measured axial ratio at Port 1 and Port 2 is quite small, which again proves the symmetric realization of the design. Larger deviations between simulation and measurements in the axial ratio occur only at higher frequencies. This is mainly caused by the phase difference of the transmission coefficients, since their magnitude remains almost equal up to 110 GHz.

Figure 3.16a represents the co- and cross-polar transmission. Losses of 1.7 dB are present at 75 GHz and decay to less than 1 dB at 90 GHz. This is related to the higher losses in waveguides near the cutoff frequency. The measured discrimination between left- and right-handed polarization is at least 24 dB, which is close to the expected 27 dB predicted by the simulation. For completeness, the input reflection coefficients

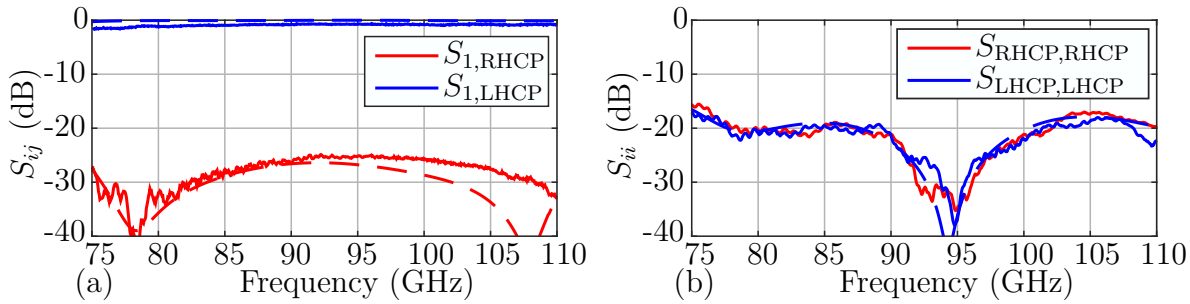



Figure 3.16: (a) Transmission coefficients between common port and Port 1 of right and left circularly polarized modes. (b) Reflection coefficients of left- and right-handed circularly polarized waves at the common port. Simulated and measured curves are dashed and solid, respectively.

at the common port for the two circularly polarized waves are given in Fig. 3.16b. Again, good agreement with the simulation is observed.

These results demonstrate that a septum polarizer covering more than 37 % bandwidth is possible using an equilateral triangular waveguide as a common port. The geometry is more complex than for conventional septum polarizers and requires advanced fabrication techniques. 3D printing offers a way to construct such complex shapes in a lightweight form that avoids lossy gaps at the corners of the waveguide. The achieved performance in terms of insertion loss and matching of the presented polarizer is similar to the state-of-the-art polarizers given in Table 3.4. However, the demonstrated bandwidth is outstanding and unique for a polarizer of this compactness.

Table 3.4: State-of-the-art septum polarizers with different waveguide shapes compared in terms of insertion loss (IL), return loss (RL), isolation (ISO), axial ratio (AR), bandwidth (BW), and center frequency $f_{\mathrm{center}}$.

| **Publication** | **WG-Shape** | **IL (dB)** | **RL (dB)** | **ISO (dB)** | **AR (dB)** | **BW (%)** | $\boldsymbol{f_{\mathrm{center}}}$ **(GHz)** |
|---|---|---|---|---|---|---|---|
| [46] | ○ | - | 20 | 28 | 0.14 | 12 | 6.1 |
| [47] | □/○ | 0.25 | 25 | - | 0.6 | 15 | 20 |
| [48] | □ | 1 | 20 | 30 | 1.4 | 10 | 225 |
| [49] | □ | - | 30 | 30 | 0.4 | 12 | 3.7 |
| [50] | □ | 0.15 | 20 | 29 | 0.7 | 16 | 13.5 |
| This work [23] | △ | 1.7 | 15 | 17 | 1.3 | 38 | 92.5 |

## 3.3 Waveguide-to-PCB Transition

Once the signal is separated into the two circular polarizations, it must be fed into the chip for amplification and downconversion. Therefore, a waveguide-to-PCB transition first transfers the signal to the PCB on which the chip is mounted.

The circuits on the CMOS chip operate differentially. Thus, a differential interface to the chip without additional components is the best option in terms of performance. Therefore, a transition from waveguide to differential line on the PCB is developed. However, the first-generation chips provided for this work contain an on-chip transformer and have single-ended inputs only. These allow characterization measurements of the chip with single-ended microprobes. To be compatible with the current CMOS chip, a single-ended transition based on the same design principles is also generated.

Most waveguide-to-PCB transitions can be categorized as either in-line or vertical transitions. Figure 3.17 outlines these two types. In-line transitions do not change the direction of signal propagation because the waveguide is mounted parallel to the PCB. Examples of such transitions covering large bandwidths are [51–53]. A major drawback of the in-line architecture is that there must be a slot in the waveguide to mount the PCB. This usually requires a split block design. Adapting in-line transitions for multilayer PCBs is possible [54], but requires a predefined stack, which limits design freedom. Vertical transitions, on the other hand, connect the waveguide vertically on the PCB, changing the direction of signal propagation by 90°. The result is a simple and robust assembly process. Broadband vertical transitions proposed in the literature always require a backside cavity [55, 56]. By omitting the cavity, only a narrow bandwidth is covered [57, 58]. This work presents a vertical broadband differential transition without backside cavity that was previously published in [59].

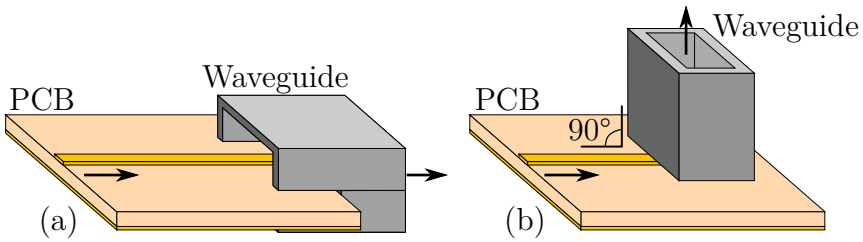



Figure 3.17: (a) In-line and (b) vertical waveguide-to-PCB transition with arrows indicating the signal propagation.

### 3.3.1 Differential Transition Design

Figure 3.18 shows the basic geometry of the transition. A signal injected at the waveguide port is confined between the two ridges and transformed to a differential signal on the two conductors on the PCB. A via fence around the transition region on the PCB prevents the excitation of substrate modes. Due to the intrinsic symmetry of the transition, an excitation at the waveguide port can only be transformed to the differential mode on the PCB or be reflected back into the waveguide. Excitation of the common mode is not possible. This enables bisection of the transition with a PEC plane at the symmetry plane. The halved transition geometry is further subdivided into several parts shown in Fig. 3.19, which are replaced by equivalent circuit elements for analysis. The waveguide and the ridge section are represented by line sections associated with a characteristic impedance ($Z_{\mathrm{R}i}$, $Z_{\mathrm{RWG}}$) and line length ($l_{\mathrm{R}i}$, $l_{\mathrm{RWG}}$). The via fence terminates the pad on the PCB where the ridge is placed. Therefore, the equivalent circuit is a short circuit stub. The length of the stub $l_{\mathrm{pad}}$ must be a quarter wavelength so that it represents an open in the propagation path from the microstrip line (MSL) to the waveguide. The impedances of the ridge sections can now be calculated for a broadband match using Chebyshev transformers [60]. For a given ridge thickness $t_{\mathrm{Ridge}}$, the physical lengths and widths of the ridges $l_i$ and $w_i$ are calculated using the power-voltage definition given in [61].

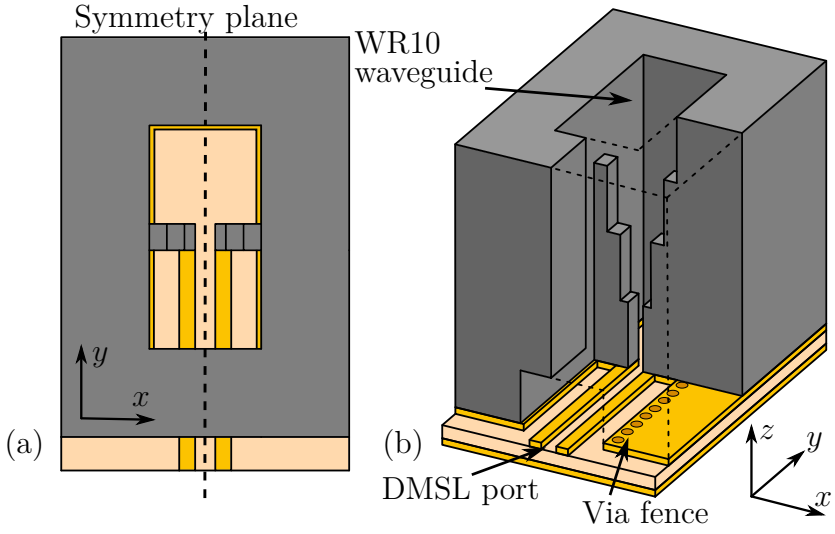



Figure 3.18: (a) Top view of the transition with its symmetry plane. (b) 3D-view with the waveguide wall partially transparent to show the ridges.

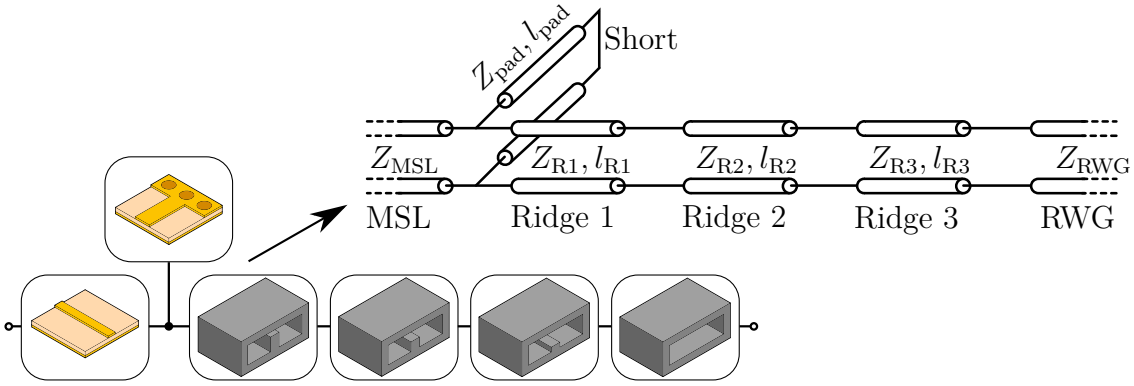



Figure 3.19: Transition separated into single homogeneous elements and the equivalent circuit.

This analytical description ignores parasitic effects at the interfaces of the elements in the equivalent circuit. Nevertheless, it provides insight into the operation of the transition and the resulting parameters are good starting values for further full-wave optimization.

Figure 3.20 introduces the parameters that define the geometry of the transition. The ridge thickness $t_{\mathrm{Ridge}}$ and the pad width $w_{\mathrm{Pad}}$ are set to 0.3 mm. Thinner ridges provide better performance, but thicker ridges make it easier to mill the waveguide in aluminum. Since the via fence abuts directly on the waveguide outline, an inset of the top copper layer of 80 µm is introduced. The vias have a diameter of 0.3 mm and a pitch of 0.4 mm. The substrate is *RO4350B*[3] with a height of 0.1 mm. With dimensions for differential microstrip line (DMSL) of $w_{\mathrm{L}} = 170\,\mu\mathrm{m}$ and $d_{\mathrm{L}} = 190\,\mu\mathrm{m}$, the line impedance is 100 Ω. A cutout in the waveguide walls of $h_{\mathrm{Cut}} = 0.5\,\mathrm{mm}$ is

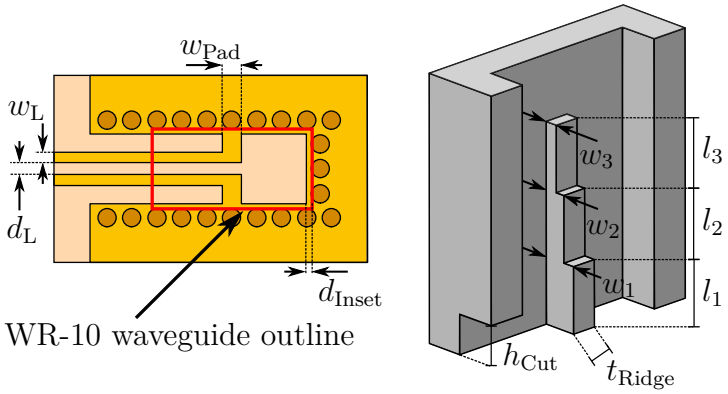



Figure 3.20: Parameters that define the geometry of the transition.

[3]Rogers Corporation *RO4350B*

Table 3.5: Ridge parameters obtained by full-wave optimization.

| | $l_1$ | $l_2$ | $l_3$ | $w_1$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|
| **Value (mm)** | 1.0 | 1.09 | 1.05 | 0.54 | 0.4 | 0.19 |

Table 3.6: Characteristic impedance and electrical line length comparison of analytical calculation and full-wave optimization for the ridge sections. $\lambda_c$ is the wavelength at the W-band center frequency of 92.5 GHz.

| Parameter | Circuit analysis | Optimization |
|---|---|---|
| $Z_{R1}$ | 63 Ω | 56 Ω |
| $Z_{R2}$ | 112 Ω | 116 Ω |
| $Z_{R3}$ | 201 Ω | 198 Ω |
| $l_{R1}$ | $0.25\lambda_c$ | $0.29\lambda_c$ |
| $l_{R2}$ | $0.25\lambda_c$ | $0.30\lambda_c$ |
| $l_{R3}$ | $0.25\lambda_c$ | $0.26\lambda_c$ |

required to feed the DMSL through. The remaining parameters, namely lengths and widths of the ridges listed in Table 3.5 are preset with the result of the equivalent circuit analysis and refined in full-wave simulation using *CST Studio Suite*[4]. The resulting insertion loss is less than 1 dB and the matching is better than 15 dB.

To emphasize the capabilities of the circuit analysis, Table 3.6 lists the characteristic impedances and electrical line lengths of the three ridge sections resulting from the calculated Chebyshev transformer and the full-wave optimization. The deviations are small and the full-wave optimization converges within fewer iterations using the precalculated values.

### 3.3.2 Sensitivity Analysis

The robustness of the designed transition is demonstrated in Fig. 3.21. Here an offset in $x$- and $y$- direction between the PCB and the waveguide is introduced. For offsets smaller than 50 µm, the matching is better than 10 dB. Displacements of 80 µm or more are to be avoided as they lead to a significant performance degradation, especially at high frequencies. A critical aspect of the whole transition is the galvanic contact between the ridges and the pads on the PCB. Figure 3.22 shows the sensitivity of the reflection coefficient to an inconsistent contact. This is modeled by a gap under the ridge with no galvanic contact. The gap size is varied in height $h_{Gap}$ and width $w_{Gap}$.

[4]Dassault Systèmes *CST Studio Suite*

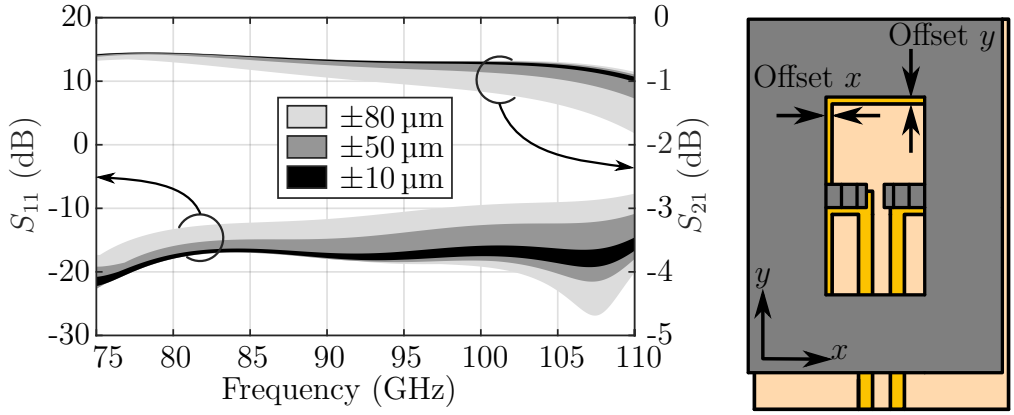



Figure 3.21: Scattering parameters of the transition for a misplacement of the waveguide on the PCB. The shaded areas mark displacements in $x$- and $y$-direction of ±10 µm, ±50 µm, and ±80 µm.

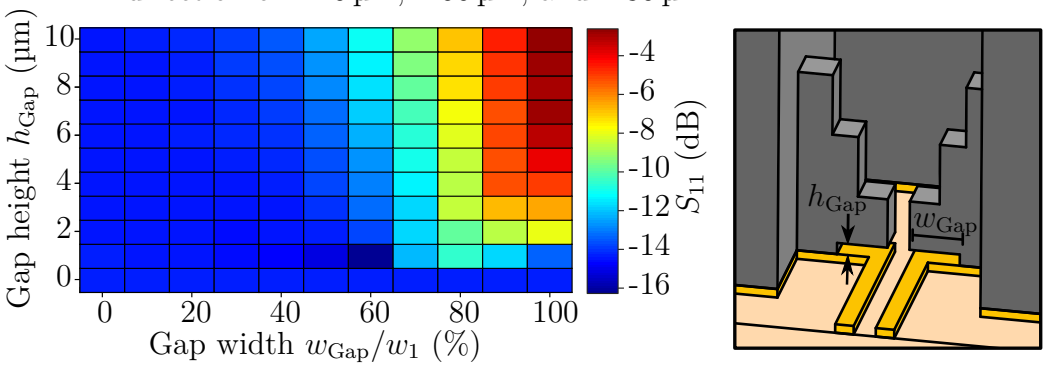



Figure 3.22: Resulting reflection coefficient for different heights and widths of the uncontacted ridge zone.

The resulting worst case reflection coefficient over the W-band is given in Fig. 3.22. As long as more than 60 % of the pad are correctly contacted, the resulting matching is better than 10 dB for gap heights up to 10 µm.

### 3.3.3 Manufacturing and Measurements

Except for the pins and screws, two symmetrical aluminum blocks are milled to form the waveguide and ridges. The PCB and waveguide blocks have alignment holes for pins to ensure accurate mating of all parts. In addition, a metal plate is machined and screwed to the back of the waveguide block with the PCB in between. Photos of the parts are provided in Fig. 3.23. The transition has three electrical ports, i.e., one waveguide port and the differential and common mode ports formed by the two microstrip conductors. They are separated, bent to opposite sides, and terminated with

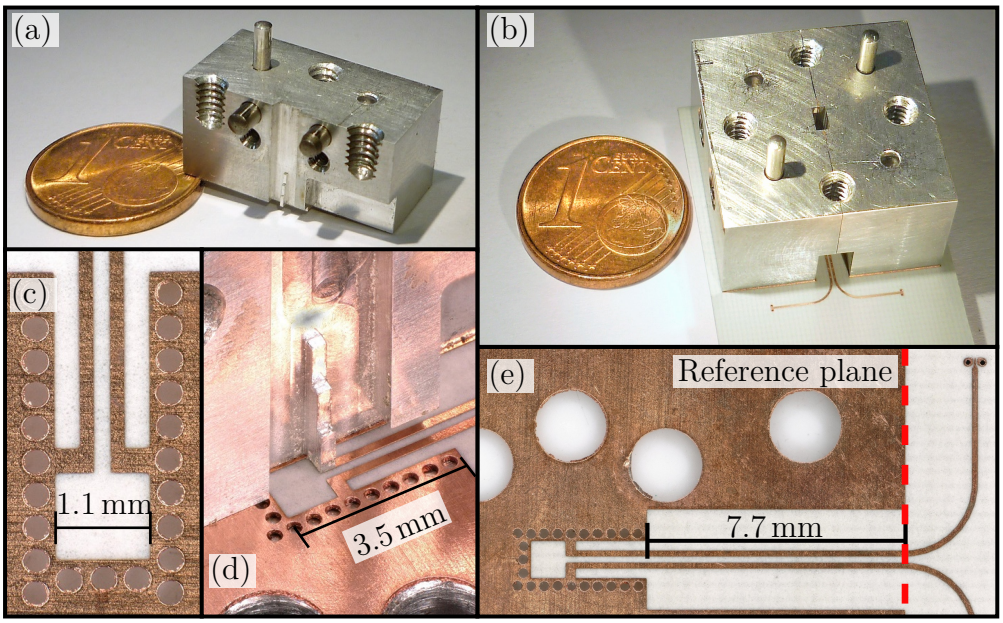



Figure 3.23: Photographs of the completed transition. (a) shows part of the split block construction. In (b) the waveguide block is mounted on the PCB and the two lines with probe landing pads are visible. (c), (d), and (e) show detailed views.

probe landing patterns. An *Agilent PNA* with W-band extensions augmented with WR10-to-1.0 mm coaxial cable transitions to accommodate the microprobes is used for the measurements. Prior to the measurements, a thru-reflect-line (TRL) calibration sets the reference plane as shown in Fig. 3.23e using a custom calibration kit. Then, to fully characterize the transition, the measurement procedure proposed in [62] is applied. The two port scattering parameters at the microstrip lines are measured with three different terminations at the waveguide port. With this data, the full 3x3 scattering matrix of the transition is evaluated in post-processing. Here, the scattering parameters are given for the three electrical ports of the transition, i.e., common mode (denoted by c), differential mode (denoted by d), and waveguide (denoted by 1).

The modal reflection coefficients plotted in Fig. 3.24a show good agreement between measurements and simulation. The matching is better than 13 dB for the differential MSL port as well as for the waveguide port. The reflection coefficient for the common mode is very high. This is due to the fact that, for symmetry reasons, a common mode cannot excite a propagable mode in the waveguide. Transmission to differential mode is also not possible for the same reason, so it is fully reflected. However, the common mode is not relevant in the target application.

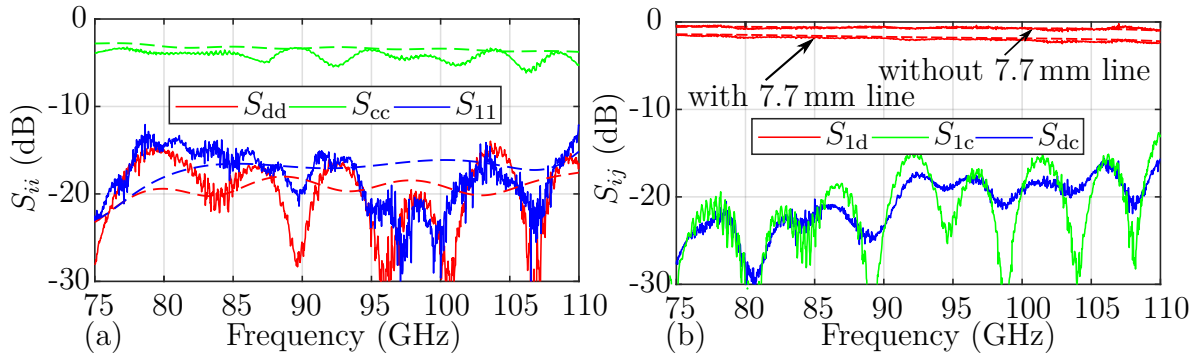



Figure 3.24: (a) Modal reflection coefficients and (b) modal transmission coefficients of the manufactured transition. Simulated and measured curves are dashed and solid, respectively.

In the simulation, the transmission parameters to the common mode $S_{1c}$ and $S_{dc}$ are zero due to perfect symmetry. Figure 3.24b reveals that the manufactured transition contains asymmetries. However, the unwanted transmission coefficients exhibit a low value of less than −15 dB. The transmission from the waveguide to the common mode on the microstrip line is measured to the reference plane shown in Fig. 3.23e which includes a 7.7 mm long differential line section prior to the transition itself. A dedicated line segment is measured separately to calculate the losses added by this line segment. With the extra losses of the 7.7 mm long line removed from the measured insertion loss, it ranges between 0.5 dB to 1.1 dB in the frequency range from 75 GHz to 110 GHz.

In Table 3.7 the developed transition is compared to differential transitions in similar frequency bands found in the literature. This work performs as well as other vertical or in-line transitions while offering a wide bandwidth and omitting a backside cavity.

Table 3.7: State-of-the-art differential transitions from the literature compared in terms of IL, RL, BW and center frequency $f_c$.

| **Publication** | **Type** | **Backside cavity** | **IL (dB)** | **RL (dB)** | **BW (%)** | **$f_c$ (GHz)** |
|---|---|---|---|---|---|---|
| [51] | in-line | - | ≤0.9 | ≤12 | 37.8 | 92.5 |
| [52] | in-line | - | ≤1.0 | ≤15 | 52.5 | 70.5 |
| [63] | in-line | - | ≤1.9 | ≤10 | 20.2 | 78.0 |
| [56] | vertical | yes | ≤2.3 | ≤15 | 33.0 | 60.0 |
| [57] | vertical | no | ≤0.5 | ≤15 | 11.0 | 96.0 |
| [58] | vertical | no | ≤2.0 | ≤10 | 11.0 | 80.4 |
| [64] | vertical | no | ≤0.8 | ≤15 | 13.0 | 60.0 |
| This work [59] | vertical | no | ≤1.1 | ≤13 | 37.8 | 92.5 |

### 3.3.4 Single-Ended Adaptation and Realization

The adaptation to a single-ended transition exploits the symmetry of the presented differential transition, as it allows the transition to be bisected by a PEC plane. Taking one half of the resulting halves leads directly to a single-ended transition. However, the size of the short waveguide wall is also halved. To get a waveguide interface with a height-to-width ratio of two, the ridge parameters must be adjusted. Vias are inserted into the ridge pad to implement the quarter wavelength transformer. For single-ended lines, simple and compact transitions to substrate integrated waveguide (SIW) are available [65]. Two such transitions are used in the single-ended transition to avoid the need for a feedthrough cutout in the waveguide. This simplifies manufacturing and allows for hermetically sealed designs.

Figure 3.25 shows the result of the design adaptation with a single-ended grounded coplanar waveguide (GCPWG) port. The GCPWG center conductor has a width of 0.18 mm and a distance to the ground plane on each side of 0.1 mm to provide 50 Ω line impedance on a 0.1 mm thick *RO4350B* substrate. The GCPWG is first transformed into an MSL and then into an SIW. The length of the SIW can be varied without severe performance degradation. In general, however, it should be kept short to reduce

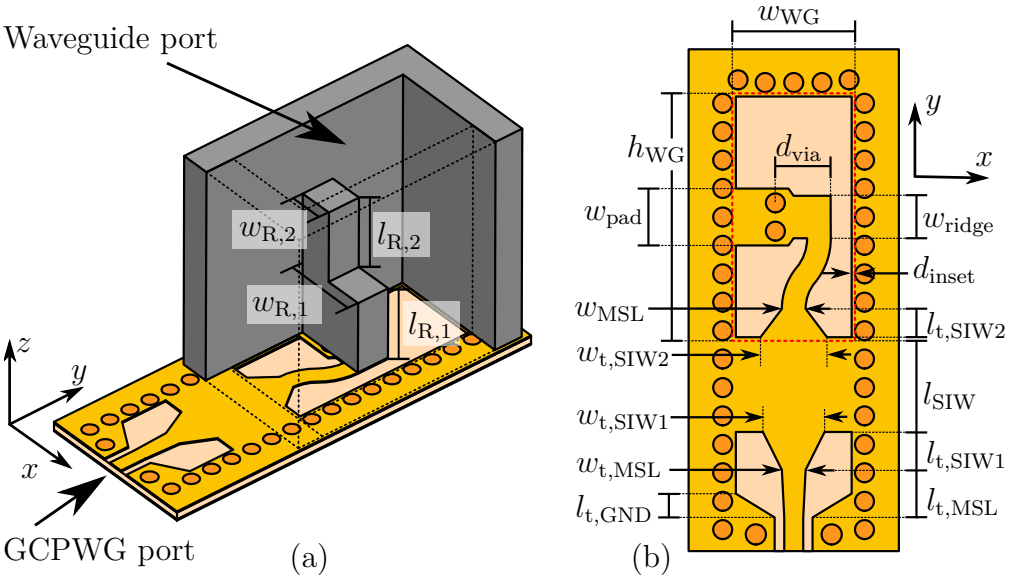



Figure 3.25: (a) 3D view of the single-ended transition with the waveguide wall partially removed. The rounding of the waveguide edges with a radius of 0.1 mm is not shown. (b) Top view of the base PCB with parameters.

Table 3.8: Parameters of the designed single-ended waveguide-to-PCB transition. All dimensions are given in mm.

| $l_{\mathrm{t,GND}}$ | $l_{\mathrm{t,MSL}}$ | $w_{\mathrm{t,MSL}}$ | $l_{\mathrm{t,SIW1}}$ | $w_{\mathrm{t,SIW1}}$ | $l_{\mathrm{t,SIW2}}$ | $w_{\mathrm{t,SIW2}}$ | $w_{\mathrm{WG}}$ | $h_{\mathrm{WG}}$ |
|---|---|---|---|---|---|---|---|---|
| 0.274 | 0.554 | 0.210 | 0.426 | 0.494 | 0.313 | 0.720 | 1.241 | 2.540 |
| $w_{\mathrm{MSL}}$ | $w_{\mathrm{pad}}$ | $w_{\mathrm{ridge}}$ | $d_{\mathrm{via}}$ | $d_{\mathrm{inset}}$ | $w_{\mathrm{R,1}}$ | $l_{\mathrm{R,1}}$ | $w_{\mathrm{R,2}}$ | $l_{\mathrm{R,2}}$ |
| 0.246 | 0.620 | 0.450 | 0.505 | 0.050 | 0.909 | 0.637 | 0.298 | 1.005 |

losses. Here, the SIW has a length of $l_{\mathrm{SIW}} = 1\,\mathrm{mm}$. All vias have a diameter of 0.2 mm and a pitch of 0.3 mm. The dimensions of the tapers before and after the SIW section are determined by constrained optimization in full-wave simulation. The same is done to obtain parameters for the ridge dimensions and the distance $d_{\mathrm{Via}}$ defining the quarter wave transformer, which is one of the most critical parameters for the transition performance.

Table 3.8 displays the resulting transition parameters. To realize the transition using additive manufacturing, the width of the ridge $w_{\mathrm{ridge}} = 0.45\,\mathrm{mm}$ is larger compared to the differential transition. In addition, the design avoids sharp edges and rounds all inner and outer waveguide edges and ridges to a radius of 0.1 mm.

Figure 3.26 depicts the simulated scattering parameters of the optimized single-ended transition. The transition is well matched throughout the W band, despite having only two ridge sections. This is due to the fact that by including the SIW transitions, there are more parameters in total to tune the performance in the optimization process. The simulated insertion loss is between 0.9 dB and 1.1 dB. This is higher than for the simulated differential transition with 0.55 dB to 1 dB. The reason is that the feed structure is much longer due to the SIW section and tapers.

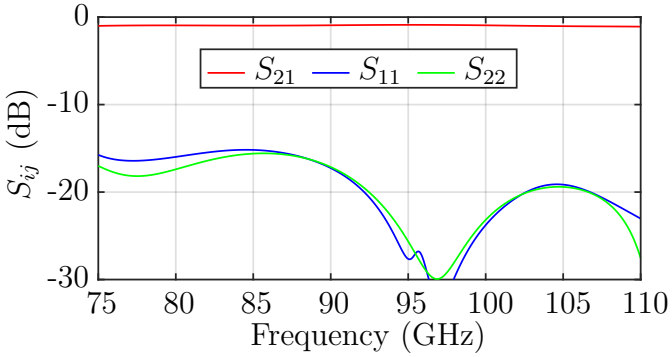



Figure 3.26: Simulated scattering parameters of the single-ended transition. Port 1 refers to the GCPWG port and Port 2 corresponds to the waveguide port.

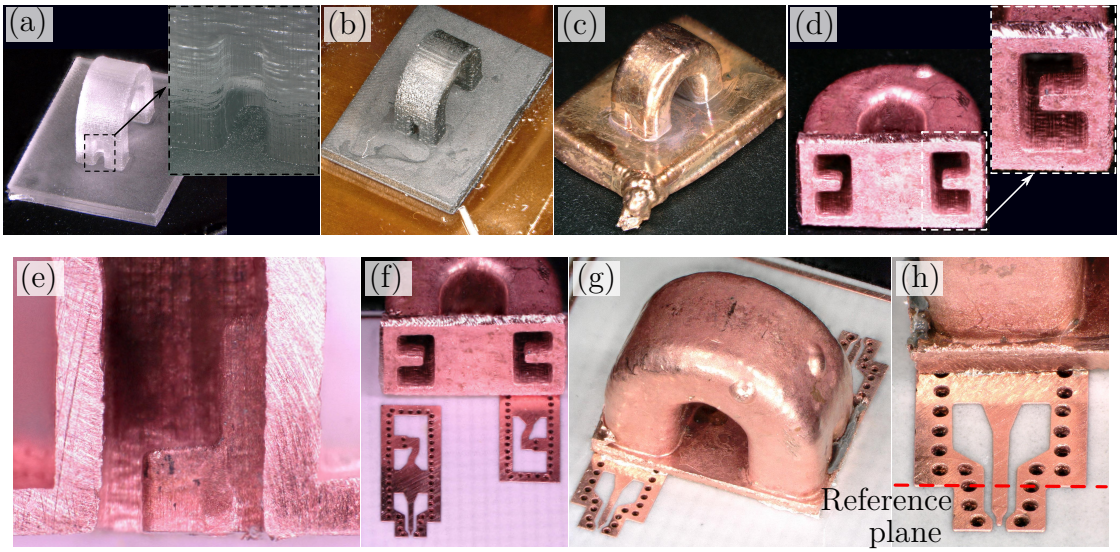



Figure 3.27: Manufacturing process of the back-to-back transition. (a) 3D printed waveguide negative with detailed view of the transition ridges. (b) Graphite coated plastic part attached to a wire for galvanic copper plating. (c) 0.4 mm thick plated part. (d) Copper waveguide component after burn-out and trimming. (e) Close-up of the realized ridge of a specimen with one wall removed. (f) PCB and copper part before assembly. (g) Transition mounted with conductive adhesive. (h) Detailed view indicating the reference plane of the measurements.

A back-to-back configuration demonstrates the performance of the single-ended transition. A semicircular waveguide section connects two transitions with a pitch of 4 mm. This results in a single metal part that contains two transitions. It is placed on a PCB and can be measured with microprobes.

To fabricate the waveguide with the transitions, first a negative mold in plastic is printed on a stereolithography 3D printer[5]. As shown in Fig. 3.27a, the mold features a rectangular base in addition to the waveguide and transition structure. The next step in Fig. 3.27b is to apply a thin layer of graphite to make the plastic surface conductive for the copper plating in the next step. Therefore, the part is attached to a wire and dipped into an electroplating bath to deposit a 0.4 mm thick copper layer as shown in Fig. 3.27c. For the plating process the plastic part is glued with its backside onto a holder. Therefore, no copper forms on the backside. This backside opening is important for the next step, to release the gases generated while the part is baked at 510 °C for 30 min to burn out the plastic mold.

[5]Formlabs *Form 1+*

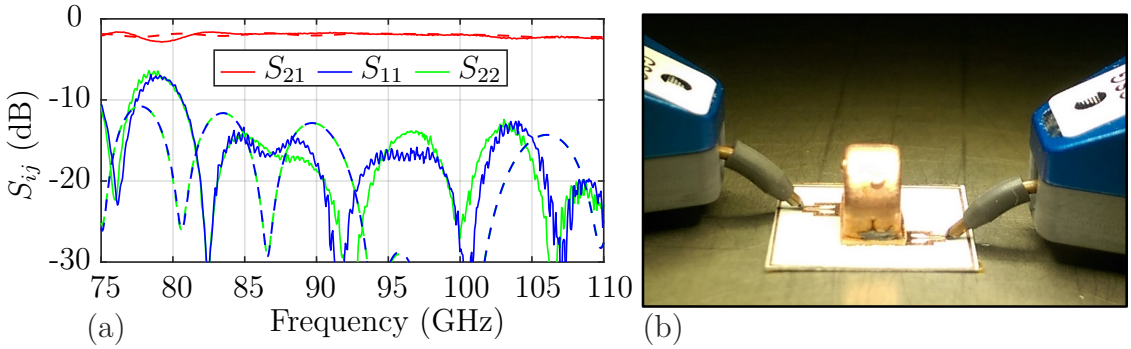



Figure 3.28: (a) Simulated (dashed line) and measured (solid line) scattering parameters of the back-to-back waveguide transition. (b) Photo of the measurement setup with microprobes.

The resulting hollow copper body is rinsed in weak acid to remove oxidized copper residues and ash. After trimming the base to appropriate dimensions, the one-piece solid copper back-to-back transition shown in Fig. 3.27d is bonded to the PCB using conductive adhesive[6]. This is documented in Fig. 3.27f-h. Note that the transition can also be soldered to the PCB since it is made of pure copper. For the photo in Fig. 3.27e, a realized component wall was removed to inspect the quality of the ridges inside the waveguide. Dimensional deviations of less than 60 µm from the design values are measured optically.

Figure 3.28 shows the measurement setup and the scattering parameters of the back-to-back transition. Around 79 GHz the return loss is only 7 dB. For the rest of the W-band, the matching is better than 11 dB for the back-to-back configuration, which corresponds to approximately 14 dB matching of a single transition. The insertion loss is very close to the simulation, except for the deviation at 79 GHz, where only 2.8 dB is measured. However, the simulation predicts a maximum insertion loss of 2.2 dB at 110 GHz where the measurements return 2.4 dB. Thus, for a single transition, the insertion loss even at 79 GHz is better than 1.4 dB and better than 1.2 dB for frequencies above 80.5 GHz. This result demonstrates that the presented manufacturing approach using 3D printing to realize complex waveguide structures with small details is well suited at least up to frequencies as high as 110 GHz.

Table 3.9 gives a comparison with other vertical transitions found in the literature. Most of the cited publications also use a back-to-back configuration for characterization. Similar to those publications, the return loss of the individual transitions in this work is

[6]EPOXY TECHNOLOGY Inc., *EPO-TEC H37MP-2*

Table 3.9: Comparison of state-of-the-art single-ended vertical transitions from the literature.

| Publication | Type | Back cavity | IL (dB) | RL (dB) | BW (%) | $f_c$ (GHz) |
|---|---|---|---|---|---|---|
| [66] | MSL to RWG | no | ≤3.0 | ≤7.8 | 10.0 | 25.4 |
| [67] | SIW to RWG | no | ≤0.4 | ≤15 | 8.0 | 29 |
| [68] | MSL to RWG | yes | ≤1.1 | ≤10 | 16.0 | 60 |
| [69] | MSL to RWG | no | ≤0.7 | ≤15 | 14 | 92 |
| [70] | SIW to RWG | no | ≤0.7 | ≤12 | 26.5 | 94.5 |
| This work | GCPWG to RWG | no | ≤1.4 | ≤10 | 37.8 | 92.5 |

estimated by the back-to-back return loss plus 3 dB. In terms of performance, the trade-off between bandwidth and return loss is clear. The higher the relative bandwidth, the lower the return loss. In terms of insertion loss, the transition of this work is worse than most others. There are two reasons for this. First, a much wider bandwidth is covered, and second, the losses of the interconnecting rectangular waveguide section used in the back-to-back configuration are not calibrated out. Thus, the 1.4 dB insertion loss includes not only the transition itself, as in the other publications, but also the short waveguide section connecting the two transitions.

## 3.4 PCB-to-Chip Transition

Finally, the signal picked up by the antenna must be transferred to the receiver chip for further processing, i.e., down-conversion and amplification. This requires a transition from the PCB to the chip pads. At low frequencies, a simple conductive contact is sufficient, but at high frequencies, multiple effects such as bond-wire inductance degrade the connection.

### 3.4.1 Common Interconnect Methods

Wire bonding and flip-chip, shown in Fig. 3.29, are the two common methods to realize such an interconnection. In the former, thin wires connect the pads of the chip to the PCB. They represent a parasitic inductance that degrades transmission, especially at high frequencies, and can only be matched in narrow bandwidths [71]. An advantage is that the chip is robustly mounted on the PCB or a heat sink, which simplifies thermal

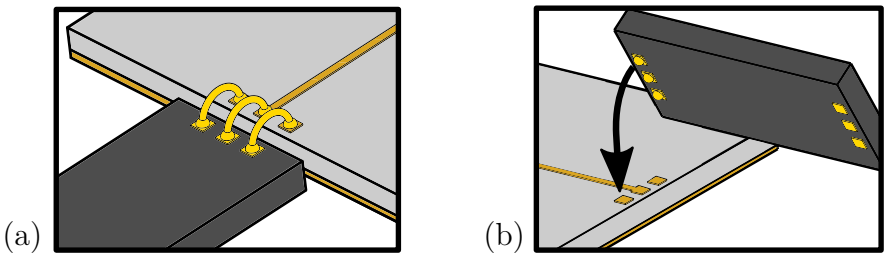



Figure 3.29: (a) Wire bonds. (b) Flip-chip with gold stud bumps.

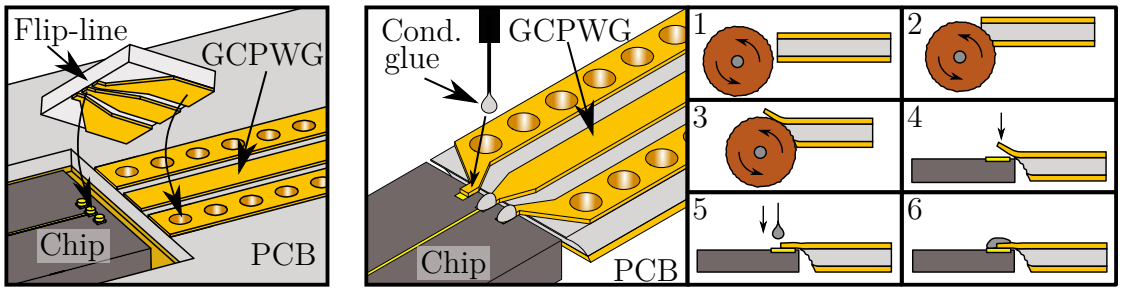
management. In addition, all of the connections can be inspected and are accessible for repair or modification. The latter is very useful for the manufacturing of prototypes.

For flip-chip interconnects, gold balls are first placed on all of the pads of the chip, which is then flipped over and connected to the printed circuit board by pressing it down onto the corresponding pads. Thermal and ultrasonic energy may be applied to achieve a good bond. The small distance between the chip and the PCB eliminates most parasitic inductance and makes the interconnect usable for broadband applications beyond 100 GHz [71]. However, since the only connection points between chip and PCB are gold bumps, the entire transition is mechanically sensitive. This can be improved with underfill adhesive, which in turn can detune the on-chip circuitry. Attaching a heat sink to a flip-chip mounted chip inevitably leads to structural stress that can destroy the sensitive interconnects. Also, attaching the gold balls to the chip pads is challenging, especially if the chip pad surface is a metal other than gold. The chips used in this work have aluminum pads, which result in very fragile bonds. Therefore, flip-chip interconnects are not investigated further here.

### 3.4.2 Advanced Interconnect Methods

This work evaluates two advanced methods for interconnecting chips. The first is proposed in [72], where an impedance controlled line section connects the upside facing chip to the PCB. Fig. 3.30a shows how a coplanar line is glued to the top of the chip and the PCB with non-conductive adhesive to make the connection. This interconnect basically has two flip-chip connections with a 50 Ω line section in between. This allows for longer interconnects without significant degradation in return loss. Regarding insertion loss, the transition should be as short as possible due to losses.

For the other advanced interconnect, called the glue-on transition, the line on the PCB is glued directly to the chip pads with the same conductive glue that was used




(a) (b)

Figure 3.30: (a) Flip-line transition without the non-conductive glue. (b) Glue-on transition with conductive glue applied to two of the three connection points and cross-sectional view of the glue-on transition manufacturing.

to mount the single-ended transition in Section 3.3.4. Figure 3.30b shows the manufacturing process. First, a rotary tool chamfers the bottom edge of the PCB. The substrate is hard and brittle. Due to the direction of rotation, the rotary tool presses the bottom copper layer against the substrate material. Both are abraded and the chamfer is formed. The top copper layer, including the pads to be bonded to the chip, flexes upward and is preserved. Once prepared, the board is placed next to the chip so that the pads overlap. The upward bent copper conductors are pressed down to align with the pads. Finally, conductive adhesive, applied to the pads, completes the electrical connection.

### 3.4.3 Manufacturing and Measurements

Four different PCB-to-chip transitions are evaluated in this work, i.e., the two advanced methods and two of the common methods, namely wire bonding and ribbon bonding. The former uses a gold wire of 25 µm diameter and is included for comparison only. Ribbon bonding uses a wire with a rectangular cross section instead of a circular one. Here a wire with a cross section of 50 µm by 17.5 µm is used. The larger width of the wire reduces parasitic inductance and improves high frequency performance compared to wire bonding.

Figure 3.31 displays photos of the four different interconnects and their fabrication process. All of them realize a transition from a 50 Ω GCPWG line on a 0.1 mm thick *RO4350B* substrate to a 50 Ω line on a 100 µm thick CMOS chip. The pads on the chip have a pitch of 100 µm and a size of 40 µm by 80 µm. Measurements are made using a VNA, waveguide extenders, microprobes, and a manual probe station. Port 1

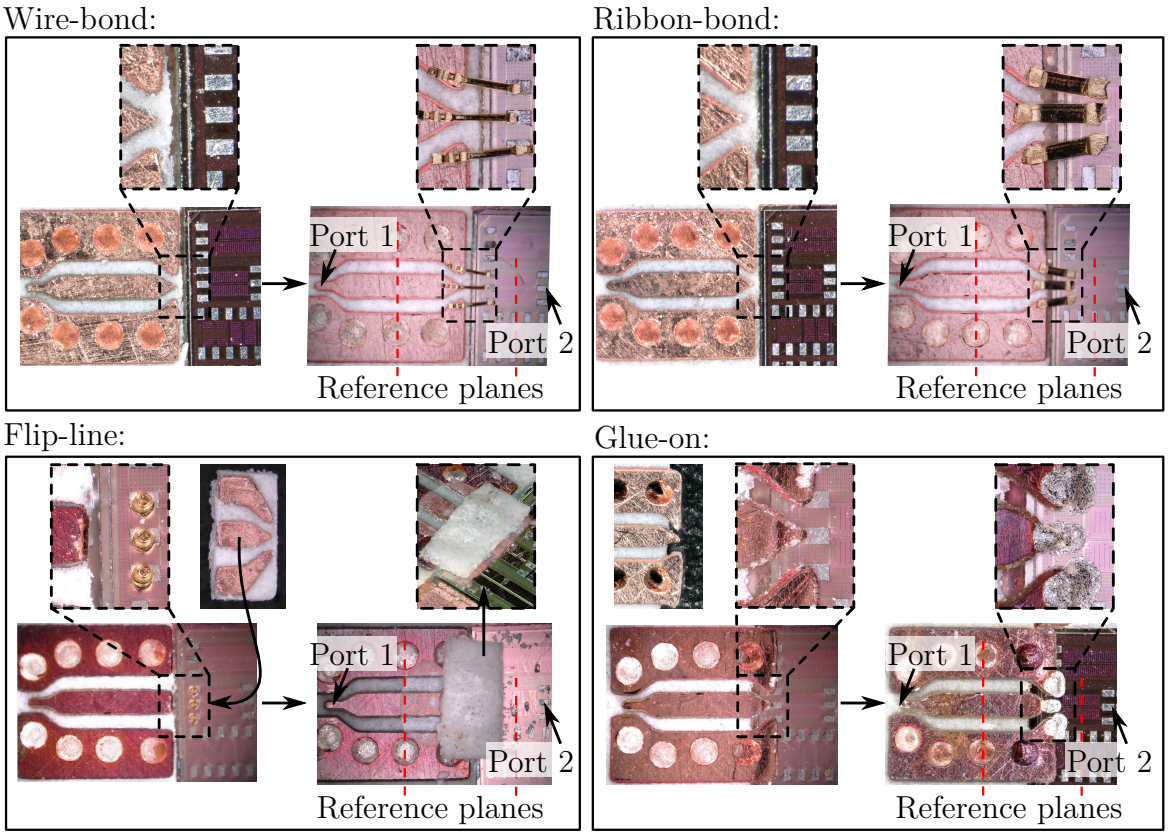



Figure 3.31: Photos showing the manufacturing and the realized interconnect for the four different PCB-to-chip transitions. The different colors of the copper traces result from different light settings on the microscope, as well as the different curing times and temperatures of the adhesives used, which create unique amounts of oxidation.

corresponds to the PCB side and Port 2 to the chip side. Figure 3.32 visualizes the measurement procedure. First, the VNA is calibrated to the probe tips with a commercial calibration substrate. Next, the four chip transitions are measured, resulting in four sets for $S_{\mathrm{Meas}}$. These measurements include the probe landing pads and the line sections on both sides of the actual interconnect. To obtain the scattering parameters with respect to the reference planes shown in Fig. 3.31, dedicated standards on the chip and a custom GCPWG calibration kit are measured. The standards are a thru, a reflect, and a line. Using the theory given in [73], the scattering matrices are calculated for the path from the probe tip to the reference planes $S_{\mathrm{A}}$ and $S_{\mathrm{B}}$. Using the transmission parameter definition, the single interconnect scattering matrix $S_{\mathrm{Bond}}$ is obtained by deembedding.

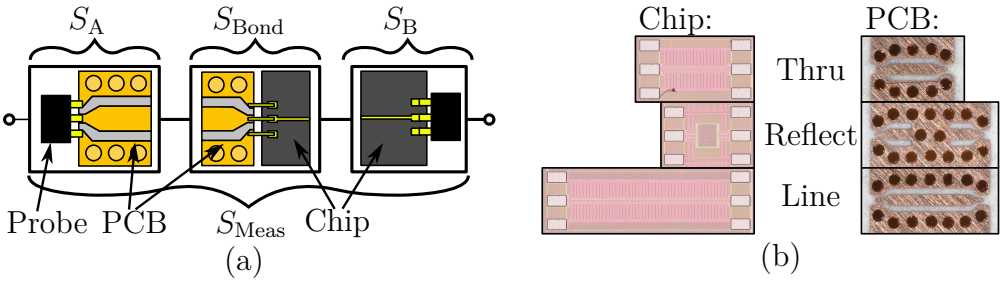



Figure 3.32: (a) Block diagram of the measurements from one probe to the other with the actual interconnect in series with the auxiliary circuit parts. (b) The calibration standards used to deembed the PCB-to-chip transitions.

The deembedded measurement results compared to the simulated values are given in Fig. 3.33. As expected, the wire-bond interconnect has the worst matching. At 110 GHz only 8 dB is achieved. The insertion loss is slightly higher than expected. This result shows that if the bond wires are kept as short as possible, wire-bond interconnects can have a decent performance even up to 110 GHz.

The ribbon-bond measurements align quite well with the simulation. A matching of 10.5 dB is predicted and 9.5 dB are measured at 110 GHz. Up to 106 GHz, the matching is better than 10 dB, making this interconnect well suited for W-band applications.

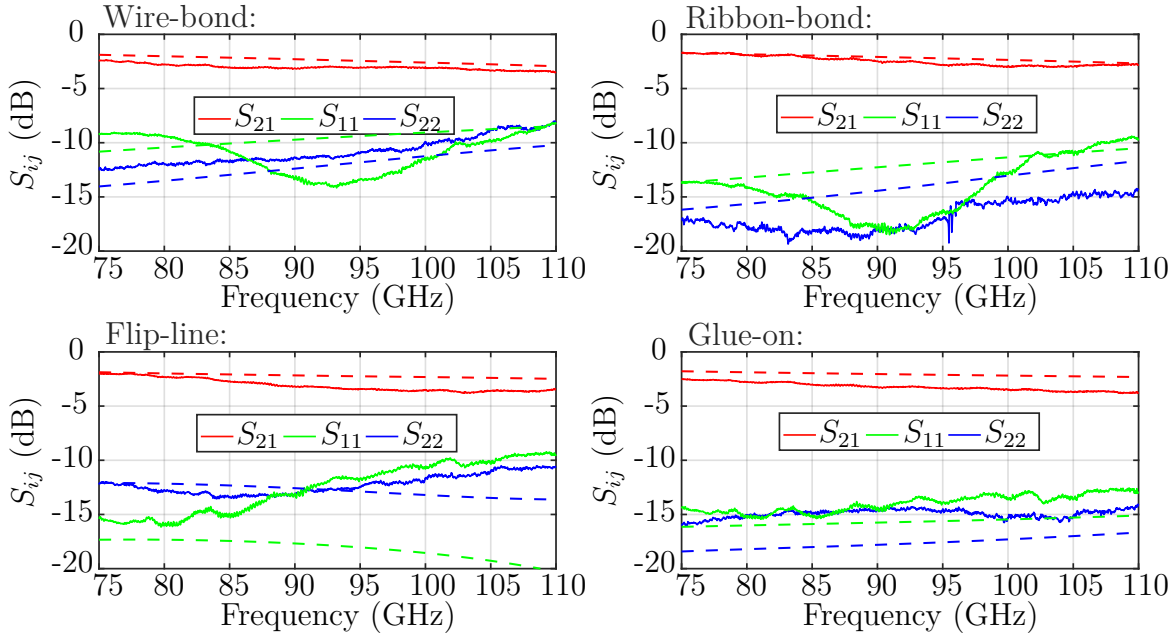



Figure 3.33: Deembedded measurement results of the four different chip transitions. Simulated and measured curves are dashed and solid, respectively.

For the flip-line interconnect, a significant deviation between measurements and simulation can be observed in terms of matching and insertion loss at the high end of the frequency range. Only up to 105 GHz is the matching better than 10 dB. This is probably due to manufacturing tolerances. As can be seen in Fig. 3.31 at the flip-line interconnect, the three gold balls on the chip are not centered on each pad, but are shifted downward by several microns. Another error that can occur is a misplacement of the flip-line segment, which cannot be inspected after fabrication.

The glue-on transition achieves the best performance in terms of matching with more than 12.5 dB throughout the W-band. The transmission deviates slightly from the simulation. The reason is that the conductivity of the conductive glue used cannot be predicted accurately. Since it consists of conductive particles to make the electrical contact, it is not guaranteed that the extremely small amount used for the bond has the same bulk conductivity as larger samples.

Comparing the four presented PCB-to-chip interconnects, the glue-on transition is used for the system realization in this work. It is simple and reliable to manufacture. Even after fabrication, the interconnects can be subject to inspection and are likely to be repairable. The flip-line transition also offers good performance, but is more susceptible to manufacturing defects. When longer interconnect distances between PCB and chip need to be bridged, it is a good alternative due to the near 50 Ω impedance of the flip-line segment. Ribbon bonding over short distances gives acceptable performance for W-band. As expected, the wire-bond interconnect has the worst performance. However, it still achieves a decent matching if the bond wires are kept as short as possible, here shorter than 200 µm.

### 3.4.4 Low-Frequency Interconnect

At the output ports of the active CMOS receiver chip used in this work, a frequency range from 1 GHz to 36 GHz has to be covered. For these rather low frequency interconnects, as well as the LO input at 18.5 GHz, wire bonding is well suited. Figure 3.34 shows such an interconnect and the measurement results. For frequencies up to 40 GHz the matching is better than 14 dB and the insertion loss is below 1.4 dB.

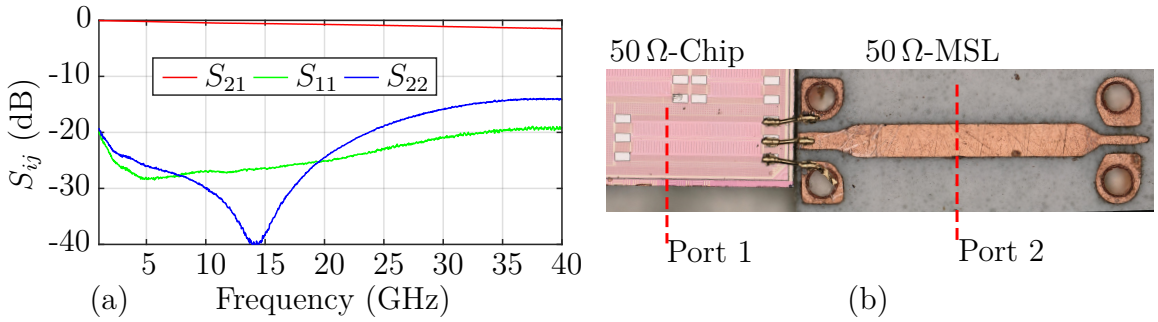



Figure 3.34: (a) Deembedded measurement result of the low-frequency wire-bond transition from a 50 Ω on-chip line to a 50 Ω microstrip line on a PCB. (b) Reference planes of the measurement.

## 3.5 CMOS Receiver Chip

The active component in this work, i.e., the CMOS receiver chip, is developed at the *Technische Universität Berlin* by the *Fachgebiet Mirkowellentechnik*. The design is manufactured by *Global Foundries* in the 22 nm FDSOI (fully-depleted silicon-on-insulator) process. Compared to standard bulk CMOS, FDSOI achieves higher maximum switching frequencies due to reduced parasitic capacitances from drain and source to the substrate [74].

### 3.5.1 Chip Overview

The CMOS chip includes several functional blocks, shown in Fig. 3.35. An LNA first amplifies the received signal which is then down-converted by a mixer and amplified again by a broadband baseband amplifier (BBA). Two such down-conversion channels (CH1, CH2) are integrated on one chip to support the two circular polarization signals with a single chip. The LO input of 18.5 GHz is quadrupled on-chip to 74 GHz, resulting in an IF range from 1 GHz to 36 GHz for signals between 75 GHz and 110 GHz at the radio frequency (RF) input. In addition, phase shifters adjust the LO phase to allow beam steering in an array configuration. The phase shifters on the first generation of chips connect the two phase shifters in series to achieve a larger shifting range in CH1. According to the simulation, the phase shifters on the preliminary chips only give a maximum phase shift of about 38° for the 74 GHz LO signal in CH1 and only 19° in CH2 [74]. This is not enough to demonstrate effective beam steering. Therefore, the LO requires external phase shifters for the array demonstration.

Figure 3.36 provides detailed pictures of the chip. The LNA itself is fully differential

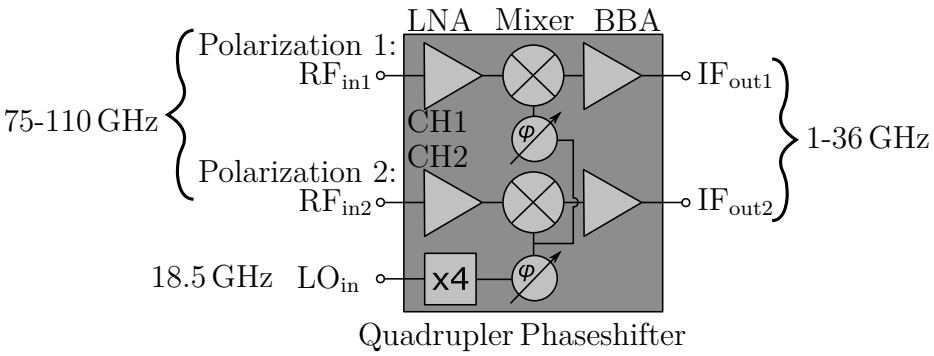



Figure 3.35: Block diagram of the receiver chip.

and uses a parasitic capacitance neutralization technique for improved bandwidth. For measurement purposes, however, the RF input is single-ended and transformed to differential by an on-chip balun. In simulation, the LNA has a gain of more than 17 dB in the W-band. The DC input voltage is 0.8 V and all components on the chip share the same common DC voltage. The additional DC inputs on each component are redundant. The mixer is of resistive type with a simulated conversion gain of −8.5 dB. A two stage push-push doubler provides the LO signal with the required amplitude for the mixer. It requires an LO input signal at 18.5 GHz with at least 0 dBm to provide sufficient output power for the mixer. As with the RF input, a balun is also used on the quadrupler input to drive the differential input of the first doubler stage with a single-ended signal. Therefore, the single-ended input signal must have a slightly

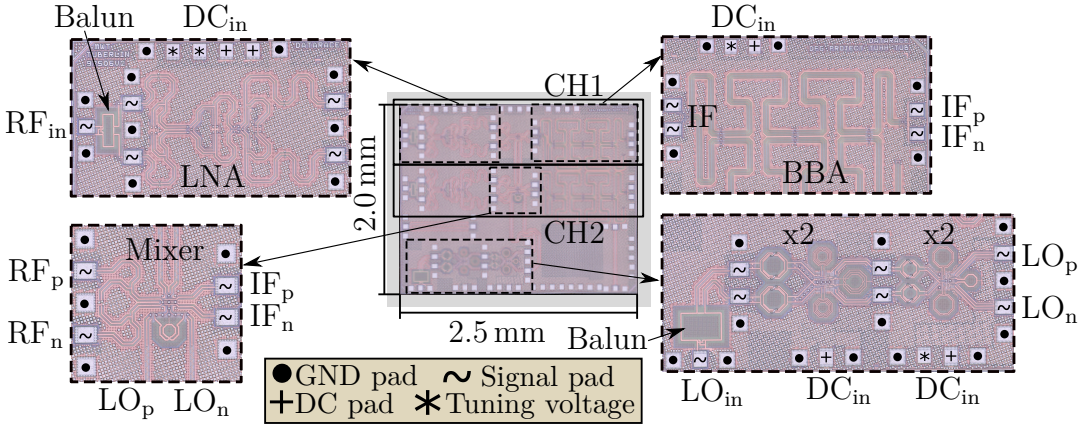



Figure 3.36: Photograph of the receiver chip with detail views on the various components. The pads in the detail views are marked with symbols associated to their function according to the documentation provided by the chip designers from *Technische Universität Berlin*.

higher level to compensate for the balun losses and to achieve a sufficient drive level for the quadrupler. After down-conversion, the BBA amplifies the IF signal. In the simulation, it has a gain of at least 11.9 dB in the frequency range from 1 GHz to 36 GHz. So the total simulated conversion gain of the receiver chip is at more than 20 dB.

### 3.5.2 Chip Characterization

To test the performance of the chip, it is mounted on a PCB with bond wires for the DC connections and for the LO and IF ports. These are connected to 2.92 mm Rosenberger Precision Connectors[7] (RPC). The glue-on interconnect is not used because only low frequency and DC signals are involved. A microprobe feeds the RF inputs of the chip during the measurements as shown in Fig. 3.37. The conversion gain with the reference planes in the probe tip on the RF side and in the RPC on the IF side is measured by inserting a signal of known power into the RF input in the frequency range from 75 GHz to 110 GHz. The signal power is less than −20 dBm to avoid saturation effects in any of the components on the chip. According to the simulation of the quadrupler in [74], the output power of the quadrupler remains fairly constant for an input power from 0 dBm to 10 dBm. Thus, this and all further measurements use an LO power of 5 dBm at 18.5 GHz. At the IF output ports, the power is measured at one polarity only, with the other polarity terminated by a 50 Ω load. The conversion gain is calculated as

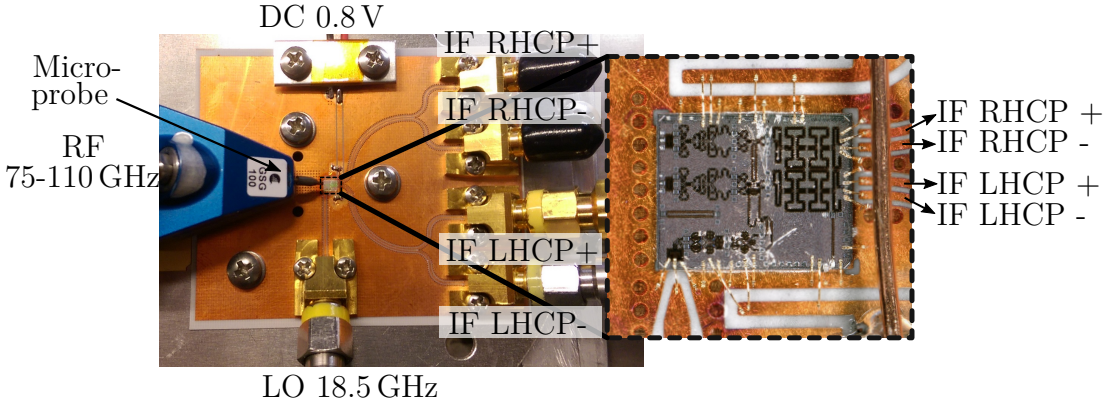



Figure 3.37: Photo of the mounted receiver chip. The connection to the PCB is made by wire bonds, as can be seen in the detail view of the chip. The microprobe can measure only one channel (RHCP or LHCP) at a time.

[7] Rosenberger Hochfrequenztechnik GmbH & Co. KG *RPC-2.92 SMD Connector 02K80F-40ML5*

the ratio of the measured IF output power and the RF input power and thus includes the losses of the integration network. However, the wire bond, the microstrip line and the RPC introduce total losses of 0.5 dB to 2.5 dB for the frequency range from 1 GHz to 36 GHz according to simulation.

Figure 3.38 plots the conversion gain measured at the IF LHCP- output for different supply voltages around the design voltage of 800 mV. With the measurement equipment used, only single-ended measurements can be performed. The conversion gain would be 3 dB higher if fully differential measurements between IF LHCP+ and IF LHCP- were performed. Measurements on all four available outputs show similar results.

There is an extremely large deviation between the predicted conversion gain of about 20 dB and the measured value with a peak of only −13 dB. Several test pads on the chip allow the signal to be measured after each component. These measurements are only qualitative as the use of a 50 Ω probe leads to severe mismatch. Nevertheless, the signal amplitude has been found to be reduced mainly by the BBA, indicating a defect in this component. It should be noted that the chips in use here are the result of a research project and are first generation chips. To make the chips fully functional, further design iterations will be beneficial. To use the present chips for an active W-band receiver, the BBA is bypassed by a differential microstrip line on the chip. The bypass construction demands for additional bond wires. Figure 3.39 shows the realized conversion gain with the bypass. It increases by 40 dB at low frequencies and by approximately 15 dB at higher frequencies compared to the previous measurements.

Without the BBA, the simulation predicts a conversion gain of at least 8 dB. Even with the BBA bypassed, the measured conversion gain is well below this value, espe-

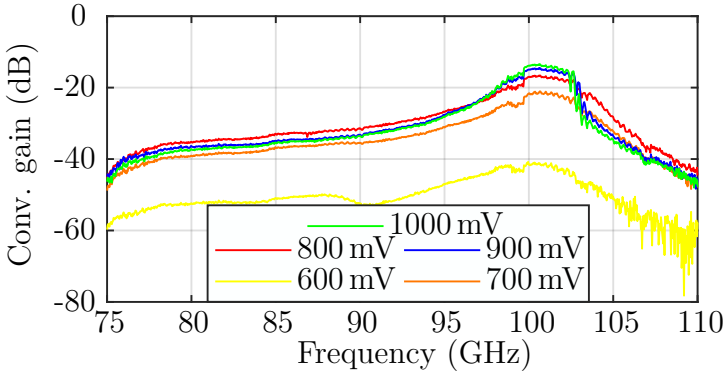



Figure 3.38: Measured single-ended conversion gain for the negative polarity of the LHCP channel (CH2) for various supply voltages with an LO power of 5 decibelm at 18.5 GHz.

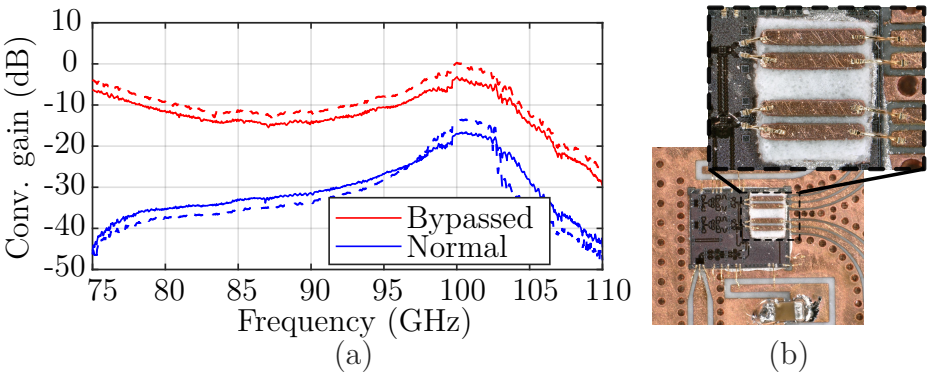



Figure 3.39: (a) Comparison of the measured conversion gain for the normal chip and the chip with the BBA bypassed. The solid and the dashed line are obtained with 800 mV and 1000 mV supply voltage, respectively. (b) Photograph of the bypass line on the chip.

cially at the upper edge of the frequency band. One reason for this is the bypassing of the BBA, which introduces a mismatch at the output of the mixer, since the 50 Ω-matched inputs of the unused BBA are not disconnected. Other reasons include the LNA, mixer, and quadruper, which are also first generation components and not fully validated. According to the specifications in [74], with all components working as simulated, the chip draws 375 mA. Without the BBA it is only 220 mA. However, in practice the chip only draws about 90 mA at the design supply voltage of 0.8 V. This suggests that the LNA and/or quadrupler are not working as intended. However, the basic functionality of downconverting a W-band signal is given and the chip's performance is sufficient for proof of principle demonstrations.

## 3.6 Power Combining Network

An array receiver combines the signals from several antennas. There are many concepts for receiver frontends, four of which are shown in Fig. 3.40. The combiner can be placed at different positions in the receiver chain. The first concept in Fig. 3.40a combines the power in the RF domain. The received signal is amplified, and then a phase shifter on each channel sets the desired phase for beam steering. Finally, a power combining network combines the signals from all elements in the RF domain. The advantage is that the entire array requires only one down-converter and ADC per polarization channel. The disadvantages of this approach are that the high frequency combining is lossy and the phase shifter must cover the entire RF frequency range.

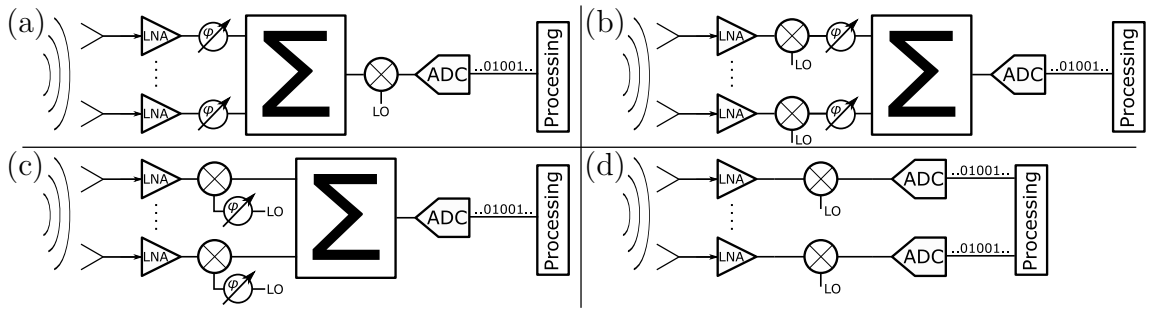



Figure 3.40: (a)-(d) Simplified frontend receiver architectures. Only a single polarization channel is shown and conceptually less important components are omitted.

The second combining approach operates in the IF domain (Fig. 3.40b). Here, the received signal is amplified and down-converted before combining. This requires one down-converter per channel, but still only one ADC for the array. However, phase shifting is challenging because the relative bandwidth is usually greater in the IF domain.

If the phase shifting is done in the LO path (Fig. 3.40c), only narrowband phase shifters are required. For this approach, each antenna element requires its own down-converter, but only one ADC for the entire array. It is only the high relative bandwidth of the IF signal compared to the RF signal that makes the combining difficult.

Finally, there is the possibility to do the combining and phase shifting in the digital domain, as shown in Fig. 3.40d. Here each antenna is followed by a complete receiver chain including amplification, down-conversion and digitization. Beamforming is done in software by summing the complex weighted receive signals. However, the processing is resource intensive, which makes this approach infeasible for broadband signals due to the large amount of digital data to be processed.

This work follows the third approach. The first two architectures would introduce high losses because the phase shifter must cover the entire W-band. A digital approach, combined with the expected data rate of 100 Gbit/s, would require too much processing power. For the chosen architecture, the challenge is to design a power combining network that covers the high relative bandwidth of the IF frequency range from 1 GHz to 36 GHz.

The approach for larger combing networks is to cascade multiple 2:1 power combining elements. Thus, only a single subelement needs to be designed in the first place, and cascading multiple copies of it leads to any desired $2^N$:1 combining network. This makes

it possible to scale the array to different sizes. For the single 2:1 power combiner, the Wilkinson approach [75] is used as the base element. Multiple line sections increase the bandwidth [76] and allow broadband power combiners to cover more than 160 % of relative bandwidth [77–80]. The combiner presented here has previously been published in [81].

### 3.6.1 Carbon Paste Resistors

An important aspect of integrating a power combiner into a multilayer stack is that no surface mount components can be used for the isolation resistors. In addition, the resistors must be very small to minimize parasitic effects. Carbon resistors can be realized with minimal dimensions using the process shown in Fig. 3.41a. Starting with a regular substrate with copper cladding on both sides ①, a pocket is etched into the top side at the desired resistor location ②. Carbon paste[8] fills the pocket ③. After curing at 150 °C for 30 min, the paste is sanded to flatten the resistor and remove paste residues around the pocket. The next step is to galvanically apply a copper layer to the entire PCB ④, which is often required anyway for plating through vias. Copper also forms on top of the carbon paste because it is conductive. The last step is to etch the PCB. The carbon paste is highly resistant to the etchant used. This releases the resistor that was previously buried under the copper ⑤. Small overlaps of the copper on the carbon paste ensure reliable electrical contact between copper lines and the carbon resistor. Two ways, which can also be combined, allow the resistance to be adjusted to achieve specific values. The first is to vary the length-to-width ratio of the carbon resistor. In addition, the manufacturer offers an insulating compound[9] that can be mixed with the carbon paste to reduce the resulting bulk conductivity of the

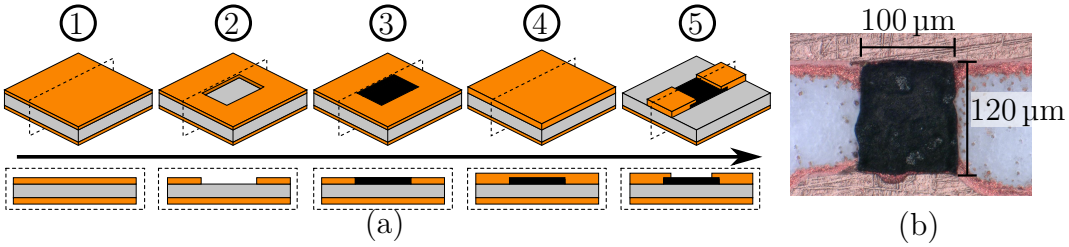



Figure 3.41: (a) Manufacturing process for integrated carbon paste resistors ①-⑤. (b) Example resistor.

[8] Lackwerke Peters GmbH & Co. KG, *SD 2843 HAL*
[9] Lackwerke Peters GmbH & Co. KG, *SD 2803 HAL*

paste. The resistor values required for the power combiner designed in this work (100 Ω to 200 Ω) are realized with a reasonable length-to-width ratios using the carbon paste without the insulating compound.

### 3.6.2 Stacked Power Combiner Design

As the output of the CMOS down-converter is differential [74], the power combiner must also be differential. This is achieved by stacking two identical multi-section Wilkinson combiners in a PCB stack as shown in Fig. 3.42. With equal amplitude and phase excitation at both inputs, a PEC plane can be inserted at the symmetry plane. This allows the structure to be split in half and only one half needs to be analyzed, which speeds up the simulation and optimization process. A four section approach for the Wilkinson combiner is chosen here because it is a good compromise between losses and isolation, as shown for three and five sections in [82].

The parameters of the power combiner, i.e., the resistance values, section lengths, and section impedances, are optimized in constrained full-wave simulation. Figure 3.43 depicts the resulting structure and the corresponding scattering parameters. Only the isolation of the two input ports is below 10 dB at low frequencies. To overcome this problem, the lengths of the four sections could be increased or more sections could be added. However, this would increase the size of the component and increase losses.

The via transition shown in Fig. 3.44 feeds the differential input and output ports of a stacked power combiner with a differential 100 Ω pair from the top layer. A detour behind the shorter via compensates for the difference in length of the vias. Full

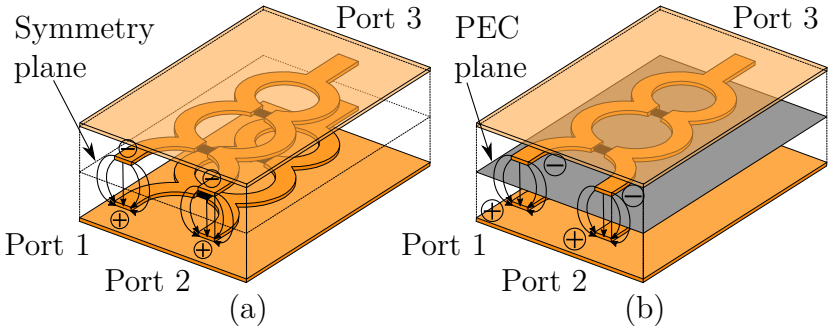



Figure 3.42: (a) Principle of the stacked Wilkinson power combiner to realize differential power combining. (b) PEC plane to bisect the device inserted at the symmetry plane. The substrate material is not shown and the top copper layer is transparent in both drawings.

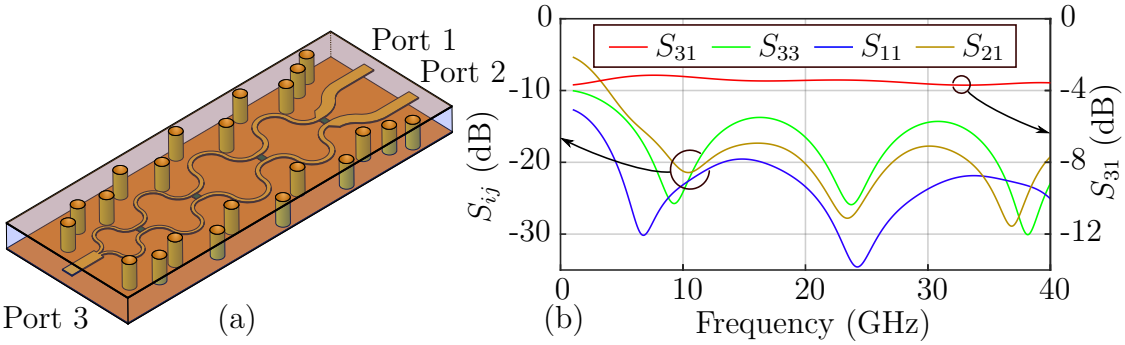



Figure 3.43: (a) Three dimensional view of the single-ended four section strip-line combiner. (b) Simulated scattering parameters.

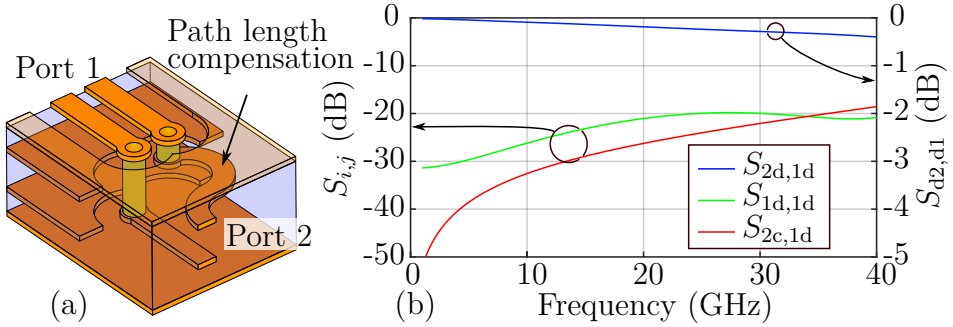



Figure 3.44: (a) Three dimensional view of the proposed transition with path length compensation. (b) Subset of the simulation results with the differential-to-differential transmission ($S_{2d,1d}$), the differential reflection ($S_{1d,1d}$), and the differential-to-common conversion ($S_{2c,1d}$).

compensation over the entire frequency range is not possible due to stray field effects at the vias. But as the simulation results show, the common mode excitation for a differential input at the top layer is below −20 dB up to 35 GHz. The optimized length of the detour is 370 µm, which matches well the via length difference of 400 µm.

Figure 3.45a displays the fully differential power combiner with the stacked four-section Wilkinson combiners and a differential via transition at each port. The two stacked Wilkinson combiners are fully integrated into the stack, covered by a ground plane at the top and bottom, and shielded by a via fence. Figure 3.45b shows the PCB stack, which consists of two cores of *RO4003C*[10] and one layer of *RO4450F*[11] prepreg.

[10]Rogers Corporation *RO4003C*
[11]Rogers Corporation *RO4450F*

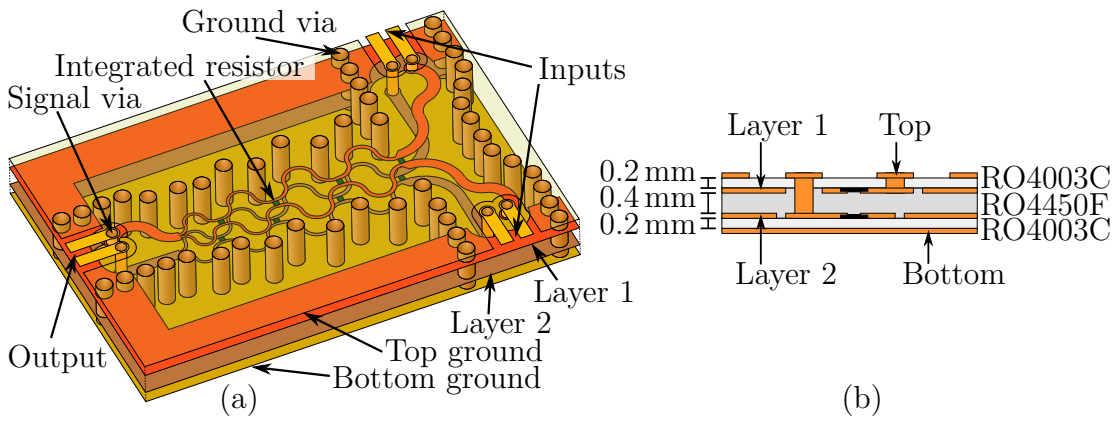



Figure 3.45: (a) 3D view on the fully differential power combiner. Top layer and substrate are transparent. Different colors are used to enhance the contrast between the copper layers. (b) Substrate stack.

### 3.6.3 Manufacturing and Measurements

For fabrication, the two cores are bonded to a 0.4 mm thick layer of prepreg, resulting in the required four copper layers. Prior to pressing, the resistors and traces are etched on the internal layers as shown in Fig. 3.46a-b. The combiner including the via transitions to the top layer has a size of only 5.8 mm by 8.5 mm. To measure the scattering parameters with the single-ended coaxial ports offered by the VNA[12], the differential pairs are split and terminated with connector landing patterns for 2.92 mm RPC as shown in Fig. 3.46c-d. Since the VNA has only four ports, multiple measurements

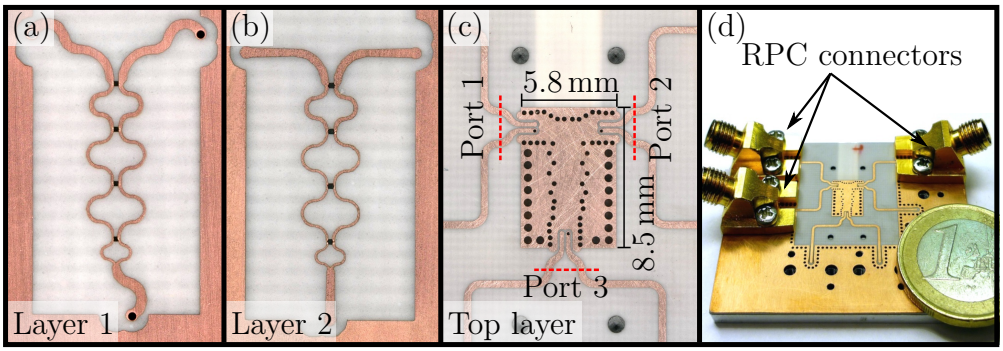



Figure 3.46: (a) and (b) inner layers with the integrated carbon resistors before pressing. (c) Close-up of the complete combiner with three differential ports. Calibration reference planes are indicated by red dashed lines. (d) The complete PCB with three of six RPCs mounted and an Euro for size comparison.

[12]Rohde & Schwarz GmbH & Co. KG *ZVA 50*

must be taken with the remaining ports terminated with 50 Ω loads. The single-ended measurement results are transformed to the modal scattering matrix according to [83].

Figure 3.47a reports the measured differential mode performance of the power combiner. The transmission coefficients from a differential input to the output are better than −5.3 dB up to 40 GHz. The input port isolation is better than 15 dB above 5 GHz and agrees well with the simulation. The differential mode reflection coefficients for all ports given in Fig. 3.47b are below −10 dB up to 36 GHz. The measurements do not fully reproduce the symmetry predicted by the simulation for the reflection coefficients at Port 1 and Port 2. This suggests that structural manufacturing tolerances affect the two inputs differently. However, the deviation from the predicted symmetry is small, so the manufacturing errors must also be small.

The cross mode transmission for differential excitation at the combiner input ports is given in Fig. 3.48a. It is important for the operation of the combiner that no common mode is excited by a differential input. For the frequency range up to 36 GHz, this excitation is always below −18 dB, which is sufficient for the target application.

Figure 3.48b plots the transmission coefficients for the common mode. These are of minor interest since the main objective is to combine differential signals and the common mode has not been considered in the optimization process. However, it shows that simulation and measurements are in good agreement for all measured modal scattering parameters.

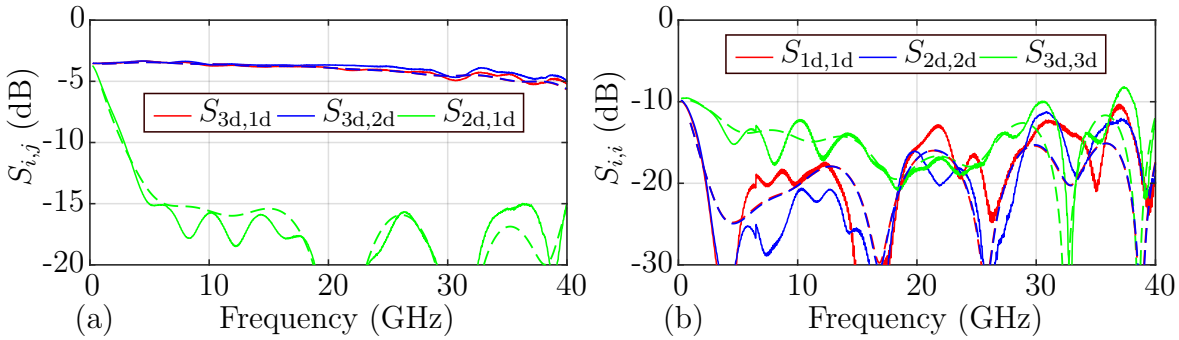



Figure 3.47: Measured (solid) and simulated (dashed) differential mode performance of the power combiner. (a) Transmission coefficients. (b) Reflection coefficients.

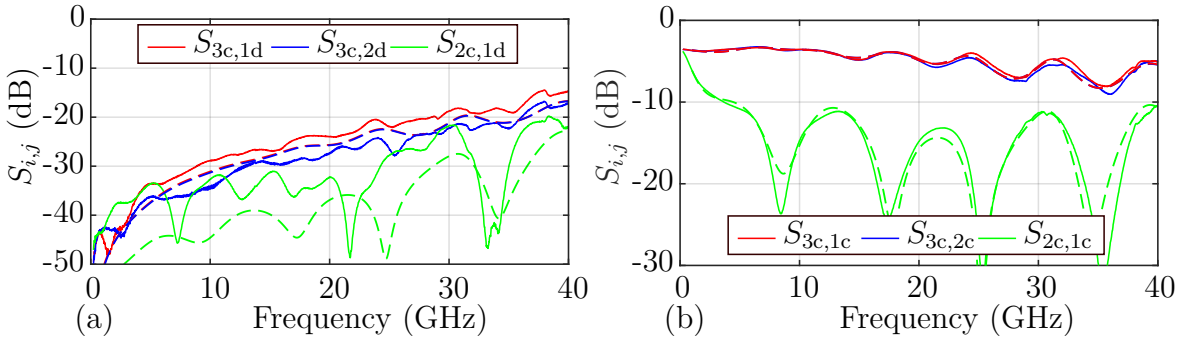



Figure 3.48: (a) Cross mode transmission for a differential input. (b) Transmission coefficients for a common mode excitation. Simulated and measured curves are dashed and solid, respectively.

### 3.6.4 Cascading Concept

For a combining network of an array with more than two elements, several 2:1 combiners must be cascaded. Figure 3.49 illustrates the basic scalable cascading concept for an exemplary four element array. Each down-converter chip outputs a differential RHCP and LHCP signal. Both need to be combined separately while maintaining the differential polarity. The proposed concept uses multiple via transitions with path length compensation for the differential signals. The concept is that the RHCP signal is routed in Layer 2 and the LHCP signal in Layer 1. Power combining uses stacked Wilkinson combiners that occupy both layers. Therefore, via transitions are required

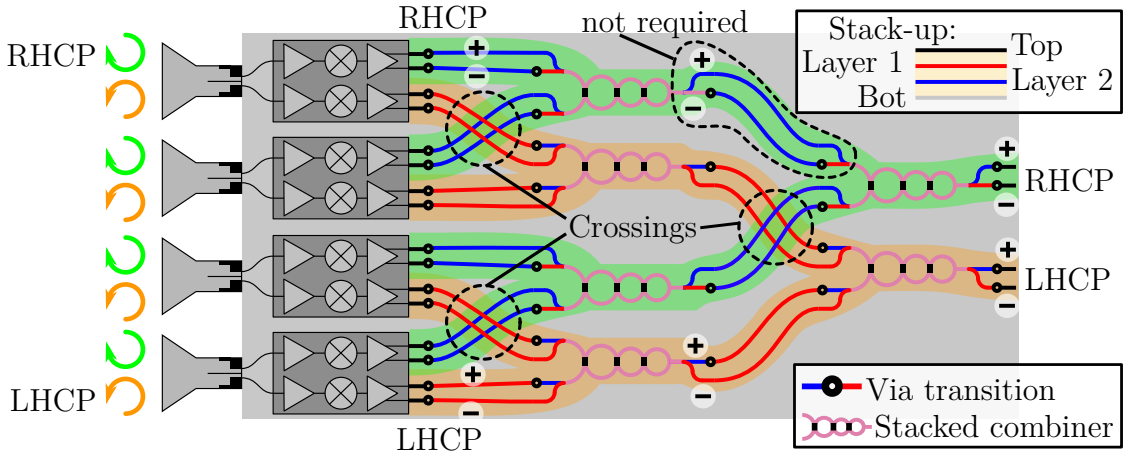



Figure 3.49: Basic cascading concept for a four element array, highlighting the signals that are routed in separate layers. The paths of the RHCP and LHCP signals are shaded green and orange, respectively. Other signals such as LO or DC distribution are not shown here.

before and after each power combiner. In principle, only the transitions before and after the crossings of the RHCP and LHCP signals are strictly required. However, to emphasize the concept of distributing the two signals to individual layers, the drawn concept includes all transitions. One not needed transitions is marked in Fig. 3.49. Of course, a design with more layers would allow complete separation of the two signals at the expense of manufacturing cost. The proposed network requires a multilayer stack with only two inner layers, simplifying manufacturing significantly.

A disadvantage of this approach is the fact that in the given concept there are three signal crossings without a shielding ground plane between the signal lines. However, if the lines are crossed in an orthogonal manner, cross-coupling is minimized. This is proven by the simulation results given in Fig. 3.50. The simulated structure has a twofold symmetry. Thus, the given subset of scattering parameters fully describes its behavior. The matching is excellent and the unwanted coupling between the two pairs of conductors exceeds −40 dB only above 30 GHz. Thus, the crossings proposed in the cascading concept can be realized in such a way that the combining behavior of the network is not noticeably affected.

Regarding the proposed combining network in Fig. 3.49, several transitions are necessary. First, the differential microstrip line at the chip output must be transitioned to a differential strip line on either Layer 1 or Layer 2, where it is routed to the power combiners. Both transitions are shown in detail in Fig. 3.51 and Fig. 3.52. They both include a 180° change in signal propagation direction to allow compact integration. This is useful for the array layout, including the antennas, because the signals can be routed directly under the chip.

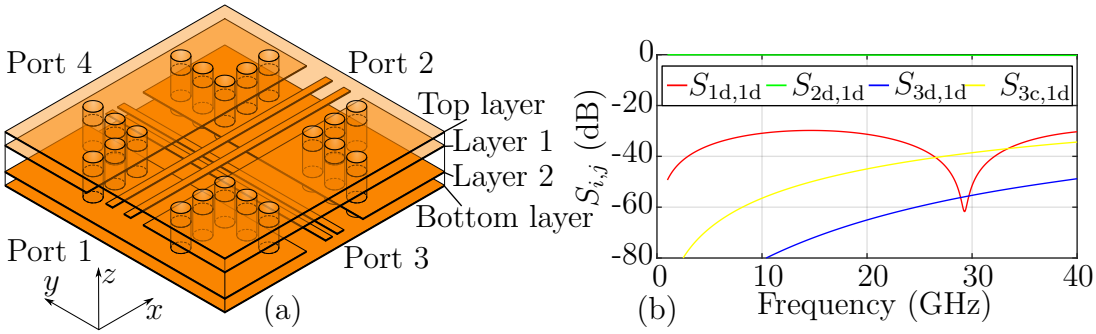



Figure 3.50: (a) Orthogonally crossing differential strip lines in 3D. Some copper layers are drawn transparent. (b) Subset of the simulated scattering parameters of the crossed lines.

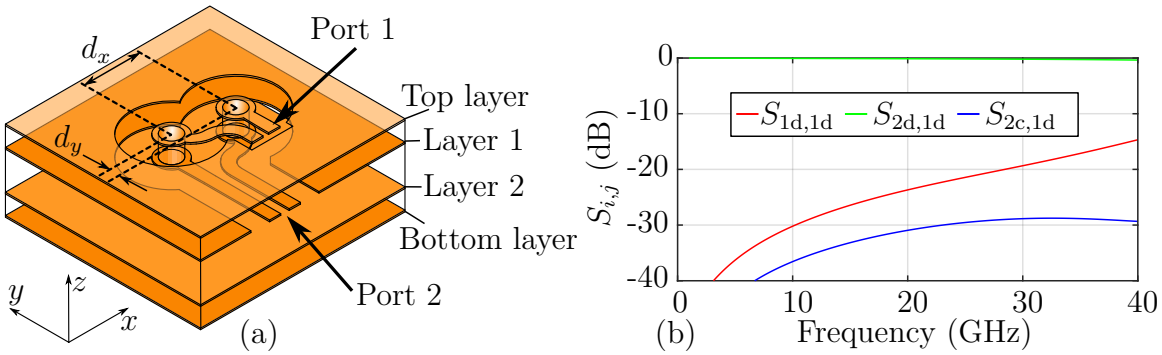



Figure 3.51: (a) Differential transition from top layer to Layer 1. (b) Simulated scattering parameters of the transition.

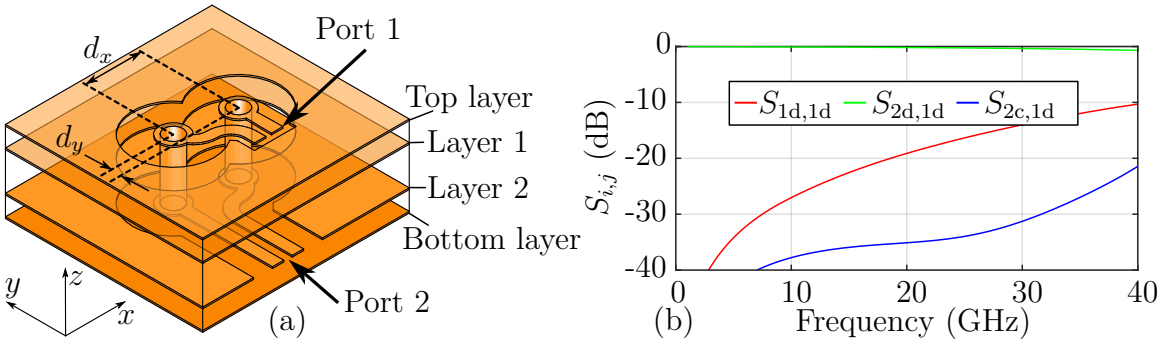



Figure 3.52: (a) Differential transition from top layer to Layer 2. (b) Simulated scattering parameters of the transition.

Due to the close proximity of the RHCP and LHCP outputs on the chip, the transitions must also be positioned very close to each other on the PCB to minimize the bond wire length. Therefore, the transitions are asymmetrical. The two vias have a diameter of 200 µm and a pitch in $x$ direction of $d_x = 590\,\mu\text{m}$ and in $y$ direction of $d_y = 100\,\mu\text{m}$.

In general, the RHCP IF and LHCP IF signals are routed on separate layers as horizontal-differential strip lines (HDSL) to allow crossings. However, the inputs of the differential Wilkinson combiners require a vertical-differential strip line (VDSL). Figure 3.53 shows the transition from HDSL at Port 1 to VDSL at Port 2.

The transition design uses the same principle of a detour line to compensate for the path length difference introduced by the via. The two ports are aligned in $x$-direction. This is a nice feature because, if needed in the routing process, the transition can be mirrored in the $xz$-plane to simply change the polarity of the transmission from Port 1 to Port 2 without changing the interfaces at either end.

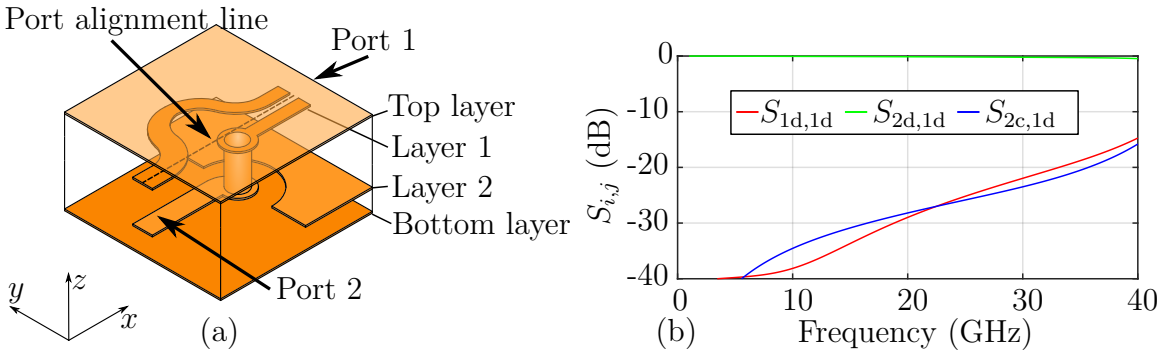



Figure 3.53: (a) Differential transition from HDSL in layer 1 to VDSL on Layer 1 and Layer 2. (b) Simulated scattering parameters of the transition.

Between the combiners, the signals are again transformed from vertical-differential to horizontal-differential strip line and back again to realize the necessary crossings. After the last combiner, the vertical-differential line can be transformed directly into a top layer differential microstrip line, since no further crossings are required. The transition from Fig. 3.44 is reused here.

For demonstration purposes, this work realizes a 2x2 planar array. Therefore, the concept of Fig. 3.49 is modified to allow a minimum number of transitions while maintaining symmetrical signal paths. Figure 3.54 displays the resulting circuit and specifies the general positioning of all the components.

All lines are routed on Layer 1 and Layer 2 except for a small section after the chips. This creates an intact ground plane on the top layer and on the bottom layer. To save space and keep the system compact, the antennas and even the chips can be placed on this ground plane, i.e., on top of the power combiners. By routing the combined output for the RHCP signal and the LHCP signal to the top and bottom respectively, only two crossings are required. The intact top layer provides enough space to route the LO and DC lines to the chips.

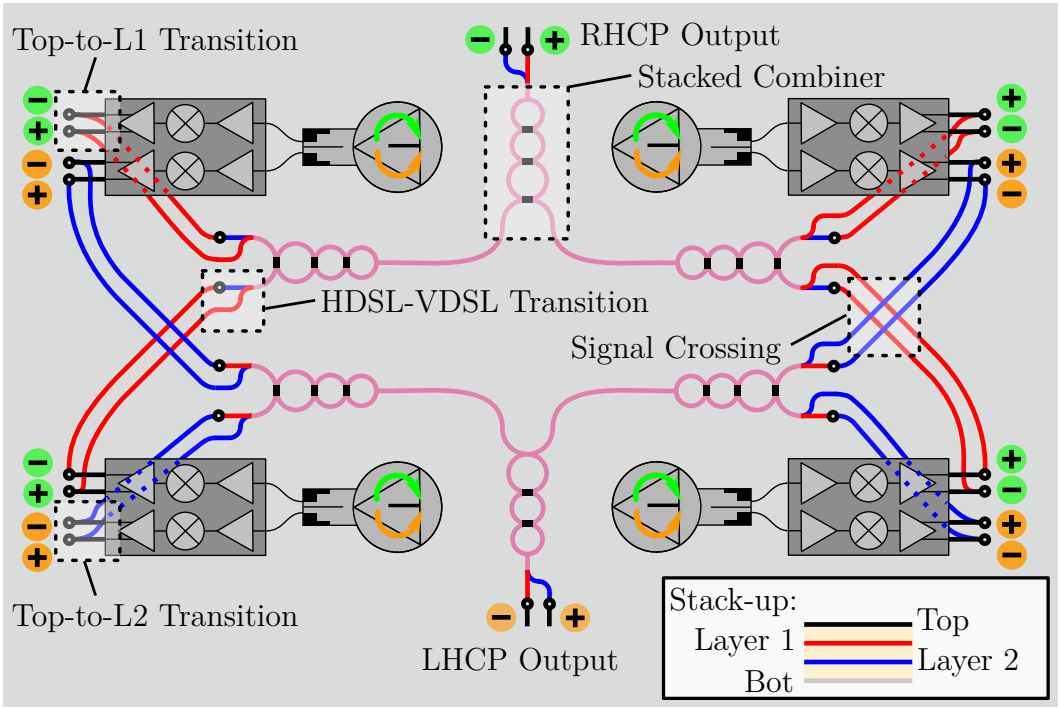



Figure 3.54: Concept of the 2x2 planar array combining network. Not to scale - the paths from the chips to the power combiners must have the same length for both polarizations.

# System Integration 4

The connection of the components from Chapter 3 forms the complete communication system. First, the passive frontend is developed and characterized as a passive single-element receiver. Next, an active system with an antenna and the CMOS chip is demonstrated. Finally, the complete system with an active 2x2 antenna array, an IF power combining network and beam scanning based on LO phase shifting is realized.

## 4.1 Passive Frontend

The passive frontend depicted in Fig. 4.1 consists of the antenna, the polarizer, and the waveguide-to-PCB transition. Its purpose is to receive a signal from free space, separate left and right circular polarization, and transform the signals to a PCB. The PCB also has sockets for coaxial connectors for attaching test equipment.

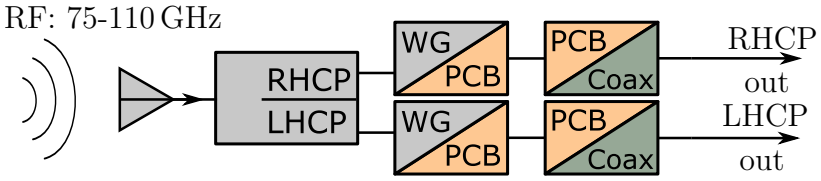



Figure 4.1: Components of the passive W-band receiver, from left to right: antenna, polarizer, waveguide-to-PCB transition, and PCB-to-coaxial transition.

### 4.1.1 Interface Design

Starting with the antennas in Section 3.1, the connection to the septum polarizer developed in Section 3.2 is straightforward because both components have the same waveguide interface. Thus, only the length of the triangular waveguide section, labeled $l_{\mathrm{conn},1}$ in Fig. 4.2a, needs to be determined. The dimensions of the triangular wave-

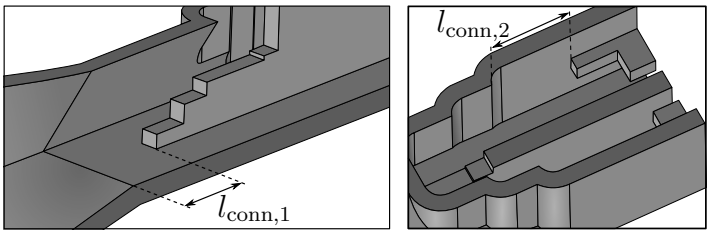



Figure 4.2: (a) Straight waveguide section connecting the polarizer to the antenna and (b) the waveguide-to-PCB transition to the polarizer. The walls of the component are partially removed to reveal the internal structure.

guide are such that only the two fundamental modes are above cutoff. The antenna is designed to suppress higher order modes, but cannot eliminate them completely. Therefore, if the connecting waveguide is too short for these modes to decay, unwanted effects such as resonances can occur, which would affect the antenna gain and the axial ratio. The interconnect length also affects the matching and isolation at the two polarizer output ports since the antenna is not perfectly matched. In general, the entire component should be as compact as possible to reduce losses and manufacturing costs. The length of the feed line $l_{\mathrm{conn,1}}$ is varied in simulation of the antenna connected to the polarizer to evaluate the behavior. This is done separately for all three scenarios. Table 4.1 lists the resulting values for the three scenarios. The length $l_{\mathrm{conn,1}}$ is chosen as a compromise between the achieved axial ratio and the port isolation. Significant gain degradation due to a longer $l_{\mathrm{conn,1}}$ as well as variations in matching are not observed.

The interconnecting rectangular waveguide section of length $l_{\mathrm{conn,2}}$ between the single-ended waveguide-to-PCB transition and the polarizer in Fig. 4.2b does not significantly affect the far-field characteristics of the antenna. Therefore, its length is determined based on a simulation that includes only the polarizer and the transition. The optimum length is found for the best matching at the GCPWG port transitions. Due to the sufficient matching of the designed antennas (see Table 3.2) all three scenarios use the same value for $l_{\mathrm{conn,2}}$. In summary, the length of the two straight waveguide

Table 4.1: Parameters for the straight waveguide sections connecting the individual components.

| | $\boldsymbol{l_{\mathrm{conn,1}}}$ | $\boldsymbol{l_{\mathrm{conn,2}}}$ |
|---|---|---|
| **Scenario** 1 | 1.2 mm | 1.1 mm |
| **Scenario** 2 | 1.0 mm | 1.1 mm |
| **Scenario** 3 | 1.2 mm | 1.1 mm |

interconnects has little effect on system performance due to the good matching of the individual components.

### 4.1.2 Manufacturing

This chapter compares two fabrication techniques for the passive frontends. One is a commercial metal 3D printing process[13] that uses additive manufacturing techniques to create the desired structure in steel. The second process uses a stereolithography (SLA) printer, an electroplating bath, and a furnace to realize 3D structures in copper. Thin walls are a challenge in the 3D printing process. Therefore, the wall thickness of the septum is increased to 0.45 mm. This requires an optimization of the other parameters for the polarizer, at the end of which almost the same performance is achieved as with the 0.35 mm thick septum.

Figure 4.3a shows the PCB for mounting the antennas. It has two connector patterns for the waveguide-to-PCB transition – one for each polarizer port. The connectors are on opposite sides of the antenna to facilitate connection of the measurement equipment. In Fig. 4.3b, the steel antenna designed for Scenario 2 is shown from different perspectives. It is manufactured by micro laser sintering of steel powder following the first manufacturing approach.

The antenna is attached to the PCB with the same conductive adhesive used to mount the single ended transition in Section 3.3.4. A *Finetec Fineplacer* places the antenna exactly on the footprint on the PCB. Figure 4.3c details the ridge placement at

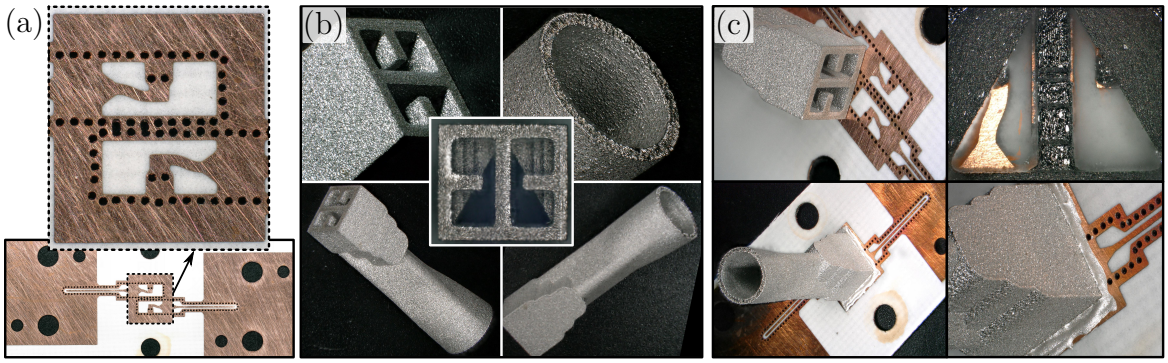



Figure 4.3: Assembly of the steel antenna for Scenario 2. (a) PCB with sockets for coaxial connectors and detail of the transition area. (b) Various views of the antenna. (c) Mounted components.

[13] 3D MicroPrint GmbH, Chemnitz, Germany *Micro Laser Sintering*

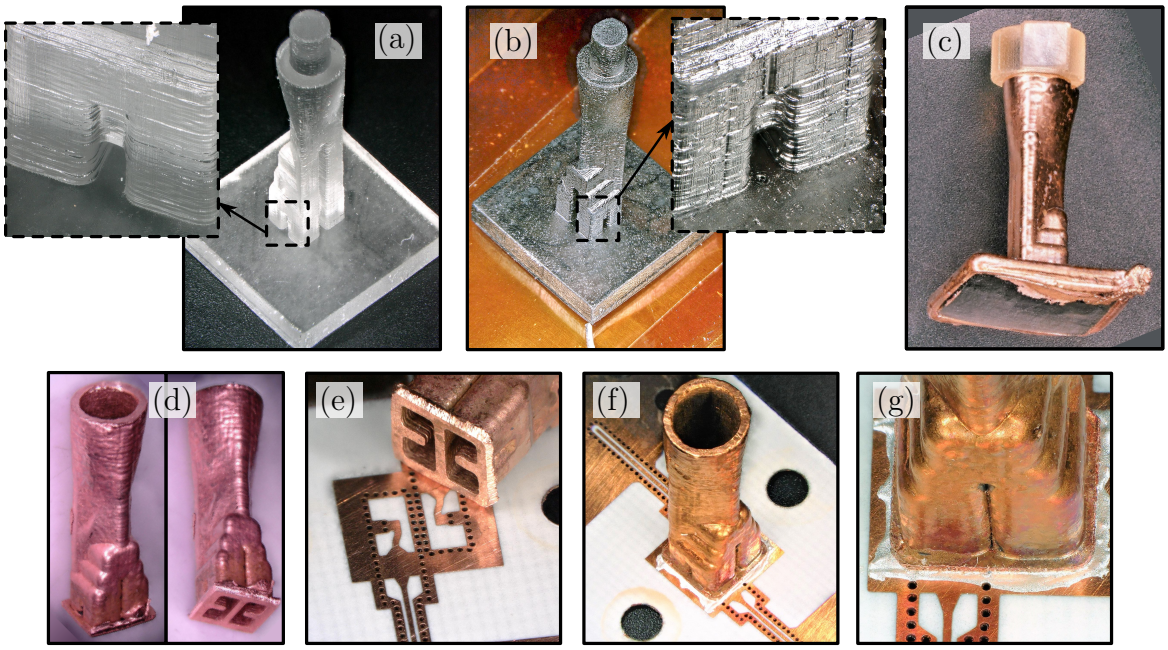



Figure 4.4: Manufacturing and assembly of the copper antenna for Scenario 2. (a) SLA printed plastic negative, (b) applied graphite layer, (c) plated component before removing the protection cap, (d) copper part after baking and trimming, (e)-(g) assembly using conductive adhesive.

the top right, looking through the antenna from above. The transition ridges precisely match the footprints on the PCB. Also, the inset of the center copper line, which is only 50 µm wide by design (see Table 3.8), extends symmetrically beyond both sides of the septum polarizer.

The second manufacturing approach is similar to the process in Section 3.3.4. Figure 4.4 shows the detailed realization of the antenna for Scenario 2 using this process. First, the inverted waveguide structure is printed in plastic. Next, a thin layer of graphite is applied to prepare the plastic surface for the subsequent galvanic copper plating. A non conductive plastic cap protects the antenna aperture from copper deposition. The thickness of the plated copper is approximately 0.4 mm. Subsequent baking of the part removes the plastic inside and results in an empty waveguide component. Excess copper at the bottom of the part is manually trimmed. The resulting copper part has the same internal structure as its steel counterpart. It is bonded to the PCB with the same adhesive used for the steel antenna to ensure a fair comparison. Alternatively, the copper horn can be soldered directly to the PCB using a standard surface mount process.

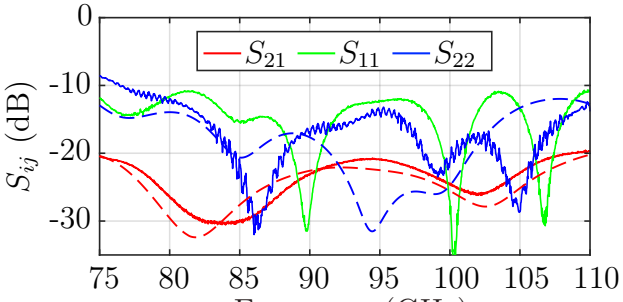
(a) (b)

Figure 4.5: (a) 3D printed steel antennas and (b) copper antennas. The top, middle and bottom antennas correspond to Scenario 3, Scenario 2, and Scenario 1, respectively.

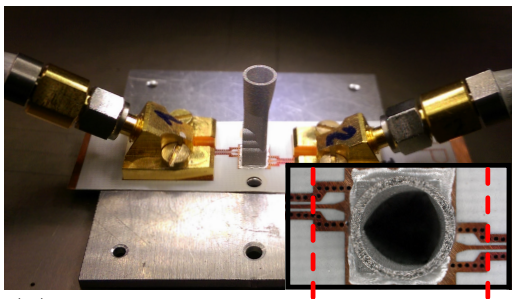
Antennas for all three scenarios are fabricated using the copper plating process and are also 3D printed in steel to compare the two processes. Figure 4.5 shows the resulting antennas in comparison. All use the same waveguide to PCB transition and septum polarizer. They only differ in their antenna parameters according to Section 3.1.

### 4.1.3 Measured Scattering Parameters

The scattering parameters of the assembled antenna are measured at the microstrip reference planes indicated in Fig. 4.6b using 1.0 mm RPC[14] coaxial connectors. It turns out that these connectors do not allow reliable and reproducible placement from




(a)




(b)

Figure 4.6: (a) Measured (solid line) and simulated (dashed line) scattering parameters of the assembled steel antenna for Scenario 2. (b) Measurement setup using angle mount connectors and a detailed top view with highlighted reference planes.

[14]Rosenberger Hochfrequenztechnik GmbH & Co. KG *RPC-1.00 SMD Connector 01K80A-40ML5*

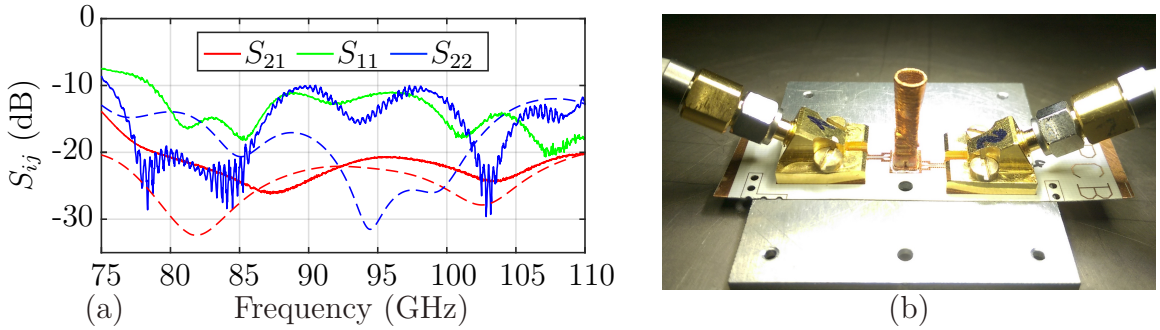



Figure 4.7: (a) Measured (solid line) and simulated (dashed line) scattering parameters of the copper antenna for Scenario 2. (b) Photo of the measurement setup with angle mount connectors.

calibration to measurements. The displacement mainly affects the measured reflection coefficients. Therefore, the reflection coefficients from the measurements are only a rough estimate of the actual antenna matching. On the other hand, the influence of the displacements on the measured transmission coefficient is small. The measurement results of the steel antenna assembly for Scenario 2 are shown in Fig. 4.6a.

As expected, the connector placement strongly affects $S_{11}$ and $S_{22}$, which deviate from the simulation. However, the measured matching is better than 9 dB, indicating proper antenna operation. The transmission coefficient is in good agreement with the simulated values. Thus, the geometric dimensions and electrical properties of the printed antenna appear to match the simulated ones.

Figure 4.7 shows the measurements of the copper antenna designed for Scenario 2. Similar to the previous measurements, the reflection coefficients are degraded by the connector displacement. The measured transmission coefficient agrees well with the simulated one above 85 GHz, but deviates below. This suggests larger manufacturing tolerances for the copper antenna compared to the steel antenna. In general, however, the copper component performs adequately.

For Scenario 1 and Scenario 3, Fig. 4.8 and Fig. 4.9 display the transmission coefficients between the two antenna ports. The results are similar to those obtained for Scenario 2. Again, the steel antenna performs as expected from the simulation. The copper antenna is slightly worse, especially at higher frequencies, but overall shows acceptable performance.

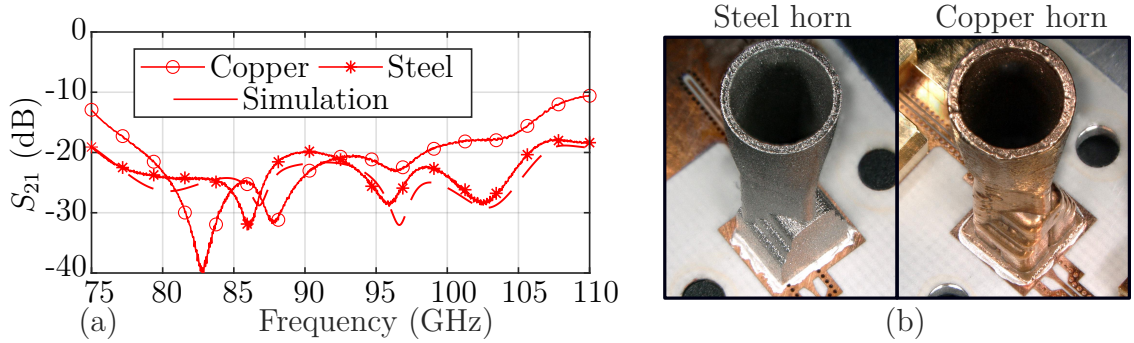



Figure 4.8: (a) Measured (solid line) and simulated (dashed line) scattering parameters of the steel and copper antennas for Scenario 1. (b) Photo of the antennas mounted on the PCB.

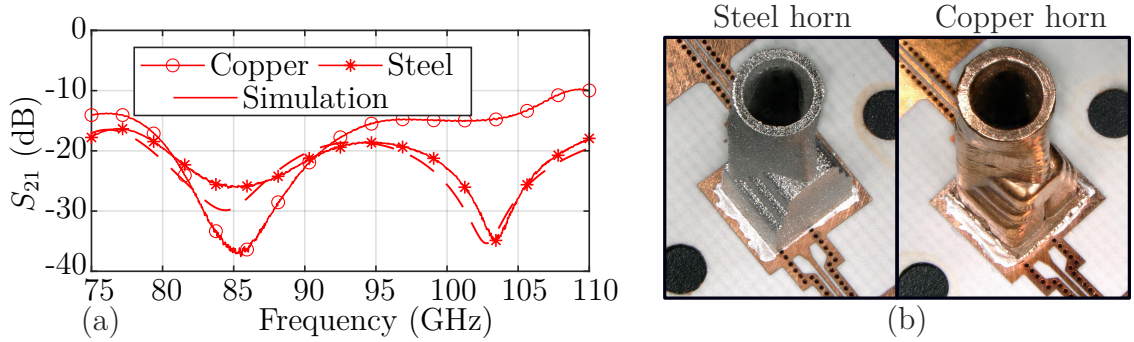



Figure 4.9: (a) Measured (solid line) and simulated (dashed line) scattering parameters of the steel and copper antennas for Scenario 3. (b) Photo of the antennas mounted on the PCB.

### 4.1.4 Antenna Characterization

The assembled antennas are measured in the anechoic chamber of the *Hamburg University of Technology* (TUHH). This gives a more accurate characterization of the antenna assemblies than just measuring the scattering parameters and allows a more detailed comparison.

#### Measurement Setup

In the anechoic chamber, a VNA operating up to 24 GHz is used to measure the high-frequency signals. Frequency converters extend the operating frequency range to perform measurements in the W-band. As shown in Fig. 4.10a, the anechoic chamber has three moving axes that are computer controlled. The circularly polarized receiving antenna is mounted on the right tower. It can be rotated about the azimuthal and the roll axis. On the left, a linearly polarized horn antenna transmits the continuous wave

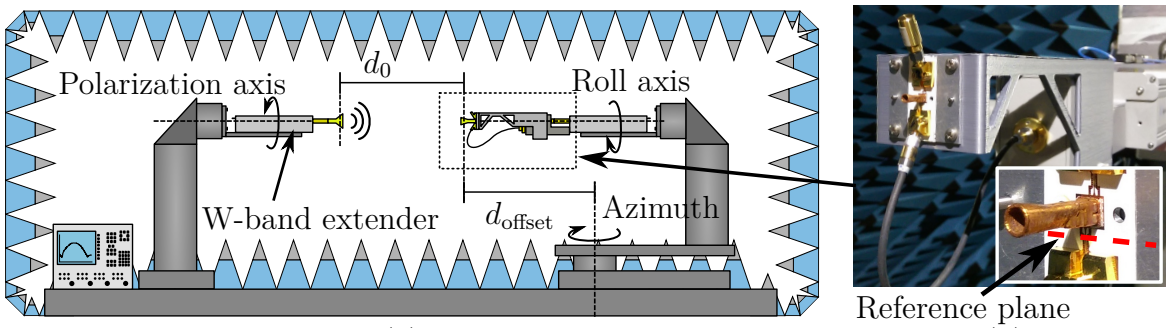



Figure 4.10: (a) Sketch of the anechoic chamber at TUHH with three moving axes. (b) Mounted AUT (here the copper horn for Scenario 2) on the receiving side with a 50 Ω load on the unused port. The metal mounting plate with the screws and pins is covered with absorptive material during the measurements to avoid detuning the AUT radiation characteristics.

test signal. It can be rotated about the polarization axis. To measure the polarization characteristics of the antenna under test (AUT), two measurements for vertical and horizontal polarization are required to calculate the radiation pattern with respect to RHCP and LHCP [24].

To obtain the AUT gain, first a known gain reference horn[15] $G_{\text{ref}}$ is measured in receive mode. As shown in Fig. 4.11, this horn connects directly to the WR10 flange of the waveguide extender module. The transmit antenna on the left is used for all measurements and is always fed with the same power. Next, the AUT replaces the reference horn and gain measurements are performed. To connect to the extender module, an auxiliary circuit is required, i.e., a WR10-to-coax transition, a 1.0 mm coax cable, and a 1.0 mm RPC. The losses introduced by these components are characterized separately by TRL measurements [73]. Therefore, the scattering parameters are measured at the WR10 ports of the two WR10-to-coax transitions, i.e., Port A and Port B shown in Fig. 4.11. Three different standards, i.e., thru, line, and reflect, are inserted between the two 1.0 mm connectors at the reference plane of the MSL (see Fig. 4.10b. Applying the method from [73] yields, among other parameters, the transmission coefficient $S_{21,\text{aux}}$ of the auxiliary circuit. Finally, the realized gain, corrected to the reference plane indicated in Fig. 4.10b, calculates to

$$G_{\text{AUT}} = \frac{P_{\text{AUT}}}{P_{\text{ref}}} \cdot \frac{G_{\text{ref}}}{(S_{21,\text{aux}})^2}. \tag{4.1}$$

[15] Custom Microwave Inc. *RCHO10R*

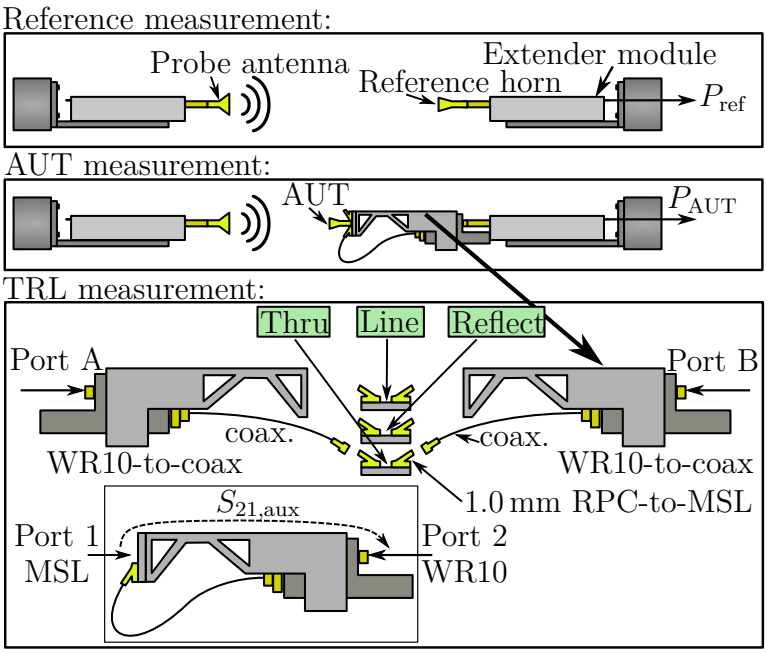



Figure 4.11: Measurements performed to evaluate the realized gain of the AUT.

This approach neglects the return loss of the auxiliary circuit. However, according to the results of the TRL measurements, it is better than 10 dB. This corresponds to the RPC performance specified by the connector manufacturer (see Footnote 14). A mismatch of less than 10 dB is accepted here because its effect on the measurements is only a small ripple superimposed on the measured antenna characteristics.

As indicated in Fig. 4.10a, the polarization axis and roll axis align with the two antennas, but due to the length of the waveguide extender and the mounting bracket, there is an offset $d_{\mathrm{offset}}$ between the azimuth axis and the AUT phase center. This leads to a twofold influence on the measurements of the antenna, as shown in Fig. 4.12. First, the effective distance $d_x$ between the AUT and the probe varies with the azimuth scan angle $\alpha$. Second, the angle $\beta$ at which the probe emits toward the AUT also varies with $\alpha$. The first effect leads to an increased path loss due to the larger distance $d_x$ as a function of $\alpha$, which calculates to

$$d_x = \sqrt{d_{\mathrm{offset}}^2 + (d_0 + d_{\mathrm{offset}})^2 - 2d_{\mathrm{offset}}(d_0 + d_{\mathrm{offset}})\cos(\alpha)}. \tag{4.2}$$

Knowing the path length increase allows the path loss variation to be calculated and compensated for in the post-processing of the measurements.

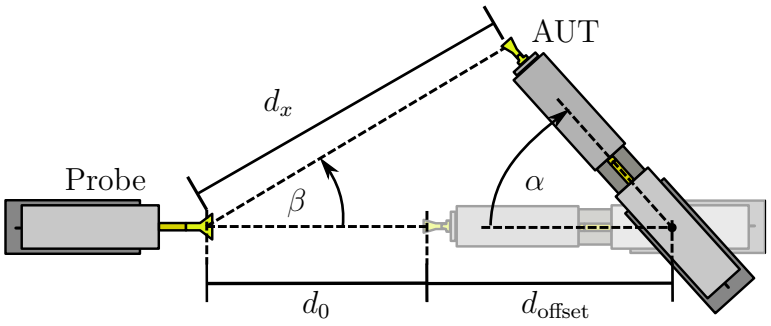



Figure 4.12: Top view of the measurement setup showing the effect of an azimuth rotation with the antenna phase center not aligned with the rotation axis. The drawing is not true to scale to emphasize the effect of the antenna displacement on the measurements.

The second effect is caused by the probe radiation angle

$$\beta = \arccos\left(\frac{d_x^2 + (d_0 + d_{\text{offset}})^2 - d_{\text{offset}}^2}{2d_x(d_0 + d_{\text{offset}})}\right). \tag{4.3}$$

Since the probe antenna has a directional gain pattern, the effective gain in the direction of the AUT depends on $\beta$. Using the probe antenna radiation pattern provided by the manufacturer, the gain differences are calculated and the measurement data are corrected in post-processing. With the present setup, the path length variation causes additional 1.5 dB loss in the worst case. The maximum value for $\beta$ is 8.5° at an azimuth angle of 90°. This results in an 8.5 dB reduction of the effective gain of the probe antenna.

To accurately measure the polarization characteristics of the AUT, several methods are available [24, 84, 85]. Since the anechoic chamber at TUHH is capable of measuring magnitude and phase of the transmission between two antennas in the W-band, the phase-amplitude method [24] is used to determine the polarization characteristics of the AUT. Figure 4.13 illustrates the simplified setup for this method. Here, the complex

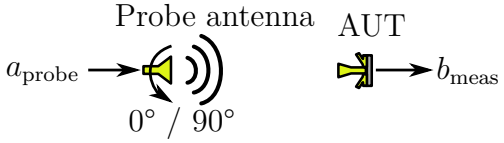



Figure 4.13: Illustration of the two measurements with different probe antenna angles required to determine the polarization characteristics of the AUT.

wave $a_{\text{probe}}$ feeds the linearly polarized probe antenna and the AUT receives the wave $b_{\text{meas}}$. Measurements are performed with two orthogonal orientations of the probe

antenna, e.g., 0° and 90°. According to [24], the axial ratio calculates to

$$AR = \frac{\sqrt{S_0^2 + S_{90}^2 + \sqrt{S_0^4 + S_{90}^4 + 2S_0^2 S_{90}^2 \cos(2\phi_0 - 2\phi_{90})}}}{\sqrt{S_0^2 + S_{90}^2 - \sqrt{S_0^4 + S_{90}^4 + 2S_0^2 S_{90}^2 \cos(2\phi_0 - 2\phi_{90})}}}, \tag{4.4}$$

with

$$\begin{aligned} S_0 &= \left|\frac{b_{\text{meas}}}{a_{\text{probe}}}\right| \qquad \text{for the probe antenna at } 0°, \\ \phi_0 &= \arg(S_0), \\ S_{90} &= \left|\frac{b_{\text{meas}}}{a_{\text{probe}}}\right| \qquad \text{for the probe antenna at } 90°, \\ \phi_{90} &= \arg(S_{90}). \end{aligned} \tag{4.5}$$

Thus, only two orthogonal measurements are required to determine the axial ratio. However, phase stability between the two measurements is critical. In the anechoic chamber at TUHH, high performance rotary joints[16] ensure phase stable measurements independently of probe antenna rotation.

### Antenna Measurements

Figure 4.14 defines the coordinate system used to display the measured antenna properties and the port numbering. Measurements over $\theta$ for $\phi = 0°$ and $\phi = 90°$ are made at both antenna ports for the steel antennas (Scenario 1-3) and the copper antennas (Scenario 1-3). Only the triangular waveguide section and the polarizer cause an asym-

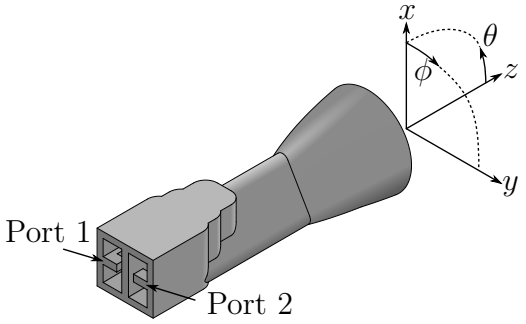



Figure 4.14: Definition of the coordinate system and port annotation used for antenna measurements. Port 1 and Port 2 correspond to RHCP and LHCP, respectively.

[16]SPINNER GmbH *1 channel rotary joint style I DC-50 GHz 2.4 mm female*

metry in the antenna structure. The radiation aperture of all antennas is rotationally symmetric. Therefore, the two measurements along $\phi = 0°$ and $\phi = 90°$ are expected to give similar results.

The notation of the following plots always indicates the angular range of interest, which is $|\theta| \leq 15°$, $|\theta| \leq 30°$, and $|\theta| \leq 45°$, respectively, with vertical black lines. The simulation data are dashed and the measured data are solid. The axial ratio in (dB) is shown in black and the gain values in (dBi) for RHCP and LHCP are plotted in red and blue, respectively.

### Steel Antennas

The radiation characteristics of the steel antenna designed for Scenario 1 measured at Port 1 are given in Fig. 4.15 for $\phi = 0°$ at selected frequencies. In the main beam direction ($\theta = 0°$) the measured axial ratio is below 2 dB over the whole frequency range. This compares well with the 1.2 dB predicted by the simulation. The simulated and measured RHCP gains differ by about 1.5 dB. This indicates that the simulation underestimates the losses.

Figure 4.16 displays the maximum axial ratio and minimum copolar gain over the $|\theta| \leq 15°$ angular range of interest obtained in the measurements for $\phi = 0°$. The maximum axial ratio over the angular range of interest is less than 2.1 dB up to 104 GHz and increases to 3.8 dB for higher frequencies, which is in good agreement with the simulation. This indicates that there are only small manufacturing tolerances in the realized antenna. On the other hand, the difference between the realized and simulated gain clearly indicates higher losses for all measured frequencies. A possible cause of the increased losses is that the surface roughness is higher than expected.

Since the entire antenna structure is symmetrical with respect to its two ports, the only expected difference is the change from RHCP to LHCP, resulting in the same measured absolute values. In practice, however, imperfections in the realized prototype lead to asymmetries. Figure 4.16 also shows the maximum axial ratio and minimum gain measured at Port 2 over the corresponding theta angle of $|\theta| \leq 15°$. The results show only small differences compared to the measurements taken at Port 1, proving a high degree of symmetry in the realized antenna.

Figure 4.17 shows the realized gain and axial ratio over $\theta$ for $\phi = 0°$ measured at Port 1 of the steel antenna designed for Scenario 2. The general shape of the radiation

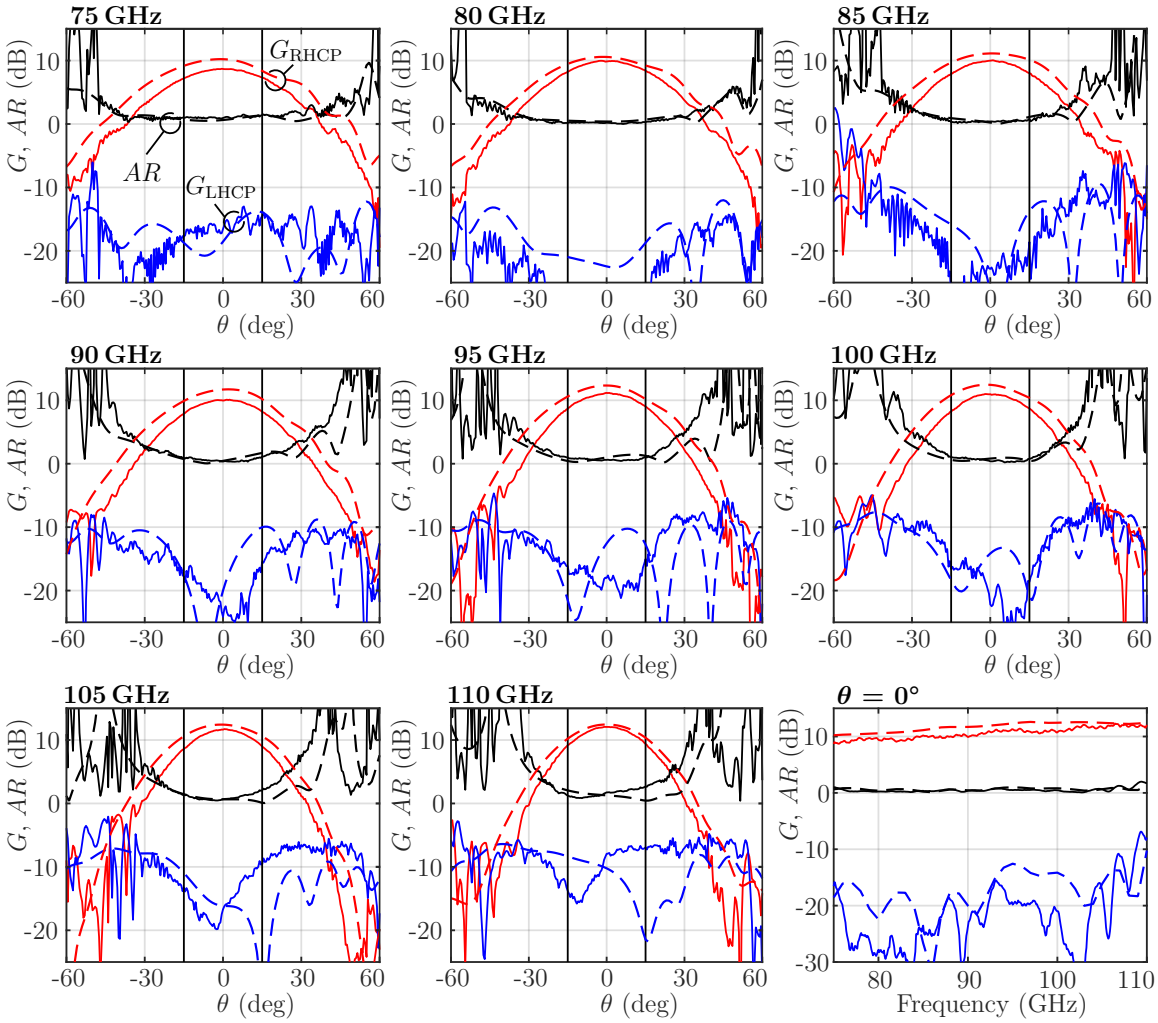



Figure 4.15: Measured (solid line) and simulated (dashed line) antenna properties at Port 1 of the steel horn for Scenario 1 at $\phi = 0°$.

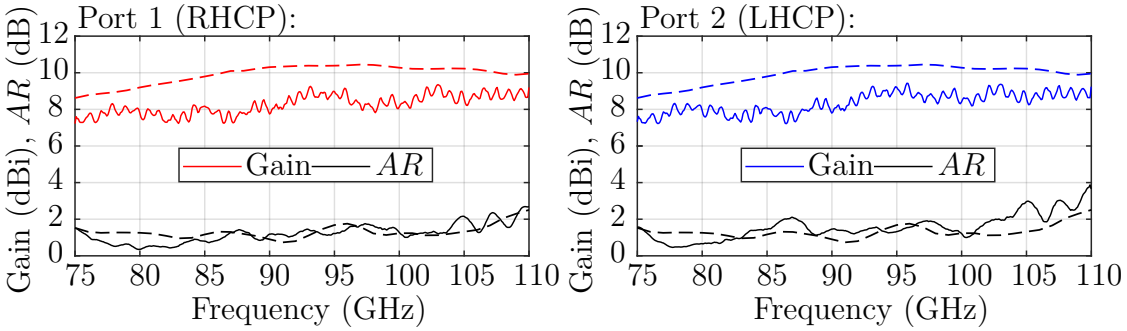



Figure 4.16: Minimum realized gain and maximum axial ratio in the angular range of interest for the steel horn for Scenario 1 for $\phi = 0°$. Simulated and measured curves are dashed and solid, respectively.

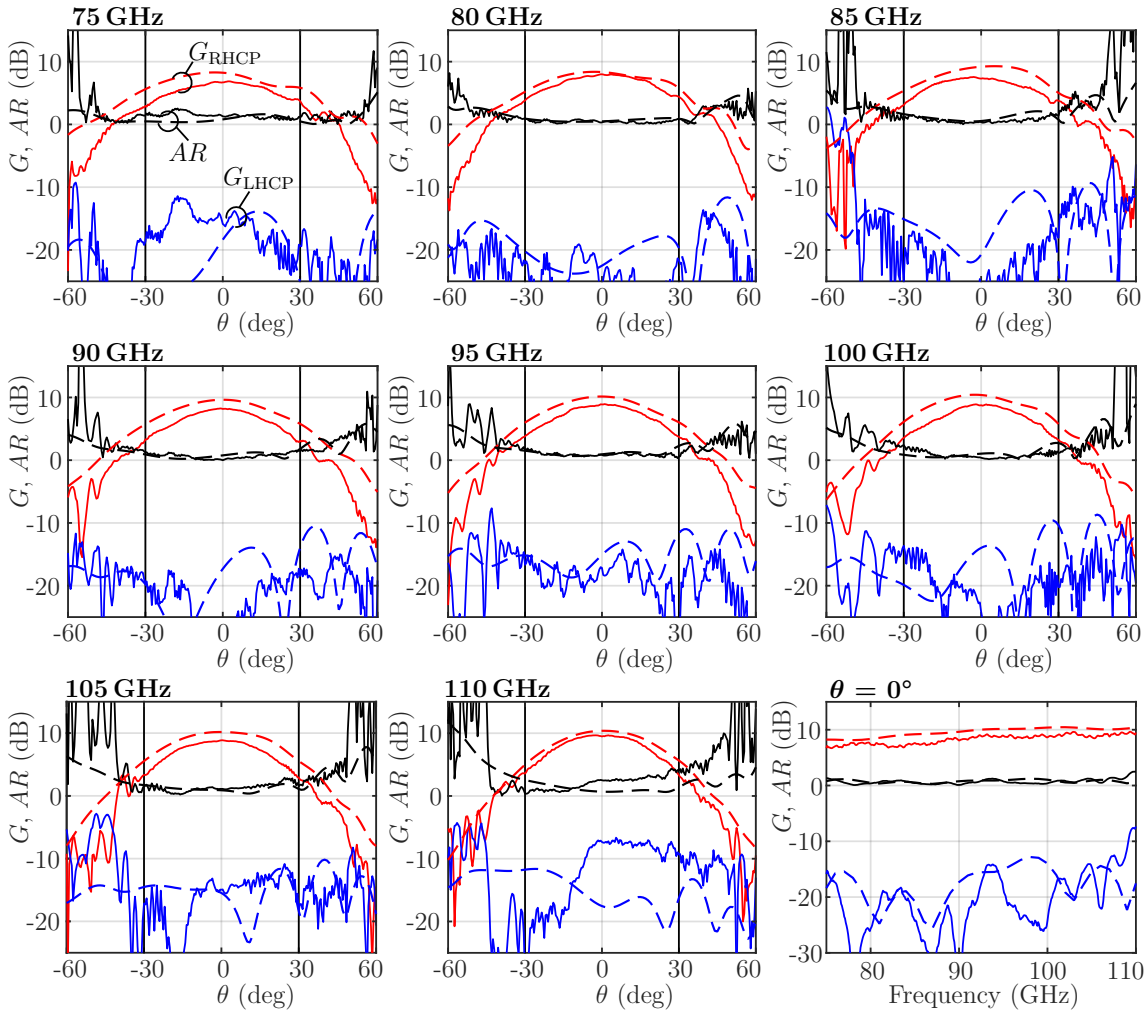



Figure 4.17: Measured (solid line) and simulated (dashed line) antenna properties at Port 1 of the steel horn for Scenario 2 at $\phi = 0°$.

pattern is in good agreement with the simulation. However, as observed earlier, the measured gain is lower than expected. The measured axial ratio in the design angular range of $|\theta| \leq 30°$ remains below 3 dB except around 110 GHz. Here, for $\theta = 30°$, an axial ratio of up to 4.5 dB is measured. However, this value is observed at the edge of the targeted angular range. Considering only the main beam direction, the axial ratio remains below 2.5 dB.

The worst case properties for axial ratio and gain over the angular range of interest are given in Fig. 4.18. Here, the discrepancy in realized gain between measurements and simulation is larger than for the Scenario 1 antennas. The deviation ranges from

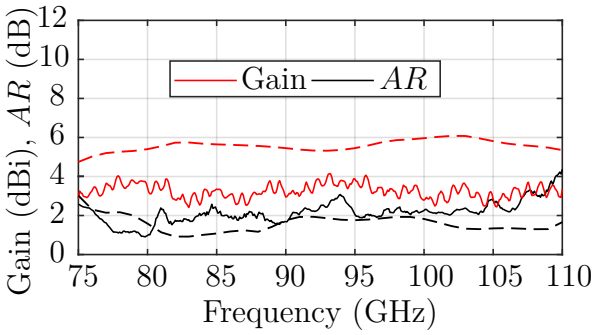



Figure 4.18: Minimum realized gain and maximum axial ratio in the angular range of interest for the steel horn for Scenario 2 measured at Port 1 for $\phi = 0°$. Simulated and measured curves are dashed and solid, respectively.

1.2 dB to 3 dB. The axial ratio, on the other hand, is within the simulated range, except for frequencies close to 110 GHz.

The simulated and measured far-field properties of the steel horn designed for Scenario 3 are given in Fig. 4.19 for $\phi = 90°$. Here, the relevant angular range of interest is much larger with $|\theta| \leq 45°$, resulting in multiple frequencies with large deviations toward $\pm 45°$. These deviations, e.g., for $\theta = 45°$ and at 110 GHz, are mostly related to the axial ratio and occur only at the limits of the angular range of interest. Gain deviations of a similar magnitude as previously observed are also present. In the main beam direction, the measured and simulated characteristics are in good agreement. Especially in the main beam direction, the axial ratio is very close to the simulation. Here, the measured values remain below 1.7 dB as predicted by the simulation.

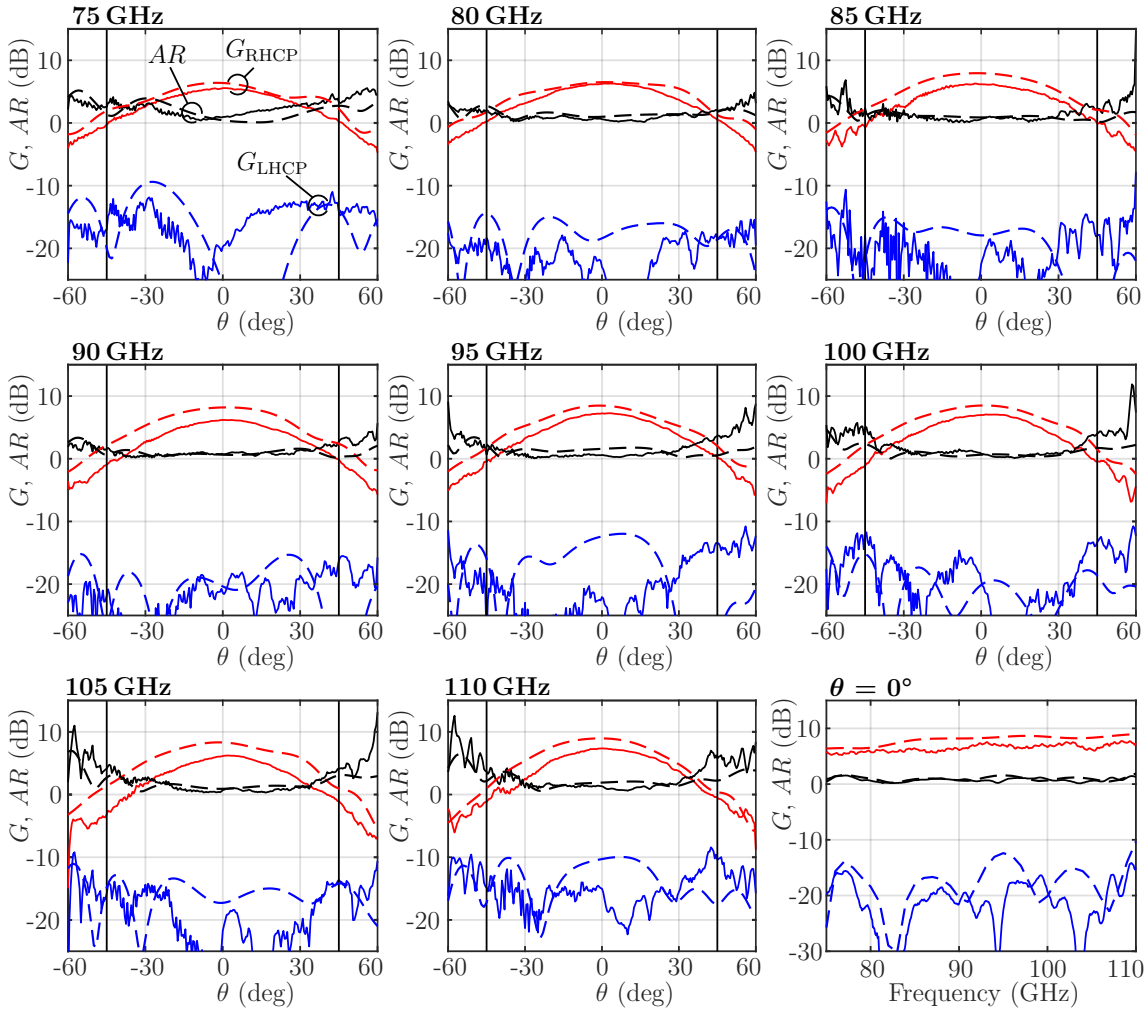



Figure 4.19: Measured (solid line) and simulated (dashed line) antenna properties at Port 1 of the steel horn for Scenario 3 at $\phi = 90°$.

### Copper Antennas

Figure 4.20 shows the maximum axial ratio and minimum gain measured at Port 1 and Port 2 of the copper antenna for Scenario 1. The measurements show that at Port 1 serious defects drastically reduce the gain and increase the axial ratio compared to the simulation.

The measurements taken at Port 2 show a better performance. The gain response agrees well with the simulated one, except for very low frequencies and the offset previously present due to the losses. The axial ratio is still significantly different from the simulation. This suggests that a manufacturing defect in the polarizer disturbs the axial ratio in both ports, and another defect near the waveguide-to-PCB transition to Port 1 reduces the measured gain at that port.

Figure 4.21 depicts the antenna characteristics measured at Port 1 of the antenna for Scenario 2 with $\phi = 0°$. At 75 GHz there is a significant degradation in performance compared to the simulation. This indicates manufacturing tolerances, especially at low frequencies, as already indicated by the scattering parameter measurements of this antenna (see Fig. 4.7). Nevertheless, a discrimination of more than 10 dB between RHCP and LHCP is measured even at 75 GHz, demonstrating proper operation. Above 80 GHz the measurements agree well with the simulation. Especially the maximum measured axial ratio of 4 dB over the whole scenario specific angle and frequency range given in Fig. 4.22 is close to the simulation. Compared to the steel measurements, the losses increase by about 0.5 dB for the copper horn, as suggested by the reduced peak gain. However, these measurements prove the feasibility of the proposed manufacturing technique for 3D printed components at W-band.

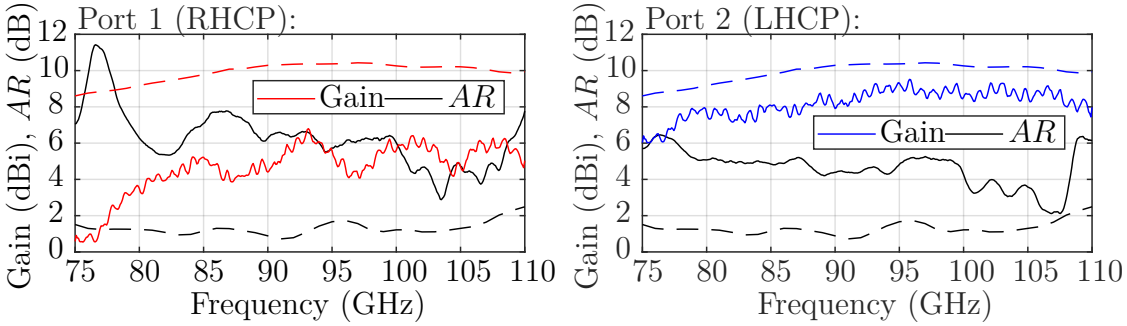



Figure 4.20: Minimum realized gain and maximum axial ratio in the angular range of interest for the copper horn for Scenario 1 for $\phi = 0°$. Simulated and measured curves are dashed and solid, respectively.

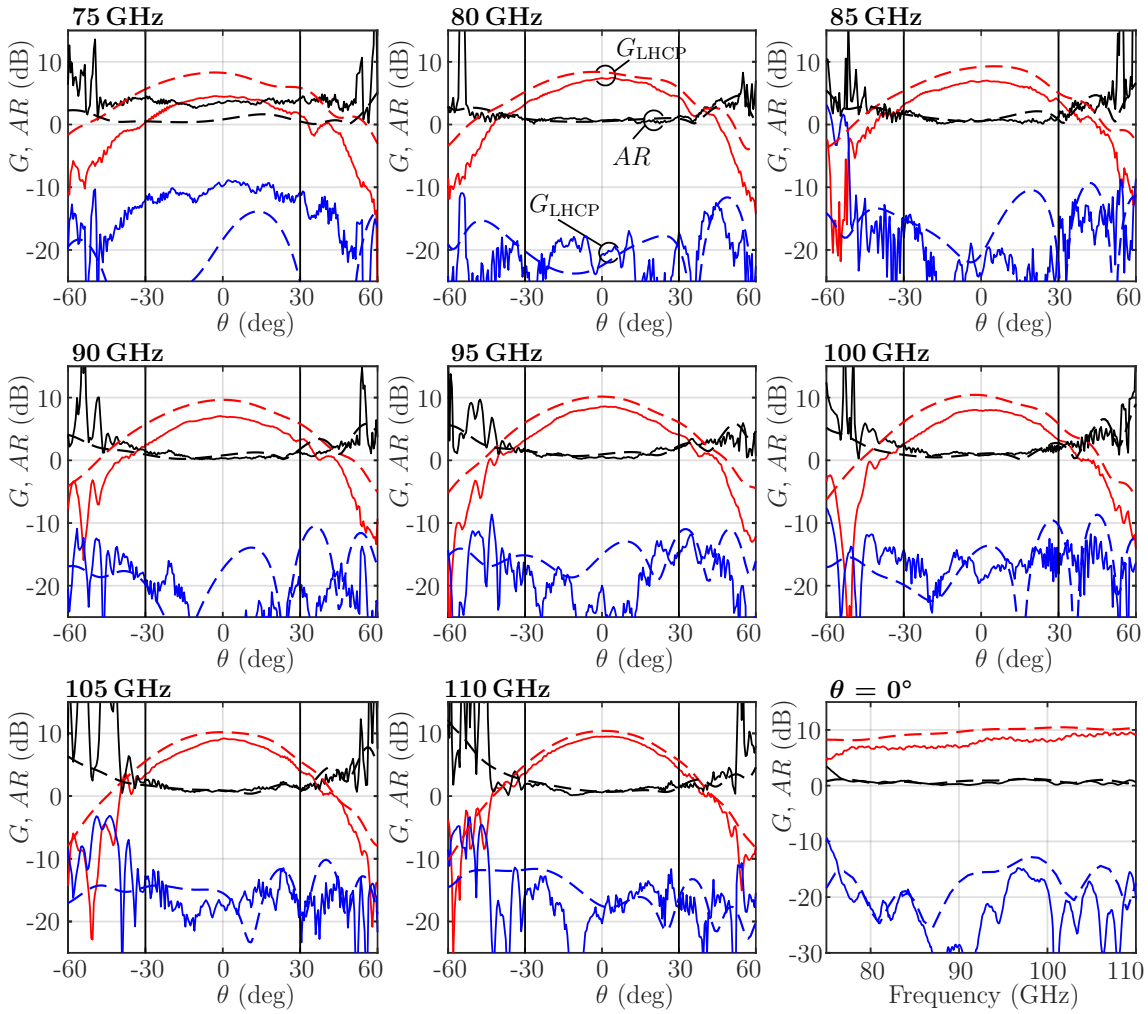



Figure 4.21: Measured (solid line) and simulated (dashed line) antenna properties at Port 1 of the copper horn for Scenario 2 at $\phi = 0°$.

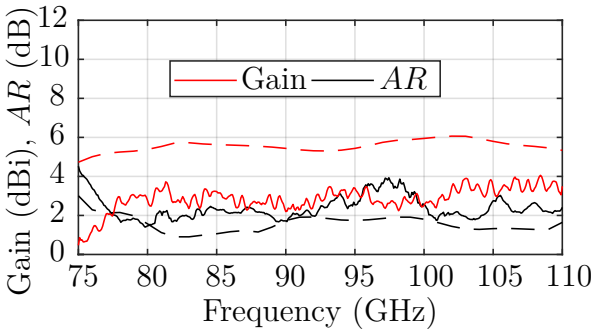



Figure 4.22: Minimum realized gain and maximum axial ratio in the angular range of interest for the copper horn for Scenario 2 measured at Port 1 for $\phi = 0°$. Simulated and measured curves are dashed and solid, respectively.

Finally, the copper antenna measurements for the ±45° scenario are given in Fig. 4.23 for $\phi = 90°$. The largest differences occur at 110 GHz, where RHCP and LHCP gain are nearly equal. At all other frequencies, the design goal of a wide, flat dispersion pattern and low axial ratio is basically achieved.

In summary, the steel antennas perform better than the copper ones. However, for Scenario 2, the copper antenna almost matches the performance of the steel antenna. The commercial steel 3D printing process is well tuned, resulting in very high dimensional accuracy with low tolerances. In contrast, the copper horns produced by the developed 3D printing and plating process are subject to several manual manufacturing steps, such as trimming off excess copper. As a result, they are more susceptible to

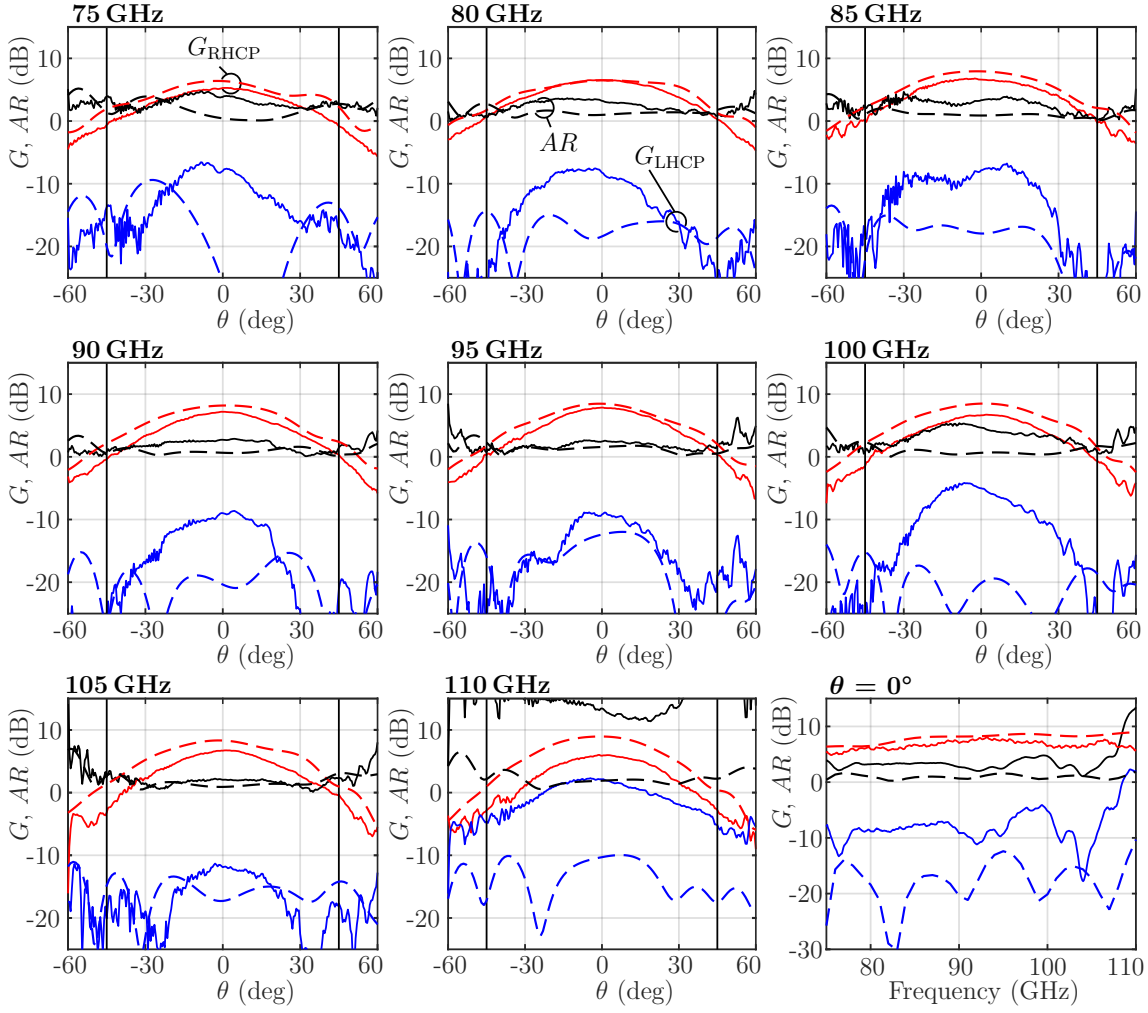



Figure 4.23: Measured (solid line) and simulated (dashed line) antenna properties at Port 1 of the copper horn for Scenario 3 at $\phi = 90°$.

defects and tolerances. In addition, the 3D printing process using the SLA printer can lead to defects in the printed parts due to print tank degradation or dust particles in the laser path. However, the results demonstrate the applicability of this process for the fabrication of complex components operating in the W-band. Especially at even lower frequencies, the relaxed tolerance requirements make this technique suitable for this application area.

For the realization of the active receivers, printed steel antennas for Scenario 2 are used in this work due to their good agreement with simulation. In addition, the ten steel horns from the same printing batch are nearly identical, which is necessary to obtain a functional antenna array. Furthermore, the antenna for Scenario 2 offers a good compromise between gain and main lobe width, while achieving a good axial ratio.

## 4.2 Active Single-Element Receiver

The active single-element receiver combines all components presented in Chapter 3 except the power combining network. So it basically integrates the previously presented passive receiver and the down-conversion CMOS chip.

### 4.2.1 Design and Manufacturing

Figure 4.24 presents an exploded view of the active receiver. A 200 µm thick *RO4003C* substrate, which is the same material used in the combiner design in Section 3.6, forms the base PCB of the receiver. This allows parts of the design to be reused later for the array receiver. The base PCB is mounted with screws and alignment pins on a solid aluminum plate, which acts as a heat sink and provides rigidity to the assembly. It also eases the usage in the anechoic chamber, which would be difficult with only the thin and flexible substrate. Conductive adhesive bonds the CMOS receiver chip to the base PCB, which carries GCPWG traces connecting the IF and LO signals to sockets for coaxial connectors. The aluminum plate and the adhesive used to bond the parts are not shown in Fig. 4.24. Wire bonds provide the connection between the chip and the low frequency signals, i.e., LO, IF and DC. Two 100 nF capacitors stabilize the supply voltage. As described in Section 3.5, a short differential line on the chip surface bypasses the BBA. The glue-on transition described in Section 3.4 connects the RF

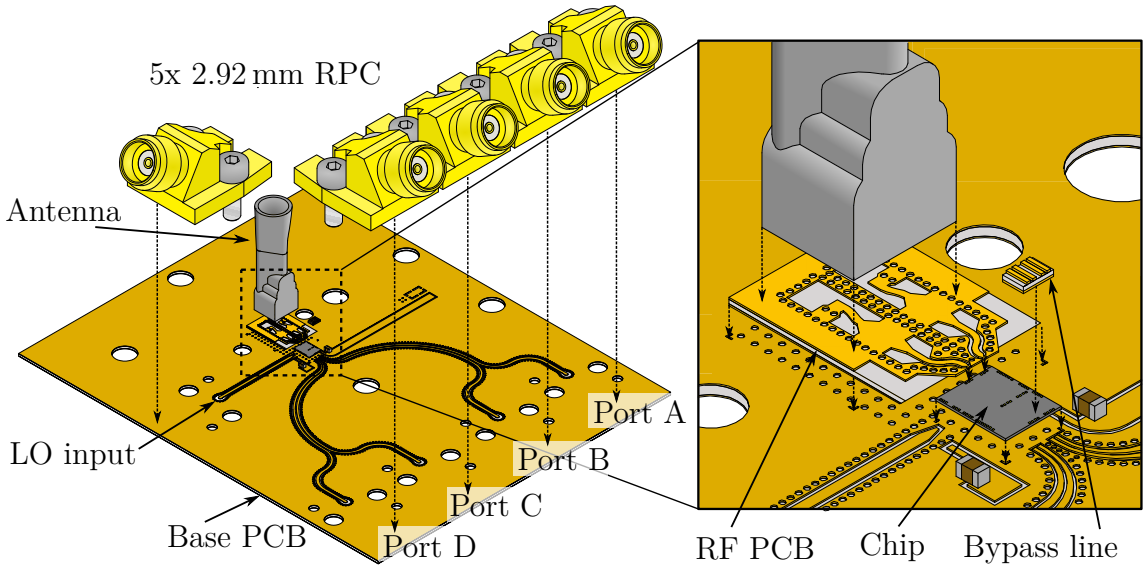



Figure 4.24: Exploded 3D view of the active single-element receiver, showing details of the antenna base and chip. Not shown is the aluminum plate underneath the base PCB with tapped holes and alignment pins.

inputs of the chip to the RF PCB made of *RO4350B*. The RF PCB is attached to the base PCB with conductive adhesive. It comprises the footprints of the single-ended waveguide transitions for the 3D printed antenna.

The via grids under the chip and the RF PCB prevent the dispensed adhesive from squeezing out and creating potential short circuits. In addition, the vias under the chip serve as a thermal path to conduct the heat generated by the chip to the aluminum plate on the backside.

Figure 4.25 details the manufacturing process of the realized active receiver. Figure 4.25a depicts the RF PCB ready to be bonded to the chip with the glue-on transition. Figure 4.25b shows the chip in its intended position on the base PCB. Wire bonds electrically connect the chip to the PCB. The bypass line on top of the chip connects the mixer output directly to the PCB. At this stage of the manufacturing process, the RF inputs of the chip are exposed and can be tested with microprobes to perform measurements on the chip. This allows testing of the bonded connections and the chip integration itself. For the next step, it is important that the lines of the RF PCB match the RF input pads of the chip before the PCB is glued in place. Then the conductive adhesive electrically connects the chip and the lines of the RF PCB, as shown in Fig. 4.25c. Finally, Fig. 4.25d shows the complete active receiver with the antenna on the RF PCB and also provides a detailed view inside the antenna

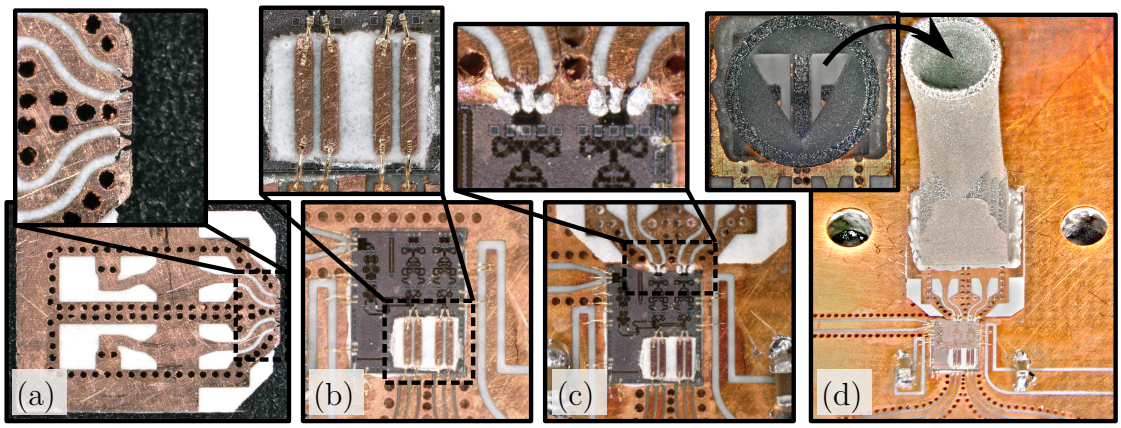



Figure 4.25: Realization of the active single-element receiver. (a) RF PCB with transition footprint and copper stubs prepared for glue-on interconnect to the chip, (b) chip mounted on the base PCB with bypass line and wire bonds, (c) RF PCB mounted on the base PCB and glue-on interconnect established, (d) fully assembled board with detailed view into the antenna showing the precise placement of the ridges.

to inspect the placement of the ridges. The conductive adhesive cures thermally at 150 °C according to the manufacturer's specifications. This puts thermal stress on all the components on the board. However, compared to a regular soldering process at about 230 °C, the temperature is moderate. And actually, the thermal stress did not lead to any defects in the completed receiver.

### 4.2.2 Thermal Analysis

Thermal design limits are not dictated by the chip, as modern CMOS devices can easily operate at junction temperatures above 150 °C. However, in terms of the receiver noise figure, the junction temperature is a critical factor and should be kept as low as possible.

According to the specification, the chip consumes 300 mW of DC power (375 mA at 800 mV). To evaluate the design thermally, a thermal simulation of the chip mounted on the PCB is performed. Since all the active components of the chip are near its top surface, the simulation model places the heat source there. The heat generated by the chip passes through the silicon base of the chip and the conductive adhesive to the top layer of the base PCB. The adhesive has a thermal conductivity of 1.6 $\frac{\mathrm{W}}{\mathrm{m\,K}}$ according to the manufacturer (see Footnote 6) and is modeled as a 50 µm thick homogeneous layer. To simplify the simulation, the top copper layer of the base PCB is omitted except

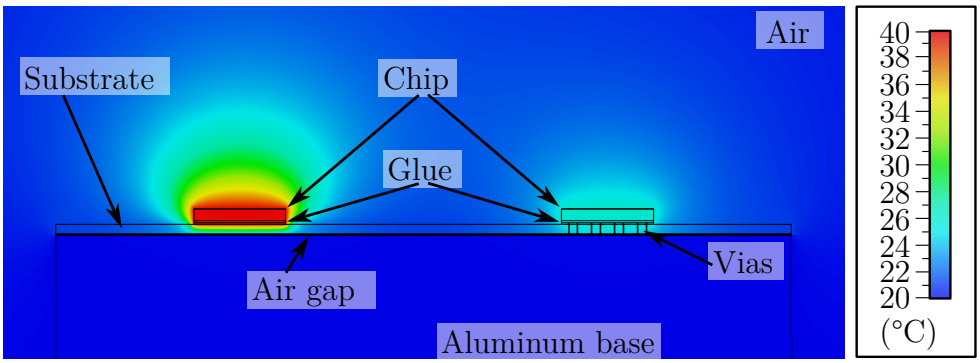



Figure 4.26: Thermal simulation of the receiver chip, which generates 300 mW of heat. Left without thermal vias and right with thermal vias.

under the chip. In this way, the results are a worst case estimate because the LO, DC, and RF copper traces on the top layer help dissipate the heat. After the top layer, the heat passes through the substrate, followed by the bottom copper layer. Finally, the large solid aluminum plate acts as a heat sink. In the simulation, the back of this plate is kept at a constant temperature of 20 °C. In practice, the surfaces of the aluminum plate and the PCB do not mate perfectly. Curvatures in the PCB, deformation of the aluminum plate, and dust between the surfaces result in air gaps between the two. To account for this, the simulation includes a continuous air gap of 10 µm between the PCB and the aluminum plate. Figure 4.26 displays the temperature distribution within the model cross section with and without thermal vias under the chip. The vias have a diameter of 200 µm and a wall thickness of 10 µm. They are arranged in a 4x5 grid with 500 µm spacing in $x$ and $y$ directions. Without thermal vias, the chip heats up to a maximum temperature of 40 °C. The proposed via arrangement reduces the maximum temperature to 26 °C. This simulation proves that thermal management is not critical for the single-element receiver.

Considering that the realized chips consume only about 90 mA (see Section 3.5), the expected temperatures are even lower. Reducing the power in simulation to 72 mW, the chip reaches only 25 °C without vias and 21.5 °C with thermal vias.

In the single-element receiver, only a thin PCB separates the chip from the aluminum plate. In the array configuration, not only are there more chips, but the base PCB is also thicker due to the integrated power combining network. Consequently, the thermal behavior must be analyzed separately for each configuration.

### 4.2.3 Measurement Setup

The receiver board is measured in the anechoic chamber to assess its radiation characteristics. Compared to the passive antenna measurements in Section 4.1.4, the active receiver includes a frequency conversion step. Therefore, the measurement setup in Fig. 4.27 is used. The VNA available in the anechoic chamber can only generate frequencies up to 24 GHz. To scan the W-band at the frequency $f_0$, the VNA generates an RF signal of $f_0/6$ at Port 1. This signal is thus in the range from 12.5 GHz to 18.3 GHz. It passes through a rotary joint and enters a frequency multiplier. The probe antenna radiates at the desired frequency. The active receiver on the RX side converts it down to IF. The quadrupler in the LO path of the on-chip mixer is fed by an external frequency source at 18.5 GHz with an adequate power level. The resulting $\mathrm{IF}_1$ just after the chip is between 1 GHz and 36 GHz. Since the VNA can only receive signals up to 24 GHz, a harmonic mixer operating on the third LO harmonic converts $\mathrm{IF}_1$ to a fixed $\mathrm{IF}_2$ frequency of 100 MHz. The VNA provides the required $\mathrm{LO}_2$ signal, which is related to $f_0$ through

$$f_{\mathrm{LO2}} = \frac{f_0 - 74\,\mathrm{GHz} + 100\,\mathrm{MHz}}{3}. \tag{4.6}$$

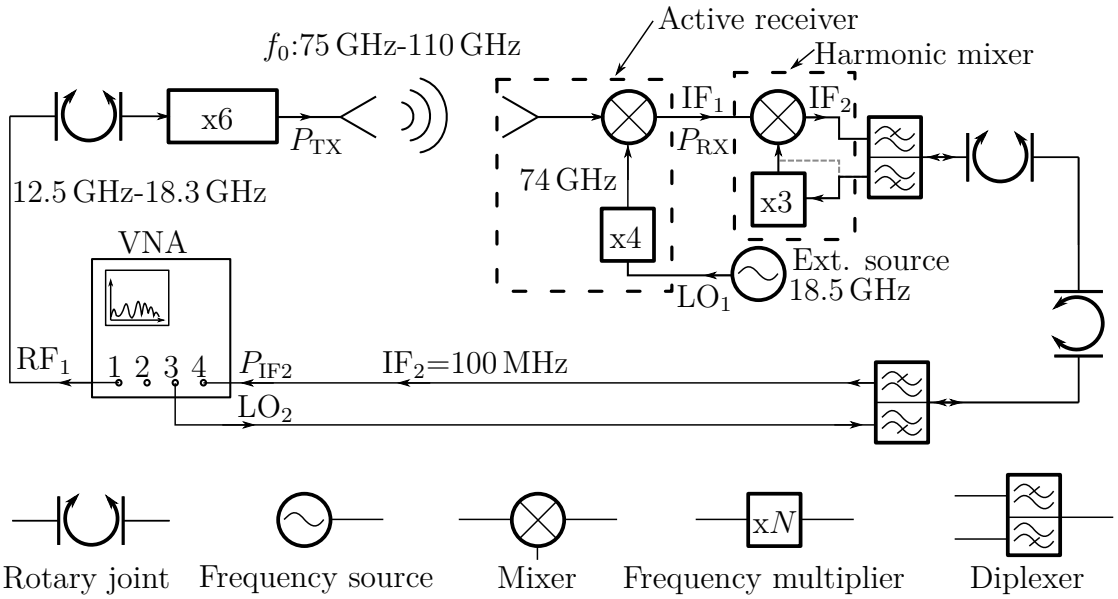



Figure 4.27: Block diagram of the measurement setup for the active single-element receiver. Arrows indicate direction of signal propagation.

With $f_0$ varying from 75 GHz to 110 GHz, $f_{\mathrm{LO2}}$ ranges from 0.367 GHz to 12.03 GHz. Diplexers combine and separate $\mathrm{LO}_2$ and $\mathrm{IF}_2$ before and after the rotary joints of the right positioner. However, the available diplexers have a corner frequency of 1 GHz and cannot separate the 100 MHz IF from the LO2 at 367 MHz. So the W-band is split into two measurements. To capture the first part from 75 GHz to 89 GHz, the harmonic mixer operates in the fundamental mode with an $\mathrm{LO}_2$ frequency from 1.1 GHz to 15.1 GHz. For the rest of the W-band, the mixer switches to the third harmonic mode with an $\mathrm{LO}_2$ frequency from 5.03 GHz to 12.03 GHz. The frequency tripler in Fig. 4.27 is for illustrative purposes only. In practice, the mixer operates on the fundamental and the third harmonic with sufficient performance, and the wiring remains the same for both measurements. The corner frequency of 89 GHz is arbitrary and has no influence on the measurement results.

The main difference from the previous setup is that only the relative magnitude of the transmission coefficient between the probe and the AUT can be obtained. A total of four independent but coherent sources are required to determine the transmission phase. This is because both the transmit and receive signals must be downconverted to 100 MHz to calculate the complex ratio that yields the desired phase information. The VNA provides only two independent frequency sources. Phase-locked external sources do not provide the phase stability required to measure meaningful complex transfer coefficients.

However, the axial ratio can also be obtained from magnitude measurements. Four measurements with a linearly polarized probe antenna set to 0°, 45°, 90°, and 135° allow to reconstruct the polarization ellipse, whose minor and major axes are directly related to the axial ratio. In this setup, the quite compact active receiver on the receiving side replaces the extender module from the previous measurement setup, so that the azimuth axis coincides with the phase center of the AUT. This eliminates the need for offset correction of the measurement data.

In order to calculate the realized conversion gain $G_{\mathrm{convrx}}$ of the active receiver, first the TX power $P_{\mathrm{TX}}$ from is measured 75 GHz to 110 GHz with a power meter at the output of the extender module. Next, a 1 GHz to 35 GHz signal with a defined power $P_{\mathrm{test}}$ is injected into the RF input of the harmonic mixer ($\mathrm{IF}_1$) and measured at the VNA as $P_{\mathrm{IF2,test}}$. Knowing these two powers, the output power $P_{\mathrm{RX}}$ of the active

receiver can be calculated for any measured $P_{\mathrm{IF2}}$ at the $\mathrm{IF}_2$ input of the VNA as

$$P_{\mathrm{RX,dB}} = P_{\mathrm{IF2,dB}} - P_{\mathrm{IF2,test,dB}} + P_{\mathrm{test,dB}}. \tag{4.7}$$

The resulting realized conversion gain of the active receiver calculates to

$$G_{\mathrm{conv,RX,dB}} = P_{\mathrm{RX,dB}} - P_{\mathrm{TX,dB}} - G_{\mathrm{TX,dB}} + \mathrm{FSL_{dB}}, \tag{4.8}$$

where $G_{\mathrm{TX}}$ is the gain of the TX antenna and FSL is the free space loss for the distance between the two antennas. The correction factors and power transfer ratios are frequency dependent.

### 4.2.4 Measurement Results

During the antenna measurements, an absorber with a hole for the antenna covers the receiver as shown in Fig. 4.28. This is necessary to reduce coupling between the antenna and other metal surfaces or circuitry to avoid axial ratio and gain degradation. Underneath the absorber, a removable plastic cover protects the mechanically sensitive bond wires.

The receiver board provides four coaxial output ports, i.e., one differential pair for each polarization. The channels have to be measured one at a time, the others being terminated with $50\,\Omega$ loads. The following measurements are taken from Port A

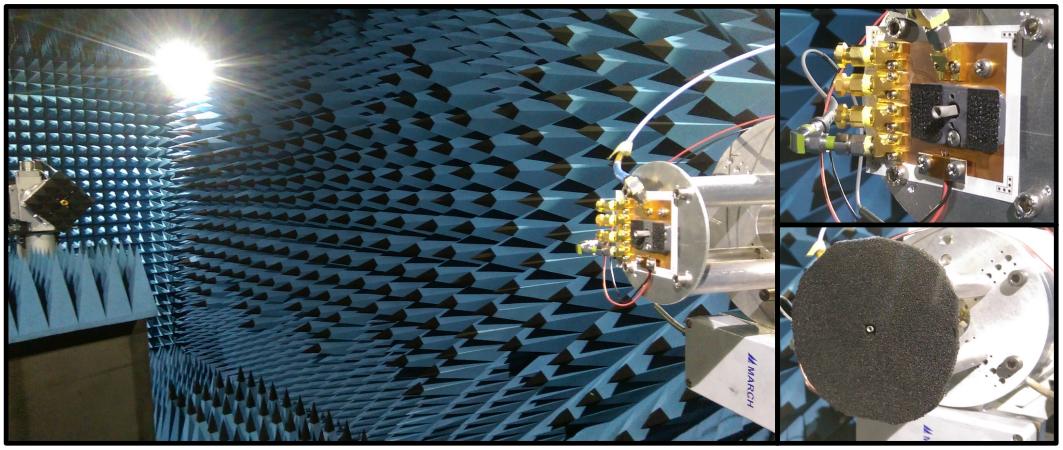


Figure 4.28: Active single-element receiver prepared for the antenna measurements in the anechoic chamber. The board is covered with absorber during the measurements.

(see Fig. 4.24), which corresponds to LHCP. An LO power of 5 dBm drives the chip's quadrupler in all measurements and the DC supply voltage is 800 mV.

Figure 4.29 shows the axial ratio in the main lobe direction $\theta = 0°$ for $\phi = 0°$. The measurement is repeated with $\phi = 90°$, which should give the same result. Both measured curves agree well, indicating a negligible influence of the antenna rotation on the measured polarization characteristics. This confirms the measurement setup. For reference, Fig. 4.29 also includes the simulated axial ratio. In the low frequency range up to 88 GHz the measurements agree well with the simulation. Around 90 GHz larger deviations are observed. However, the measured axial ratio remains below 3 dB, resulting in a very high cross polar discrimination. At 103 GHz the measured axial ratio rises steeply. One explanation for this behavior is frequency selective coupling with the uncovered metal parts behind the antenna. Since an exact modeling including the chip and the mounting situation in the chamber is hardly possible, the simulation shows only the passive subsystem from Section 4.1. This also explains some differences between measurements and simulation for the following measurements.

The conversion gain of the active receiver is measured as described above. The measured data are corrected in a post-processing step. Figure 4.30 shows the resulting conversion gain over frequency in the main lobe direction. For comparison, the sum of the measured antenna gain in the main lobe direction from Section 4.1.4 and the measured conversion gain of the chip with the bypass line from Section 3.5.2 is displayed.

The measurement results prove the successful integration of chip and antenna on the PCB. Compared to the sum of the cascaded measurement data of the subsystems, the

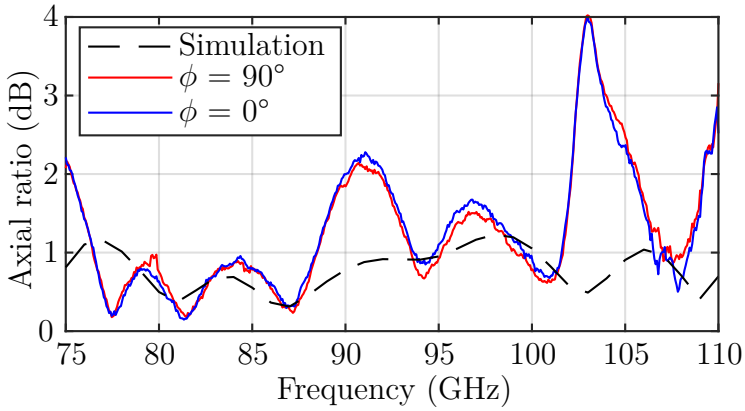



Figure 4.29: Axial ratio in the main lobe direction measured for $\phi = 0°$ and $\phi = 90°$. The simulation data represent the passive frontend.

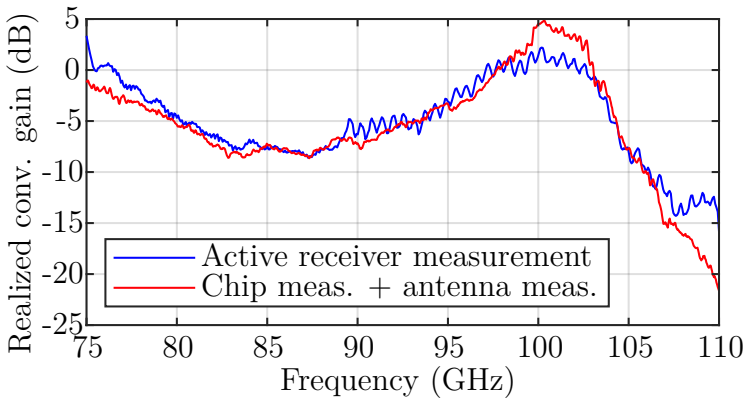



Figure 4.30: Realized conversion gain of the active receiver in the main lobe direction for a supply voltage of 800 mV and an LO drive of 5 dBm. Comparison between the active receiver (blue) and the cascaded subsystems from Section 4.1.4 and Section 3.5.2 (red).

active receiver performs similarly. Both differ by approximately 3 dB around 100 GHz at the gain peak. Larger differences appear toward 110 GHz, which may be related to manufacturing tolerances of individual components as well as coupling effects with the mounting brackets.

Full azimuth scans of the measured far-field properties at selected frequencies are shown in Fig. 4.31. To ease comparison, the conversion gain is normalized. Apart from the band edges, the frequencies are chosen as follows: minimum (87 GHz), intermediate (95 GHz), and maximum (100 GHz) conversion gain, and maximum axial ratio from Fig. 4.29 (103 GHz).

The shape of the radiation pattern agrees well with the simulated horn characteristic at all frequencies. Regarding the axial ratio, the maximum deviation occurs at 103 GHz. The passive antenna measurements from Fig. 4.17 show no such deviations around 103 GHz. So they must be the result of the combined components. For the other measurements at 87 GHz, 95 GHz, and 100 GHz, the axial ratio closely matches the predictions in the angular range of interest. At 110 GHz the noise level increases due to the reduced conversion gain of the chip (see Fig. 3.39).

The integration of the previously presented components into a functional system is successful. Over a wide frequency range, the far-field characteristics of the active receiver match the predicted performance. The measured conversion gain is also consistent with the theoretical cascading of the individual components. Only minor deviations in the axial ratio are observed at some frequencies.

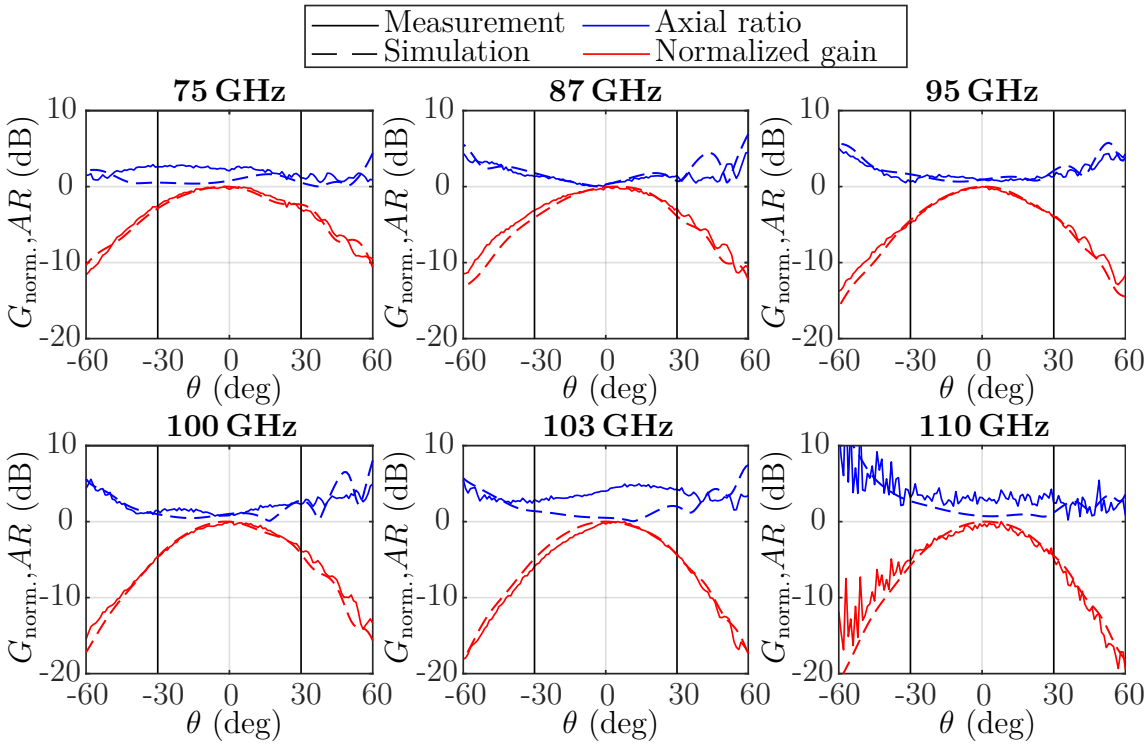



Figure 4.31: Measured axial ratio and normalized gain of the active receiver compared to the simulated characteristics of the passive frontend for $\phi = 0°$. Vertical black lines indicate the angular range of interest.

## 4.3 Active Array Receiver

To demonstrate the feasibility of an active array receiver at W-band, a 2x2 element array is developed using the antennas for Scenario 2. Chip and antenna integration follows the single-element active receiver design. Three major complexities are added by the array approach:

1. Defining the array dimensions, i.e., the horizontal and vertical array spacing.
2. Integration of the combining network, considering antenna and chip placement.
3. LO distribution, including the ability to shift the LO phases individually.

### 4.3.1 Array Spacing

The analysis of planar arrays excited with equal amplitudes with $M$ elements in $x$-direction and $N$ elements in $y$-direction is based on the array factor $AF$ [24] defined as

$$AF(\theta,\phi) = \left(\frac{\sin(\frac{M\psi_x}{2})}{\sin(\frac{\psi_x}{2})}\right) \cdot \left(\frac{\sin(\frac{N\psi_y}{2})}{\sin(\frac{\psi_y}{2})}\right). \tag{4.9}$$

Here, $\psi_x$ and $\psi_y$ are

$$\psi_x = kd_x \sin\theta\cos\phi + \beta_x \tag{4.10}$$

and

$$\psi_y = kd_y \sin\theta\sin\phi + \beta_y \tag{4.11}$$

with the wavenumber

$$k = \frac{2\pi}{\lambda}. \tag{4.12}$$

$\beta_x$ and $\beta_y$ are the excitation phase differences in the $x$ and $y$ directions, respectively.

However, the radiation pattern of an array obtained by multiplying the array factor and the radiation pattern of a single element neglects the coupling between the elements. The horn antennas presented in this work are highly directional and have low coupling coefficients. To quantify this coupling, nine antennas, designed for Scenario 2, are arranged in a 3x3 grid in the simulation. Figure 4.32 shows the resulting transmission coefficients from the central element to the adjacent ones. They all remain below $-37\,\mathrm{dB}$. There are groups of coupling coefficients with similar behavior over frequency.

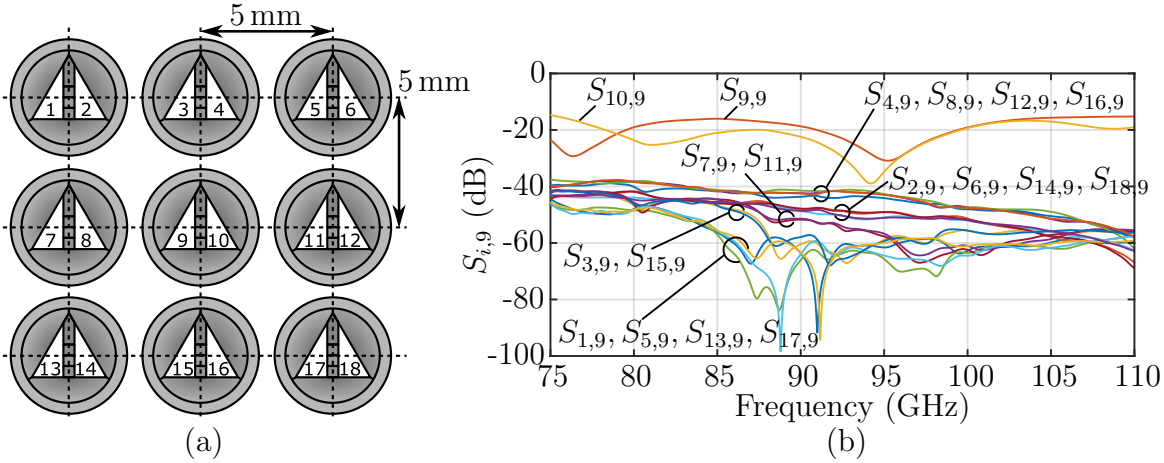



Figure 4.32: (a) Array of nine elements with port numbering for each antenna with its two polarizations. (b) Simulated scattering parameters with respect to the input ports of the antennas. Only Port 9 is fed and the transmission to all other ports is observed.

These groups are formed by antennas with the same polarization and distance to the central array element, e.g., Port 1 and Port 13. Only the input reflection at Port 9 $S_{9,9}$ and the coupling to Port 10 $S_{10,9}$ show higher values compared to the remaining coefficients. However, these show the single element characteristics which are dominated by the polarizer. The coupling between the antennas is small enough to assume that the overall radiation pattern is well approximated by the product of the single element radiation pattern and the array factor.

The main lobe in the array configuration occurs at specific $\theta$ and $\phi$ angles for which $\psi_x = 0$ and $\psi_y = 0$. Thus, by adjusting $\beta_x$ and $\beta_y$ the direction of the main lobe in $\theta$ and $\phi$ is varied. Other maxima, called grating lobes, occur when $\psi_x = n \cdot 2\pi$ and $\psi_y = m \cdot 2\pi$, where $n$ and $m$ are integers.

For most applications, the grating lobes are fully suppressed to prevent power from being radiated in directions other than the current target. This is achieved regardless of scan angle and number of elements when the element spacing is less than half the free space wavelength. In W-band, this corresponds to an element spacing of less than 1.36 mm center-to-center. A standard W-band waveguide is 2.54 mm by 1.27 mm. In conjunction with an antenna, the aperture size is even larger. Therefore, conventional horn antennas cannot be used to build planar arrays without grating lobes. Dielectric filled antennas shrink the physical dimensions while maintaining the electrical size required for operation above the cutoff [86, 87], allowing for grating lobe

free arrays. However, at W-band the antenna dimensions are already challenging in terms of accuracy, and further downscaling leads to major manufacturing difficulties.

The array developed in this work does not have to cover the whole hemisphere, but only an angular section (see Fig. 3.2). To prevent grating lobes from appearing in the angular range of interest, the spacing constraint is loosened considerably. For Scenario 2 no grating lobes should appear within $\pm 30°$. This corresponds to an element spacing of about 2.7 mm. With the developed antennas even this larger spacing is not achievable.

Therefore, grating lobes are accepted in this work. Regarding the whole communication system, the presence of grating lobes leads to a reduced power in the desired main lobe. In addition, two users could possibly be addressed at the same time. However, the latter could be easily solved at the protocol level.

To minimize the effect of grating lobes, the spacing must be as small as possible. The W-band rectangular waveguide sections of the array receiver are 2.54 mm wide and taper to a circular aperture of 3.5 mm diameter. With a metal wall thickness of 0.4 mm, the outer diameter of the antenna is 4.3 mm. This is the minimum possible pitch. However, for reliable manufacturing, a certain distance is required for the antenna placement. Here a distance of 700 µm between the antenna elements is used. The resulting element spacing is 5 mm.

When designing broadband arrays, beam squint must be considered. If the phase shifts $\beta_x$ and $\beta_y$ used to control the main beam are constant over frequency, the resulting direction is frequency dependent. Figure 4.33 demonstrates this effect for a linear array with three and ten elements. A constant phase shift of 97° between the elements directs the main beam in both cases toward $-10°$ at 92.5 GHz. At 75 GHz and 110 GHz, for instance, the pointing direction changes to $-12.5°$ and $-8.5°$, respectively. Larger steering angles as well as larger element spacing increase the beam-squinting effect.

In general, higher element counts in an array configuration result in a narrower main lobe. In combination with beam squinting, this can lead to problematic radiation characteristics. Figure 4.33 shows that for ten elements at $-12.5°$ the array factor is zero at 110 GHz, where there is a maximum at 75 GHz.

No beam squinting occurs when the beam steering is realized with a true time delay instead of a constant phase shift between the array elements. In this way, the main beam direction is independent of frequency. However, in this work, the down-converter chip includes phase shifters. Thus, beam squinting is accepted for the array proof

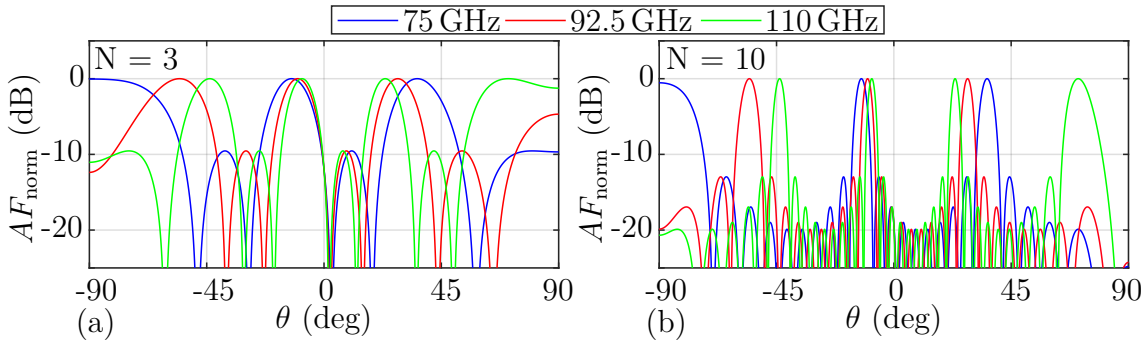



Figure 4.33: Normalized array factor for a linear array with a spacing of 5 mm and $\beta_x = 97°$ (main lobe at $-10°$). (a) Three elements, (b) ten elements.

of concept. For further work, a true time delay or hybrid approach [88] should be considered to minimize the effects of beam squinting. Broadband true time delay phase shifters have been demonstrated in [89–91]. The fact that they are designed in CMOS technology allows integration into a single chip solution including digital parts. However, unlike the phase shifters on the current down-converter chip, the true time delay element must be placed in the signal path either on the RF side or on the IF side of the mixer. In both cases, it must cover the entire signal bandwidth.

### 4.3.2 LO Distribution

A single LO source powers all four receiver chips in the array. Therefore, the LO signal fed to the array board must be divided by three 1:2 power dividers. A divider with only one decoupling resistor is sufficient, as the required frequency range is narrow around 18.5 GHz. Figure 4.34 shows the simulation model of the power divider, including the geometry of the 100 Ω decoupling resistor. The 50 Ω common port is implemented as a GCPWG with a line width of 0.36 mm and, on the top layer, a gap of 0.15 mm to ground. The PCB is *RO4003C* with a height of 200 µm and has a full copper plane on the backside. After a straight section, the line splits into two $w_{\text{narrow}}$ wide and $l_{\text{narrow}}$ long lines, which enclose a grounded patch and end in a 100 Ω resistor. Finally, a short taper restores the original GCPWG line width, connecting the 50 Ω output ports. The line impedance and the length of the high-impedance line section are optimized in a full-wave simulation with initial values taken from the standard Wilkinson approach [41], i.e., 70.7 Ω and $\lambda/4$, respectively. The optimization goal is to minimize the reflection and coupling coefficients while maximizing the transmission from Port 1 to Port 2 and Port 3 at 18.5 GHz. The resulting parameters are $w_{\text{narrow}} = 0.15$ mm and $l_{\text{narrow}} =$

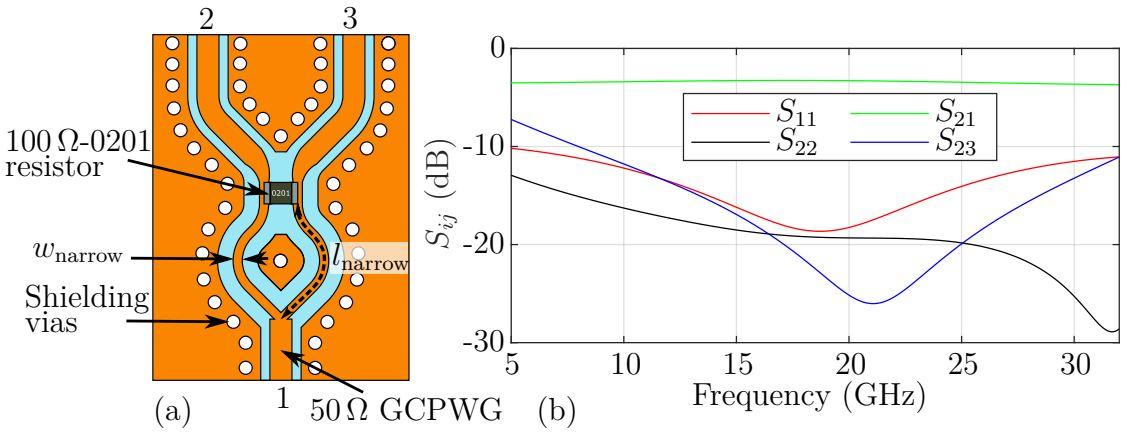



Figure 4.34: (a) Power divider design with port numbering. (b) Simulated scattering parameters of the optimized power divider.

2.28 mm. Both values differ slightly from the theoretical values because the simulation includes effects like the resistor pad as well as the geometry of the resistor itself. The resulting scattering parameters in Fig. 4.34 document the best performance around 18.5 GHz as expected.

For the array demonstration, it is necessary to adjust the LO phase separately for each chip. The CMOS chips include phase shifting capability in the LO path. However, the first generation chips provided for this work do not have sufficient phase shifting range to demonstrate effective beam steering.

As an alternative to digital phase shifting, the LO distribution lines are manually loaded with dielectric material to adjust the phase differences between the chip LO supplies. As a consequence, the routing of the LO distribution has to be done on the top layer. This is feasible because the power combining network is placed on inner layers anyway. Figure 4.35 shows the simulation model of the dielectrically loaded line and the resulting scattering parameters. A 70 µm thick and 10 mm long strip of dielectric with a relative permittivity of 3.4 is placed on the GCPWG line. The resulting matching is better than 20 dB and the transmission is nearly the same as for the unloaded line. Regarding the transmission phase at 18.5 GHz, the loading introduces a phase shift of 35°. Placing segments of different lengths on the LO distribution lines allows very precise phase adjustments. Since the LO signal is quadrupled on the receiver chip, the effective phase shift introduced per millimeter of dielectric is 14 °/mm according to the simulation. In order to have sufficient margin to account for simulation deviations, longer than necessary LO distribution lines are included in the array PCB design.

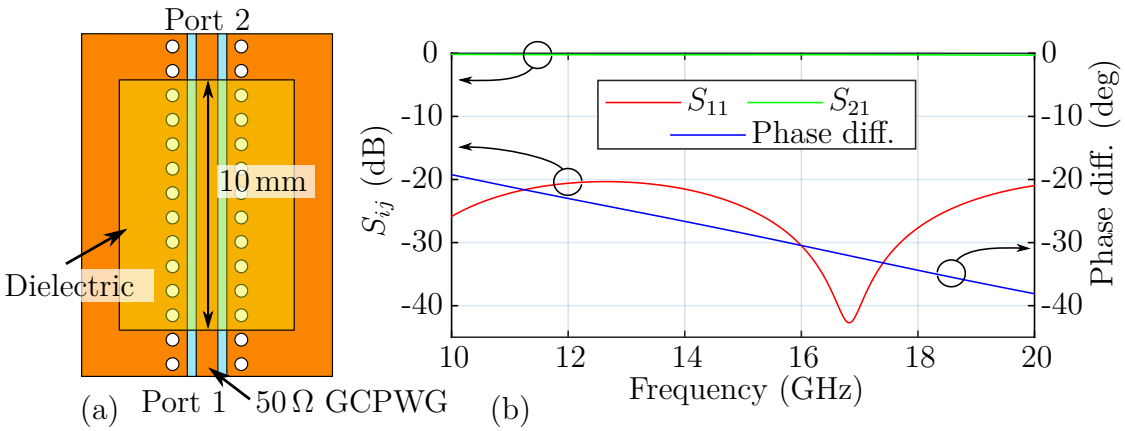



Figure 4.35: (a) Dielectric placed on a GCPWG line. (b) Simulation result of the loaded GCPWG and the phase difference between the loaded and unloaded GCPWG.

### 4.3.3 System Development

Figure 4.36 shows the antenna and chip arrangement developed for the active receiver array. Four antennas are placed in a 5 mm grid on the corresponding transition pads. The latter are implemented on a separate RF PCB made of *RO4350B* with a substrate height of 0.1 mm, which is mounted on the base PCB. This in turn realizes all power combining on its inner layers and provides interfaces for chip integration. For DC, IF

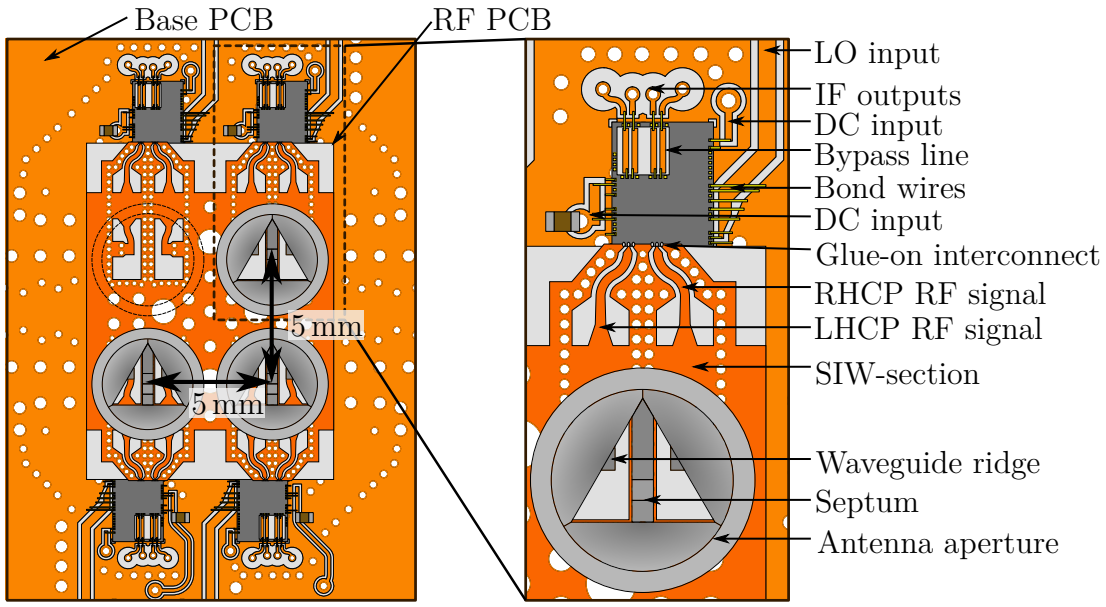



Figure 4.36: Top view of the array layout and detail view of a single element. The antennas are connected to the RF PCB, which is placed on the base PCB.

and LO, bond wires provide the electrical connection between the PCB and the chip. The RHCP and LHCP RF signals from the antennas feed the respective chips above or below the antennas. This concept allows only $N$x2 arrays because chips and antennas share the same side of the base PCB.

Figure 4.37 depicts the relevant sections of the outer and inner layers of the base PCB with the integrated power combining network, which is based on the concept described in Section 3.6.4. A total of six stacked differential power combiners, three for each polarization channel, combine the LHCP and RHCP IF signals. This results in two 4:1 differential combiners. The top layer provides space for the chips and the RF PCB with the four antennas. Via transitions transform the IF output signals of the four chips directly to the inner layers, where they are covered by the mostly intact upper ground plane. The three combiners on the right and on the left combine the RHCP and LHCP, respectively. The two orthogonal crossings ensure a minimum of parasitic coupling between the two polarizations. The symmetry of the transitions developed in Section 3.6 facilitates the realization of equal line lengths from the chip

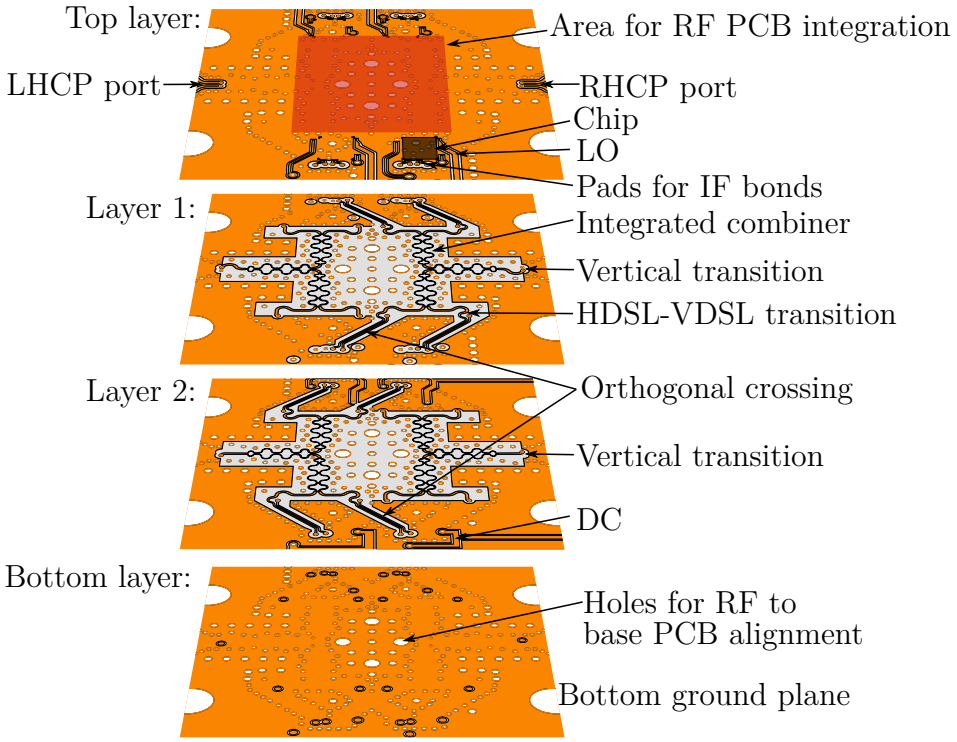



Figure 4.37: Exploded view of the power combining network PCB section without the intermediate prepreg and substrate layers.

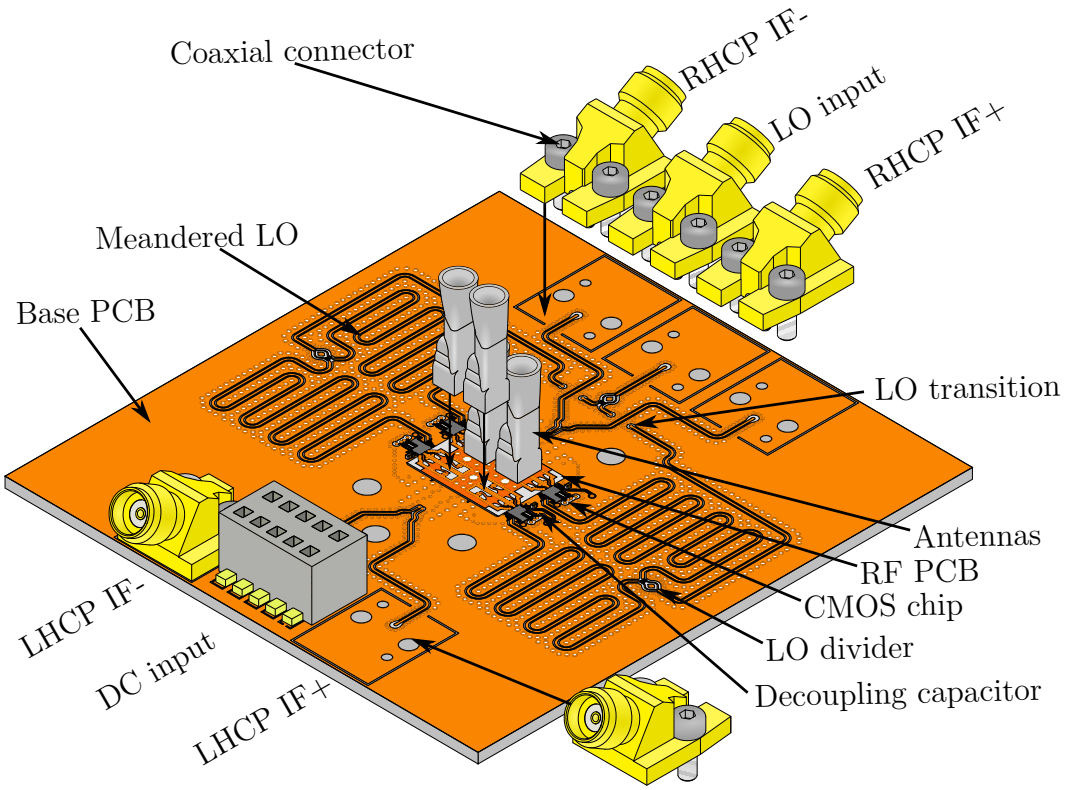



Figure 4.38: Superstructure of the active array receiver with assembled components. The aluminum plate under the PCB is not shown.

to the power combiner. Towards the output, the path length compensated differential transition from Section 3.6 transfers the combined RHCP and LHCP to the top layer. The LO signal line terminates on the top layer close to the chip to allow bond wire connection.

Figure 4.38 displays the complete active receiver. As with the single-element receiver, multiple coaxial connectors interface with the test equipment. The RHCP and LHCP output connectors are on opposite sides of the board. For symmetry, the LO input is placed between the two RHCP outputs. The LO signal is divided twice by 1:2 power dividers on the top layer. Just after the first divider, the LO line crosses the RHCP signals near the connectors. Therefore, a transition routes the LO signal to Layer 2 and back to the top layer after the crossing. In this way, Layer 1 acts as a shield between the LO and IF signals. After the second LO divider, a meander line provides sufficient exposed line length to set each LO phase by dielectric loading. A 10-pin connector with 2.54 mm spacing provides DC power, with two pins for each chip's supply voltage.

The remaining two pins are common ground. Separate access to all four chip supply voltages allows individual control of the chips for calibration purposes.

### 4.3.4 Thermal Analysis

Figure 4.39 depicts the results of the thermal analysis for the array receiver. The simulation model is similar to the one for the single-element receiver, as it uses the same material parameters and includes an air gap between the PCB and the aluminum heat sink. It also omits the top and inner copper layers for simplification. For the array arrangement, however, the simulation includes four chips and antennas in their designated positions. Because of the omitted copper layers, the antennas are not well thermally coupled to the heat sources and do not dissipate much heat. The PCB only includes seven vias under the chip to account for the routing that is done there. Nevertheless, the simulated temperatures are moderate with a maximum of 33°. Considering that the chip consumes less than 100 mW in reality and this simulation assumes the specified 300 mW, even lower temperatures can be expected for the actual setup.

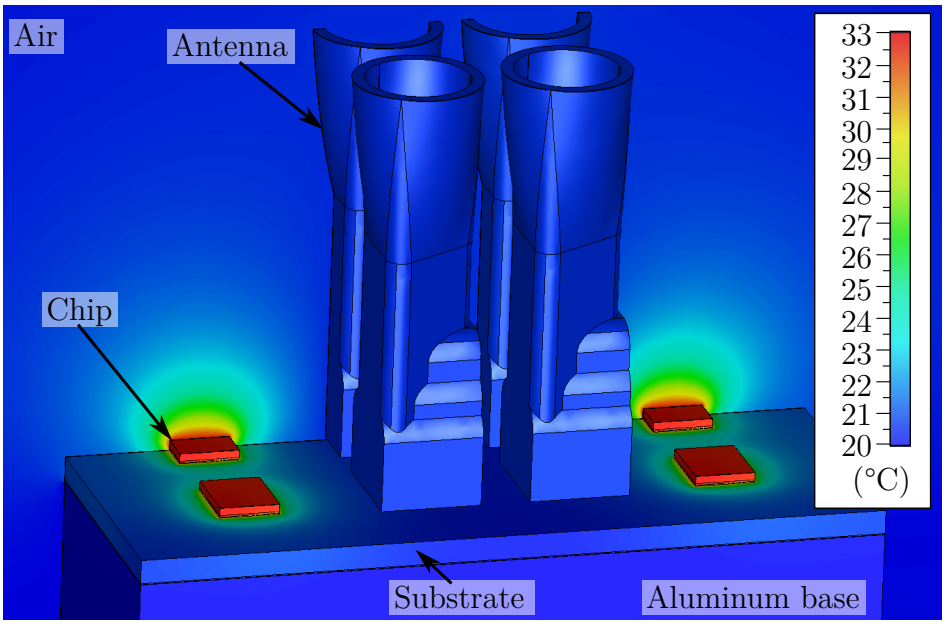



Figure 4.39: Thermal simulation of the array receiver with four chips, each generating 300 mW of heat.

### 4.3.5 Manufacturing and Measurements

Manufacturing of the active receiver begins with the base PCB. Two sheets of *RO4003C* are processed as described in Section 3.6.1 so that the required structures appear on Layer 1 and Layer 2 as shown in Fig. 4.40a-b. These are the carbon paste resistors and the copper structures on the inner layers. Next, the two sheets are laminated with the processed sides facing each other using *RO4450F* prepreg. Finally, holes are drilled and plated, and the outer structures are etched. Back drilling of some of the vias included in the different transitions allows to avoid the processing of blind vias completely. The RF PCB made of *RO4350B* requires less manufacturing effort since it has structures on only one side. However, its outline must be prepared for the glue-on transition as explained in Section 3.4.1. Holes and copper marks ensure precise alignment when attaching the RF PCB to the base PCB. As the chips are glued in

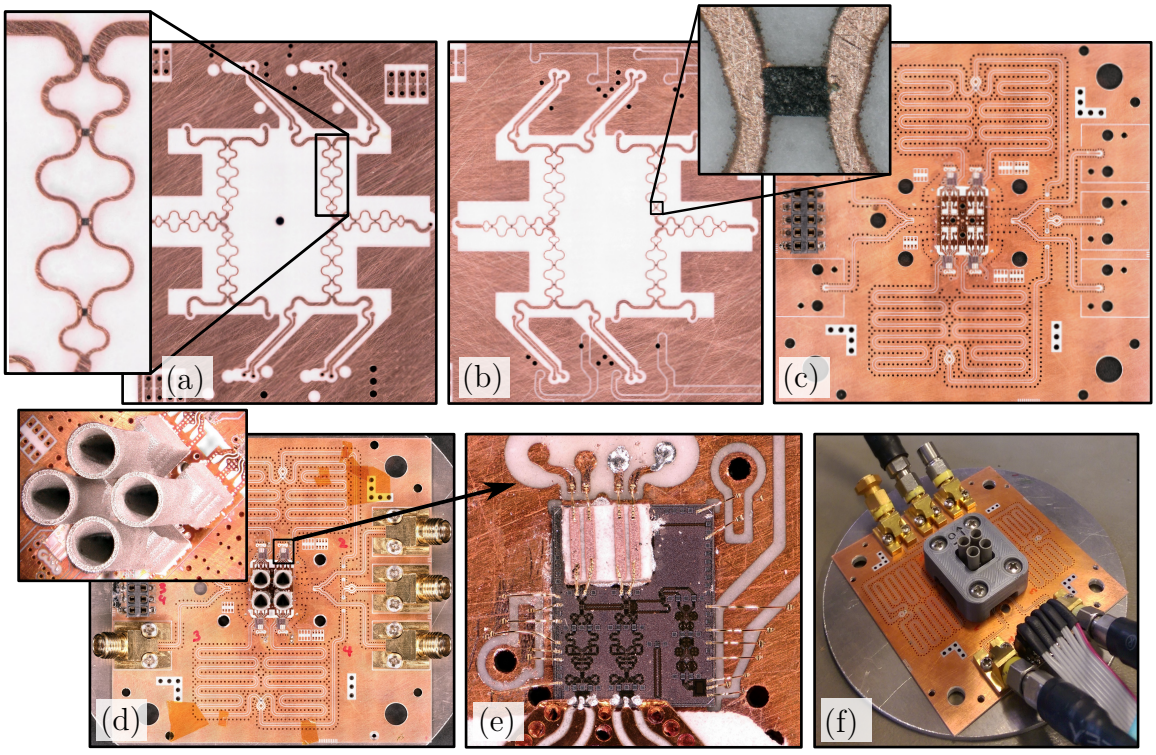



Figure 4.40: Manufacturing of the 2x2 active array receiver. (a) and (b) Inner layers of the base PCB with the power combiners, (c) top view of the base PCB with the chips and RF PCB mounted, (d) complete receiver with detail view of the four antennas, (e) zoom on one of the four chips with bypass line and bond wires, (f) receiver with plastic cover mounted on the circular aluminum plate with RF and DC connectors for measurements.

place, the protruding lines from the glue-on transition must mate with the chip pads. In the next step, the bypass line bridges the defective BBA. Then the glue-on transition and bond interconnects provide the electrical connections from the chip to the PCB. Regular solder joints attach the solderable components, i.e., decoupling capacitors, resistors and the DC connector, to the PCB. Figure 4.40c shows the assembly up to this point. The final step is to glue the antennas onto the PCB stack and mount the coaxial connectors Fig. 4.40d-e. A plastic cover on top of the board protects the delicate bond wires and chips from damage during handling.

The measurements of the receiver array are similar to the measurements of the single-element receiver. Again, phase correct measurements are not possible. However, reconstruction of the polarization ellipse from multiple magnitude measurements provides the polarization characteristics. Also, only one IF port can be measured. The following calibrations and measurements correspond to RHCP IF + (see Fig. 4.38).

Prior to the actual measurements, the array elements must be matched in magnitude and phase. Theoretically, all four signal paths of each polarization affect the magnitude and phase of the received signals in the same way. This is because the signal paths from the antenna to the chip and through the power combiner have the same components and the same line lengths. Only the individual LO phase affects each signal differently. In practice, however, manufacturing tolerances introduce amplitude and phase imbalances between the array elements. By varying the supply voltage of each individual chip, it is possible to adjust the gain for each channel separately. This is the purpose of the controller board shown in Fig. 4.41. It provides four output channels with variable voltage sources and six logic bit outputs on each channel. The latter can drive an

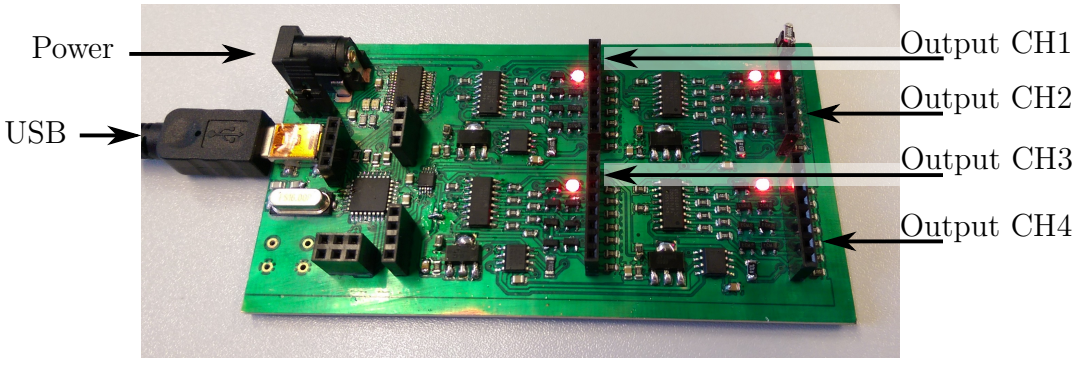



Figure 4.41: Four-channel array controller board. Each provides an eight-pin output connector with ground, variable supply voltage and six logic bits. Red LEDs indicate output status.

Table 4.2: Voltages and currents for the equalized array.

| Channel No. | Voltage | Current |
|---|---|---|
| 1 | 825 mV | 107 mA |
| 2 | 800 mV | 90 mA |
| 3 | 900 mV | 118 mA |
| 4 | 1000 mV | 153 mA |

on-chip 6-bit phase shifter in future chip revisions. By means of a control application running on a PC, the supply voltages of the chips are switched on and off as well as precisely adjusted to specific values.

The measurement setup in the anechoic chamber allows precise magnitude measurements. The magnitudes of the four channels are calibrated by turning on individual channels and adjusting their supply voltages until their measured output magnitudes are equal. Table 4.2 lists the resulting voltages and the current drawn with the LO enabled. With these settings, all four channels are equalized to less than 0.7 dB.

To equalize the phase of the array elements, the measurement setup must be modified as shown in Fig. 4.42. A 14.8 GHz signal supplied by the VNA feeds the W-band extender on the TX side of the chamber. Here, the multiplier generates the 88.8 GHz signal radiated by an antenna. The second VNA source provides the 18.5 GHz LO signal to the receiver chip, which downconverts the received 88.8 GHz signal with the quadrupled LO. The resulting IF signal has the same frequency of 14.8 GHz as the output on Port 1 of the VNA. Thus, the complex quotient of the IF signal and the RF signal can be evaluated. This yields the desired phase difference, which includes the 88.8 GHz transmission path. Only at this specific frequency are phase-correct

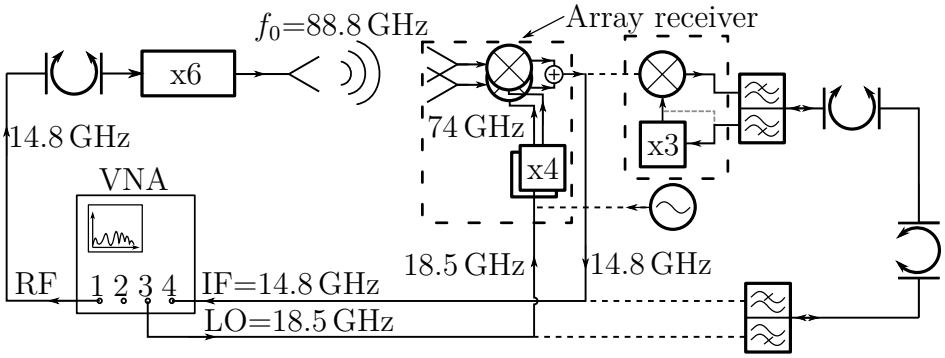



Figure 4.42: Modified measurement setup used to correct and adjust the array element phases. Dashed lines show the original connections for the actual antenna measurements (cf. Fig. 4.27).

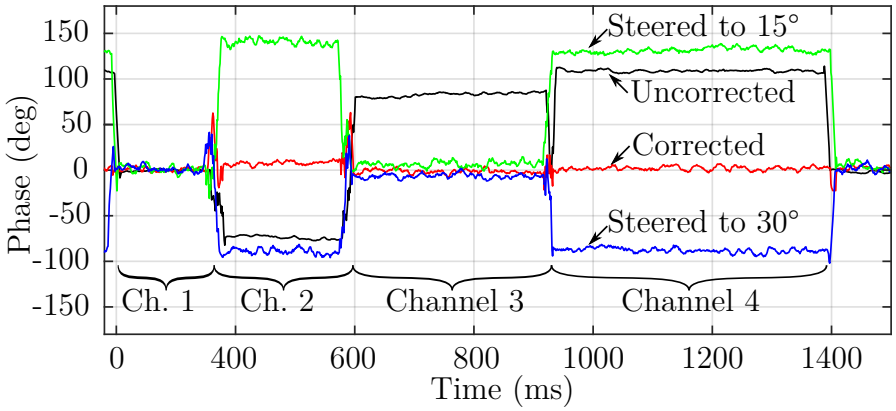



Figure 4.43: Measured phases for the uncorrected, corrected, and steered array configurations. All four measurements are aligned so that channel 1 is at 0°.

measurements possible with the available components. This frequency is in the center of the W-band and the correction of the element phases at this frequency is valid for a certain range around it. If the elements are nearly identical, the calibration is valid for the entire W-band, while manufacturing errors would limit the range.

The phase obtained from the modified setup represents the phase of the transmission coefficient of the entire setup, including the receiver. The entire setup is susceptible to phase drift. Therefore, the phase comparison of the array elements must be performed quickly. To correct the phase, the array controller board sequentially turns on only a single channel for a specified time, i.e., 175 ms, 200 ms, 350 ms, and 450 ms for channels 1 through 4, respectively. This makes it possible to distinguish the different channels in the continuous measurement stream.

Figure 4.43 shows the measured phases for the uncorrected, equalized and steered array. For the uncorrected array, the phases of the individual channels are very different. However, correcting the phases by precisely loading the LO distribution lines with dielectric results in nearly equal phase for all four channels. Zero phase difference of the array elements corresponds to a steering angle of 0°. According to Eq. (4.11), the phase difference of the elements in $y$-direction $\beta_y$ must be 145° to steer the main lobe at 92.5 GHz to $\theta = 15°$ or 280° for a main lobe pointing to $\theta = 30°$. These two cases are also displayed in Fig. 4.43.

The conversion gain measurements are performed as for the single-element receiver. The results in Fig. 4.44 show similar behavior as the sum of the individual chip and antenna measurements. This proves a successful array integration. However, the ab-

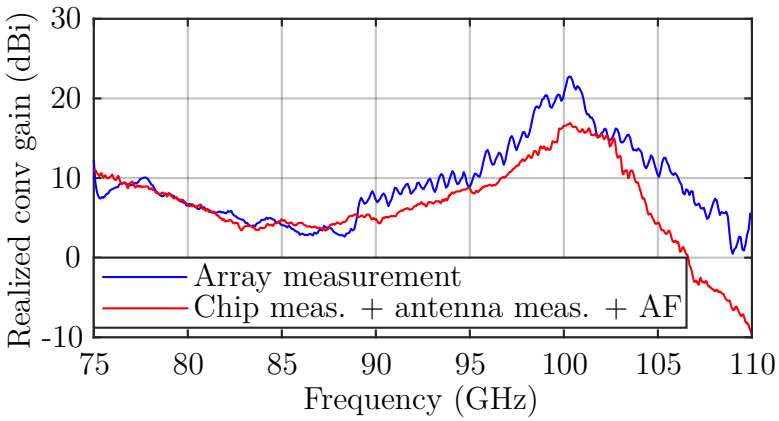



Figure 4.44: Measured conversion gain of the array steered to $\theta = 0°$ compared to the sum of the measured conversion gain of the chip, the passive antenna , and the array factor.

solute gain values obtained from the measurements are subject to inaccuracies due to the long measurement times. A single measurement takes more than an hour. During this time, the output power of the active components involved in the measurement may drift. The measurements for the array shown in this work were performed within three days, and only one power calibration was performed prior to all measurements. The lack of accuracy in the power calibration only affects the conversion gain measurements. The axial ratio calculation is based on relative measurements and is not affected by power drifts. The same is true for the relative gain.

Figure 4.45 shows that the measured axial ratio in the main lobe direction remains below 3 dB over the entire frequency range. As for the single-element receiver, a second orthogonal measurement quantifies the uncertainties. Compared to the simulation,

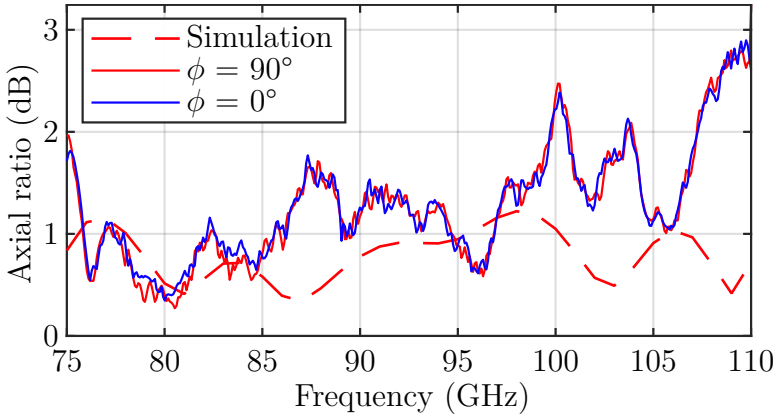



Figure 4.45: Axial ratio in the main lobe direction $\theta = 0°$ measured with all element phases equalized.

slightly higher values are observed, especially in the upper half of the frequency range. For the single-element receiver in Fig. 4.29 a peak up to an axial ratio of 4 dB is measured at 103 GHz. The array receiver, however, shows two peaks at 100 GHz and 104 GHz, both below 2.5 dB. This is due to the fact that in the array configuration, random manufacturing defects of individual elements have only a small effect on the far-field properties due to the contributions of the other elements. In this way, the manufacturing defects of the individual elements in the array partially cancel each other out.

The measurements of the array with all element phases equalized are shown in Fig. 4.46 for different frequencies. The array characteristic with well-defined zeros around the main lobe is measured with good agreement to the simulation. For the axial ratio, the simulation predicts the same value for the array as for the single antenna even at low gain levels. In the measurements, the axial ratio increases strongly at low gain levels. This is due to the fact that at low amplitudes, small interferences become more relevant for the axial ratio. In the simulation, the far-field characteristics are

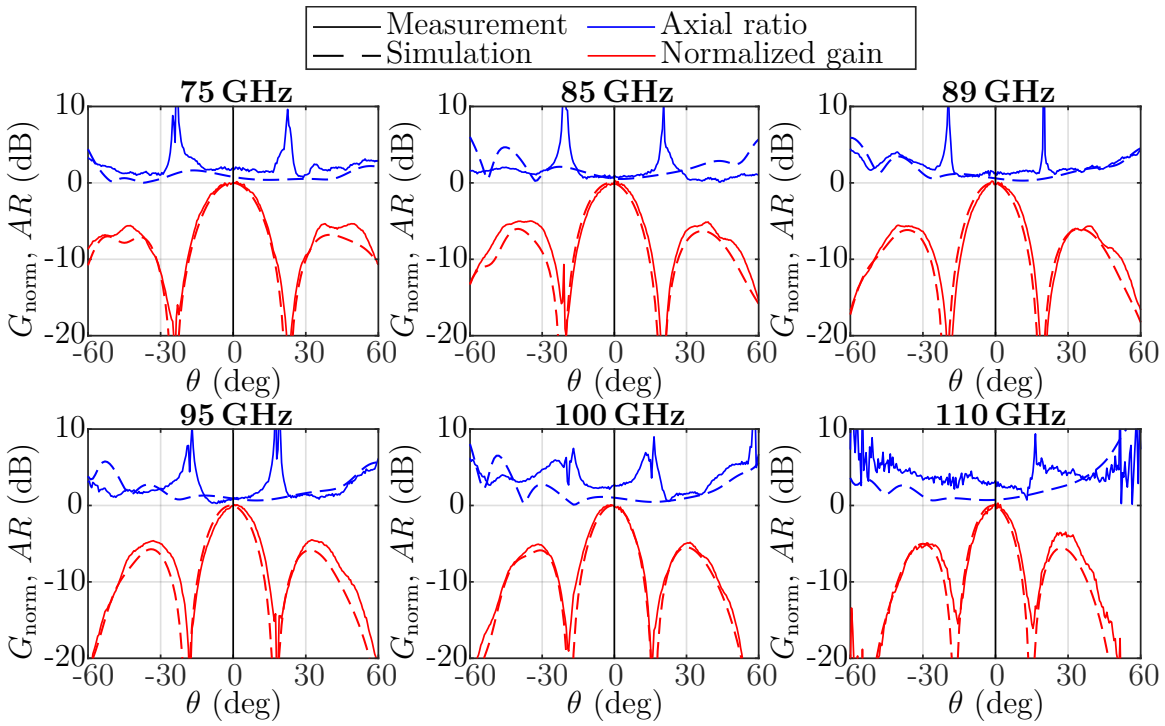



Figure 4.46: Normalized realized conversion gain and axial ratio of the array with calibrated phases on all four elements scanned over $\theta$ with $\phi = 90°$.

simply multiplied by the array factor, resulting in the same axial ratio for the single antenna and the array.

Over the entire W-band, the direction of the main lobe is close to 0°. This means that even though the array is only calibrated at 88.8 GHz, the phase difference between the array elements is nearly constant over the entire frequency range.

Figure 4.47 shows the measured and simulated far-field characteristics of the array, for a steering angle of $\theta = 15°$. Again, measurements and simulation agree well. The axial ratio is slightly different. For the midrange frequencies, i.e., 85 GHz, 89 GHz, and 95 GHz, the axial ratio in the main lobe direction is below 1.5 dB. At higher and lower frequencies it remains below 3 dB. A similar behavior was observed for the main lobe direction of the array directed towards $\theta = 0°$ (see Fig. 4.45). Only at 100 GHz the measured main lobe direction differs slightly from the predicted one. Therefore, at this frequency, small manufacturing or process variations are likely to result an additional phase difference between the elements in the $y$-direction.

The measurements for the main lobe at 30° in Fig. 4.48, are consistent with the simulation. A phase shift of 280° between the array elements in the $y$ direction sets

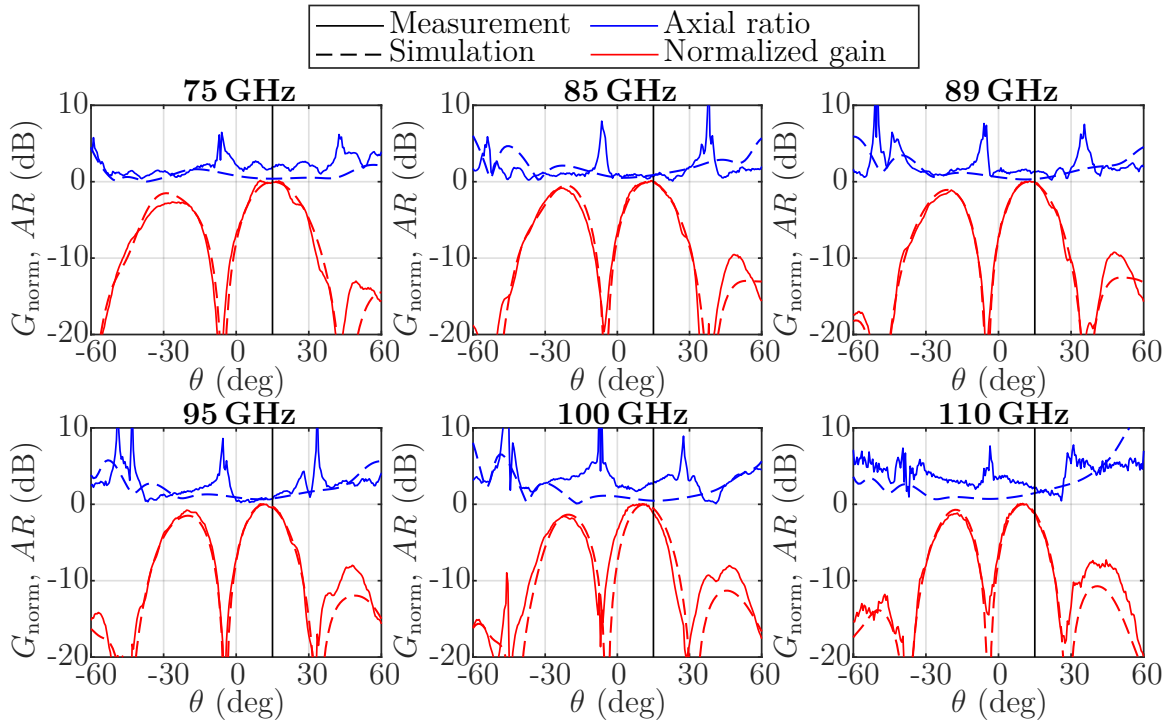



Figure 4.47: Normalized realized conversion gain and axial ratio of the array steered to 15°, scanned over $\theta$ with $\phi = 90°$.

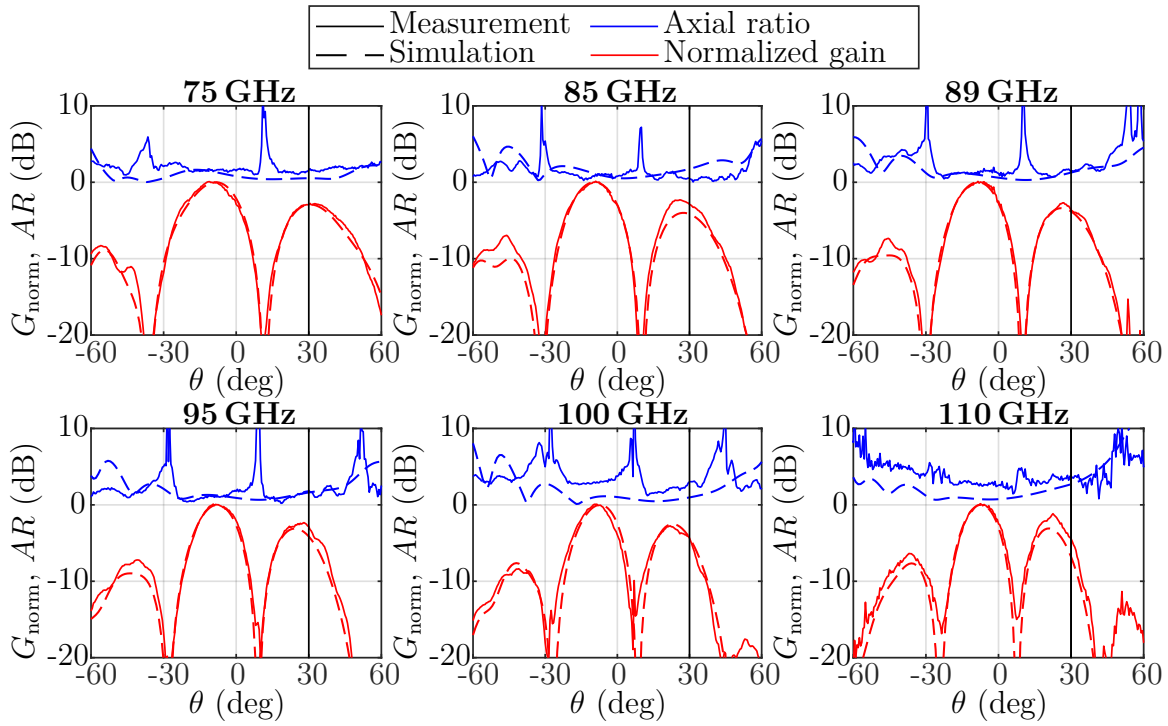



Figure 4.48: Normalized realized conversion gain and axial ratio of the array steered to 30°, scanned over $\theta$ with $\phi = 90°$.

the main lobe direction to 30°. However, the lobe with the largest amplitude occurs at approximately $\theta = -8°$. This is due to the large array spacing chosen in this work, which results in grating lobes in the angular range of interest.

In addition, beam squinting occurs due to the constant phase shift used to steer the main beam. As a result, the main beam points to 30° around the frequency used for calibration, i.e., 88.8 GHz. Higher frequencies tend to point to smaller $\theta$-angles, and lower frequencies to larger $\theta$-angles. Both effects are visible in Fig. 4.48.

For the two steered measurements, Fig. 4.49 gives the axial ratio in the main lobe direction over frequency. For the main lobe at 15°, the measured axial ratio in that direction remains below 2 dB, except for a narrow range around 100 GHz, where the axial ratio measures up to 3 dB. For the main lobe at 30°, the highest axial ratio occurs at 110 GHz with a value of 3.8 dB. However, for frequencies up to 97 GHz it stays below 2 dB. This is close to the simulation and proves the feasibility of an active circular polarized receiver array operating in the W-band.

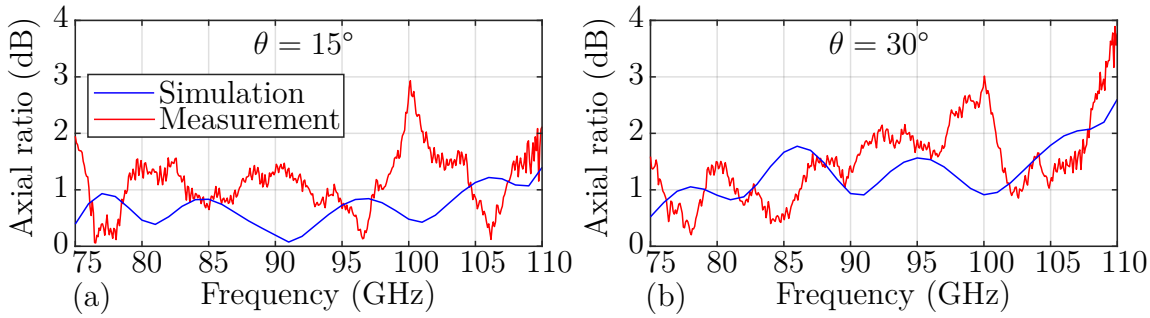



Figure 4.49: Measured and simulated axial ratio in the main lobe direction for the array being steered to (a) 15° and (b) 30°.

### 4.3.6 Scalability Aspects

The array receiver presented here is made up of 2x2 elements. This is the minimum array size to demonstrate a planar array. The array concept of Section 3.6.4 places chips and antennas on the same PCB layer. This allows scaling the array only in one direction, resulting in $N$x2 arrays. However, for such an array, the routing of the power combining network on internal layers becomes more challenging at high element counts. More layers can be used to simplify the routing, but this increases the manufacturing effort and therefore the cost.

Grating lobes in the angular range of interest have been accepted in this work. A reduction of the array spacing reduces the grating lobes. However, only a spacing below 1.36 mm completely suppresses the grating lobes. Realizing such a small spacing in a scalable way would require not only shrinking the horn antennas but also the chips. With the current chip size of 2 mm by 2.5 mm, a grating lobe free and scalable array is not achievable. Using different antenna types and architectures, a spacing close to a quarter wavelength is possible in the W-band [92–94]. However, full W-band coverage with dual polarization remains a challenge.

With the additive manufacturing technique in this work, only single antennas are produced because single-element and array configurations are built with the same antennas. However, the additive manufacturing approach allows to print multiple antennas as a single piece. Since only a minimum wall thickness is required between the antennas, the minimum array spacing is reduced to the aperture diameter. The additional margin between the antennas needed for placement is also eliminated. Thus, for Scenario 2, the minimum spacing in a multi-antenna print is 3.5 mm. This is still not small enough to completely suppress grating lobes in the ±30° angular range used in

Scenario 2. This shows that with air-filled horn antennas, grating lobes must be accepted and possible effects on a communication system must be solved at the protocol level.

For a fully scalable $M$x$N$ planar array, the chip must be placed on the backside side of the PCB to achieve a reasonable array spacing. This requires advanced interconnects to route the RF signals through the multilayer board. Thermal management must also be rethought for such a design. With the chips on the backside, a heat sink cannot be attached directly to the PCB. Thus, there are several challenges to overcome in order to generate a generic scalable array layout.

# Conclusion and Outlook 5

In this work, an active receiver array is developed and characterized in terms of its far-field characteristics. It supports two circular polarizations, covers the entire W-band from 75 GHz to 110 GHz and is capable of beam steering.

The development begins with the individual components required for the array. First, three different horn antennas are designed to meet the requirements of three possible application scenarios. The antenna and the subsequent septum polarizer must be able to split the two received circularly polarized waves into their RHCP and LHCP components with the highest possible cross polar discrimination. Therefore, several different antenna apertures are analyzed. The result is that a circular aperture provides the best performance in terms of axial ratio and gain.

The challenge in the septum polarizer design is the large relative bandwidth of 38 %. To avoid the in-band resonances associated with conventional square and circular waveguides, a triangular waveguide is used. The resulting compact septum polarizer covers more than 38 % of relative bandwidth while maintaining state-of-the-art performance.

For the interface of the waveguide components, i.e., the horn antenna and the septum polarizer, with a printed circuit board, two different transitions are developed. Key aspects in the design are compactness and robustness. Surface mounted vertical broadband transitions in the literature often require a metallic cavity on the backside of the PCB. The transitions developed in this work eliminate the backside cavity while maintaining broadband performance by employing ridges in the waveguide. Transitions with both single-ended and differential ports on the PCB are used to demonstrate this concept.

The down-converter CMOS chip, the central active component in the array, was provided and developed in a separate research project. A large deviation from the expected performance was found in the detailed analysis of the first generation chips

provided. Bridging of some on-chip elements by external circuitry improves the conversion gain to some extent. This allows the chips to be used in an array demonstrator to show basic functionality, while the actual gain values with a fully functional chip would be at least 20 dB higher.

To integrate the chip on the PCB, different high frequency integration methods are developed and compared with conventional methods. The glue-on transition developed provides the best electrical performance. It is robust and allows the chip to be mounted directly on the PCB, resulting in a proper thermal interface.

To combine the differential IF outputs of multiple chips in the range from 1 GHz to 36 GHz, a broadband power combiner is designed. The fully differential 2:1 combiner is enabled by integrated carbon paste resistors that allow two Wilkinson power dividers to be stacked in a multilayer PCB. Multi-section combiners are used to cover the wide bandwidth. For an array setup with more than two elements, multiple combiners must be cascaded. Therefore, the various required transitions and routing concepts, including general component placement, are provided.

Prior to the design of the active receiver, the passive subsystem consisting of antenna, polarizer and waveguide-to-PCB transition is fabricated and analyzed in terms of scattering parameters as well as far-field characteristics. Two different manufacturing approaches for the waveguide part are pursued. The first is a commercial 3D steel printing process. The second creates the waveguide structure in copper by electroplating a 3D printed mold. Antennas fabricated by both processes are measured and compared. It turns out that the commercial process gives slightly better results and is more reproducible. Therefore, the former is used for the active receiver demonstration.

To form a single-element active receiver, the chip is integrated with the antenna on a PCB. Thermal simulations show that no critical temperatures occur for the proposed design. Measurements in an anechoic chamber confirm the successful integration of the down-converter with the antenna. Over a wide frequency range, the axial ratio is within the region predicted by the simulation.

Ultimately, a 2x2 antenna array is constructed using all the components presented. The far-field characteristics of this array are investigated in an anechoic chamber. The measured conversion gain is within the expected range, confirming successful integration. By adjusting the LO phases of the individual elements, the steering of the main lobe is demonstrated. The phase calibration is performed at one frequency only, but is valid for almost the whole W-band. This shows that manufacturing tolerances cause

only minor differences between the elements. The axial ratio is also within the expected range, even when the beam is steered.

Further work on this topic should investigate dielectric filled horn antennas to completely suppress grating lobes. These would have a smaller footprint and could be placed in a tighter grid. With today's advanced manufacturing techniques and materials[17] the dielectric could be 3D printed and then metallized to form the antenna.

On the chip side, a redesign that improves performance would be desirable. This could also include reducing the footprint and integrating true time delay phase shifters in the RF or IF path. This would eliminate the beam squinting caused by the large bandwidth. If the delay for the two channels is individually controllable in the chip, independent beam steering of the two polarizations is possible.

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