

Research paper

Local thermal runaway during surge events in power rectifiers[☆]Ole Jonathan Bergmann^{a,b,*}, Tim Boettcher^a, Hoan Vu^a, Hoc Khiem Trieu^b^a Development, Nexperia Germany GmbH, Stresemannallee 101, 22529 Hamburg, Germany^b Institute of Microsystems Technology, Hamburg University of Technology, Hamburg, Germany

ARTICLE INFO

Keywords:

Surge current (IFSM)
Local thermal runaway
Failure mode
Hole injection
Minority carrier injection

ABSTRACT

This article presents a model for device failure of power rectifiers during surge current events. A possible failure cause of those devices are exceeding surge currents. Therefore, the detailed understanding of the device behaviour under surge conditions and the related failure mode is essential to achieve and maintain a stable device performance. In this work, the IFSM failure mode is investigated in terms of experimental determination of the failure temperature for rectifier diodes. The failure locations of the stressed devices are determined on the chip and partial-electro-thermal simulations are run to model the temperature distribution. The simulated temperature distribution matches with the analysed failure locations. The failure can be explained by local thermal runaway for PN as well as Schottky diodes, if hole injection from the PN junction or the Schottky contact is taken into account.

1. Introduction

Power rectifiers are commonly used as freewheeling diodes in all kinds of switch mode power supplies. Depending on the application, these can be PN junction or Schottky contact based devices. One important property of rectifiers is the ability to withstand surge current events, which commonly occur at power-on of the power supply. This property is verified with the so-called forward surge maximum current (IFSM) test as it is published in all datasheets. This parameter is known to be mainly determined by the device type and the thermal design of the anode contact. In this paper, two Schottky diodes with different die sizes but equal clip bond and two PN diodes with different clip bonds but equal die size are analysed (Table 1). Using temperature dependent IFSM tests, the surge current destruction level and the failure temperature of the investigated devices can be determined. The identified failure locations are compared with electro-thermal simulation results. Because pure thermal modelling of the device thermal impedance cannot explain the observed findings, the transport properties of the devices must be considered as well.

The thermal impedance (Z_{th}) represents a transient thermal resistance such that $Z_{th}(t \gg 0) = R_{th}$ holds and a function of the thermal capacitances and resistances of the different layers of the device. It is linked to the material properties and the geometry of the device. With

the thermal impedance, the junction temperature of a device can be determined as a function of the time dependent pulsed power dissipation, described by the relation:

$$T_j(t) = T_{amb} + Z_{th}(t) \cdot P, \quad (1)$$

where P is the dissipated power, T_j and T_{amb} are the junction and ambient temperature, respectively [1].

Previous analysis of power diodes under surge current conditions were conducted in [2,3]. However, with the introduction of clip-bonded diodes, the thermal and electrical properties have improved significantly compared to wire bonded devices. The clip attach to the die spreads the current over a wider area compared to wire bonded wire bonded devices thus decreasing the current density and increasing the total maximum current. Furthermore, the copper clip facilitates a better thermal connection and a higher thermal capacitance and lower thermal resistance on the top side of the die, lowering the thermal impedance for short pulse durations. Therefore, this paper presents detailed investigations of the surge current capability of power diodes utilizing measurements, finite element method (FEM) as well as technology computer aided design (TCAD) simulations for clip bonded silicon diodes.

[☆] This article is part of a Special issue entitled: 'ESREF 2024' published in Microelectronics Reliability.

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Table 1

Overview of clip shape and die size of investigated devices. The black areas in the clip shapes indicate the dimple, i.e. the part of the clip that is in direct contact with the die.

Device	Clip	Die size
S1		1.85 mm × 1.85 mm
S2		1.7 mm × 1.7 mm
PN1		1 mm × 1 mm
PN2		

2. Measurement results and significance

The measurements to determine the IFSM rating of the device are such that the device is stressed with a series of 50 Hz half-sine wave current pulses with increasing amplitude after each pulse. The reverse characteristic of the device under test (DUT) after each current pulse is monitored to detect failures. If the DUT fails the reverse test, the IFSM level is determined as the last current amplitude which did not cause failure.

Using electrical self-heating during surge tests we were able to determine the IFSM current as a function of junction temperature for Pt-killed PN and PtSi Schottky diodes, such that the failure formation temperature could be extracted through the extrapolation to zero IFSM current. Higher device temperatures during IFSM tests result in lower surge current levels, because less energy must be supplied to the junction to cause failure. Following this principle, the temperature where no external energy, i.e. surge current must be supplied can be deduced by extrapolation. Thus, this temperature yields the failure temperature of the DUT. The devices are then de-capped to locate and characterize the failure.

For both device types, the estimated IFSM failure temperature was as high as 850 °C, as shown in Fig. 1. This is much higher than expected from numerical FEM models, predicting peak temperatures in the range of 500 °C (see Fig. 2).

However, it matches very well to the melting point of PtSi in the Pt-rich regime, where the melting temperature can be as low as 851 °C [4]. The PtSi is present in both investigated devices at the semiconductor-metal interface, since it forms either the Schottky contact or is used as the source material for recombination centre diffusion.

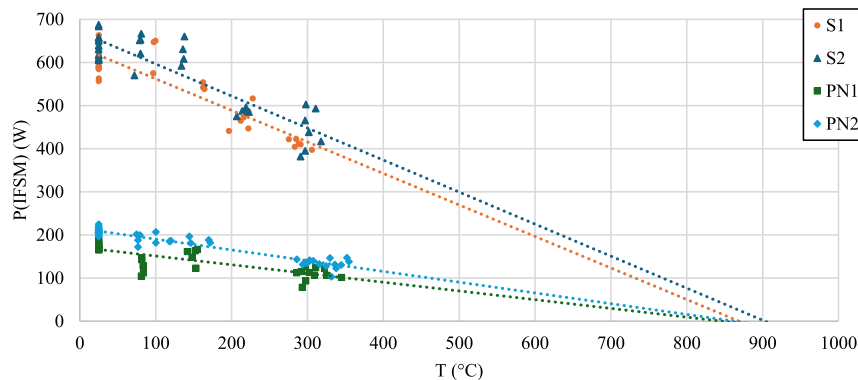


Fig. 1. Peak power during IFSM measurement plotted as a function of the junction temperature prior to the surge test for Schottky diodes (S1, S2) and PN diodes (PN1, PN2). The extrapolation to $P(IFSM) = 0$ yields the defect failure temperature as indicated.

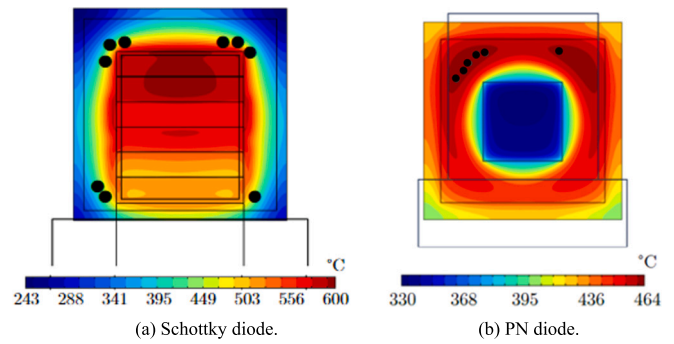


Fig. 2. Silicon-metal interface peak temperature during IFSM test, as obtained from thermal impedance simulation for Schottky (a) and for PN (b) diodes after $t = 5.3$ ms, with indication of the failure locations (●). Also shown is the location of the soft soldered clip.

3. Failure locations and FEM simulations

To explain the findings, the devices are simulated using a partial-electro-thermal finite element method models in COMSOL. The models are set up with the silicon die, the front metal stack, soft solder and the respective clip bond on the top, the back metallization and copper lead frame on the backside. For the sake of simplicity, the epoxy molding compound (EMC) is neglected and boundary conditions without heat transfer to the ambient are applied, resembling the poor thermal conductivity of the package material.

For all layers excluding the epitaxial layer, temperature dependent material parameters that are fully coupled in an electro-thermal simulation were used. To account for the diode behaviour in the model, the resistivity of the epitaxial layer is matched to the measured current-voltage characteristics during the surge current events as observed during the measurements. Therefore, this layer is not fully coupled in the electro-thermal simulation and thus we refer to the term “partial-electro-thermal”, however, the current is implicitly temperature dependent due to the change self-heating during the measurement. Dynamic losses in the diode can be neglected in this case as the diode is not switched from forward to reverse bias. The static losses are divided into two parts; first, the resistive loss based on the current-voltage characteristics, and a second part based on the threshold voltage of the diode. The resistivity of the epitaxial layer is derived from the total resistance based on the current-voltage characteristics obtained from the surge current measurements after subtracting the forward voltage of the diode $R_d = (V - V_T)/I$. Next, the partial resistances of all layers except the epitaxial layer are subtracted. With the geometric entities, the remaining epitaxial layer resistance is converted to a current dependent resistivity and assigned to the epitaxial layer in the model. The epitaxial layer is the

main contributor for the current dependent heat generation of the partial-electro-thermal model. The dissipated power due to the threshold voltage is added as a current dependent volumetric heat source ($P' = I_{FSM} \cdot V_T$) to the epitaxial layer, based on the prior assumption that the majority of the power is dissipated in the epitaxial layer. This volumetric heat source is time and current dependent, the dissipation is uniformly distributed in the entire epitaxial layer and therefore not dependent on electrically simulated current density.

The chip failure locations are found in all cases outside of but in close proximity to the soft soldered die top surface, i.e. in the area with bad thermal and sufficiently good electrical contact. The respective pictures of the de-capped silicon chips are shown in Fig. 3 and Fig. 4.

For the PN rectifier devices, the Al metal layer in the metal stack outside the solder area is fully molten as seen from the topography of the metal surface (Fig. 3(a)). This is in line with the thermal impedance simulation in Fig. 2 since the Al melting temperature is as low as 660 °C. However, the silicon defect leading to the device failure as indicated in Fig. 3 is only found in very localized spots, just next to the soft solder joint.

For the Schottky devices, the front metallization is only molten around the soft soldered clip as shown in Fig. 4. All analysed samples show the failure location in proximity to the clip attach and the majority of the analysed samples exhibit the failures at the narrow end of the clip. The extracted failure locations from the experiments are indicated (●) in the simulated temperature in Fig. 2 and correspond to the area of maximum temperature.

3.1. Simulated temperature distribution

The FEM simulations show substantial differences of the hotspot locations relative to the clip between the Schottky and PN devices. Fig. 5 indicates the location of primary heat generation at the junctions and in the epitaxial layer of the device. The epitaxial layer has the lowest doping concentration and thus the biggest resistivity, making for the biggest voltage drop and thus power dissipation in the device.

The distance of the epitaxial layer to the front metallization has major influence on the maximum temperature in the metal. Unlike in Schottky devices, the comparably thick, highly doped p+ well distributes the total current more efficiently over a bigger area of the chip. Hence, the current density in the thermally poor connected, i.e. higher local thermal impedance, region outside the soft solder area is higher compared to Schottky devices, resulting in a ring with higher temperature around the soft solder (Fig. 5(d)). In contrast to this, the Schottky device as shown in Fig. 5(d) is limited in the ability to spread the current and the resulting peak temperature is close to the clip contact area.

Fig. 6 shows the rapid decrease in vertical current density outside the soft solder area for the Schottky devices and indicates a local maximum around the solder edge. The regions with highest surface temperatures from Fig. 2 and the failure locations are in line with this ring.

The bigger clip-volume to die-volume ratio of the PN devices

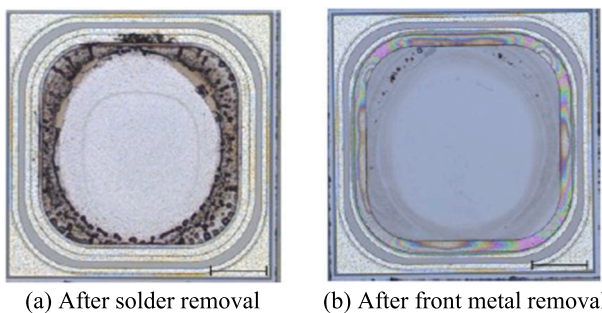
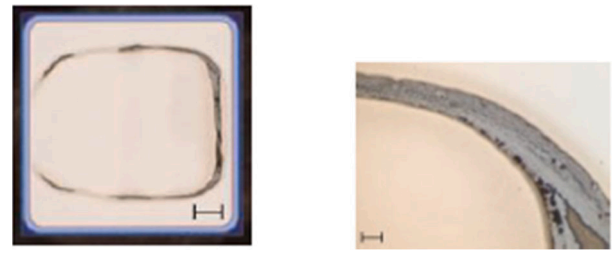


Fig. 3. Failure analysis of PN diodes after different etch steps. Scale bar corresponds to 200 μm .



(a) After front metal removal. (b) Local thermal runaway. Scale bar corresponds to 200 μm . Scale bar corresponds to 20 μm .

Fig. 4. Failure analysis of Schottky diodes after removal of front metallization.

amplifies the metal temperature difference. Due to the bigger ratio, PN devices have a bigger thermal capacitance than Schottky devices, improving the thermal performance. These two effects explain the different temperature distributions of Schottky and PN devices, resulting in a substantial temperature gradient in the PN chip to the clip.

4. Sentaurus simulations and failure model

The observed, very localized defect topography is known for the effect of local thermal runaway, which can happen as soon as regions with negative temperature coefficient of the forward voltage are not sufficiently stabilized by a good thermal contact. The heat generated at IFSM tests raises the intrinsic carrier concentration to a level orders of magnitude above the *epi* doping level, and it approaches the concentration of the injected charge carriers.

4.1. Failure model for PN rectifier

For PN devices, the charge carrier concentration n in the device can be described by Eq. (3), where n' is the donor induced carrier density and n_i is the intrinsic charge carrier density. Under normal operation, n_i can be neglected and $n \approx n'$ holds.

$$n = n' + n_i \quad (3)$$

At higher temperatures, n_i grows exponentially following Eq. (4), where N_c and N_v are the effective density of states in the conduction and valence band, respectively, E_g is the band gap energy, k is Boltzmann's constant, and T is the temperature, respectively. When all donor atoms N_d have been ionized, i.e., $n' \rightarrow N_d$, n_i saturates and exceeds n' ($n_i \gg n'$). Then, the charge carrier concentration becomes $n \approx n_i$.

$$n_i = \sqrt{N_c N_v} \exp(-E_g/(2kT)) \quad (4)$$

This effect can also be described in a simplified way using the temperature coefficient of the forward voltage of the material. PN junctions in silicon have a negative temperature coefficient, meaning that for increasing temperatures the resistance decreases. Higher currents increase the temperature in the material. The increased temperature decreases the forward voltage and thus the current along this path is increased even more. This effect will then eventually result in local thermal runaway of the device in areas of lower thermal conductance.

The formation of very localized small defects on the die is enhanced by the Al metallization, as Al is known to form spikes in silicon due to silicon diffusion in Al [5].

4.2. Failure model for Schottky rectifier

For Schottky rectifiers, minority carrier injection must be considered when the forward current density j exceeds the saturation current density j_{ns} of the device. Scharfetter showed in [6] that the minority carrier injection ratio γ becomes proportional to the current density j as in Eq. (5), with the electron and hole mobility μ_n and μ_p , respectively.

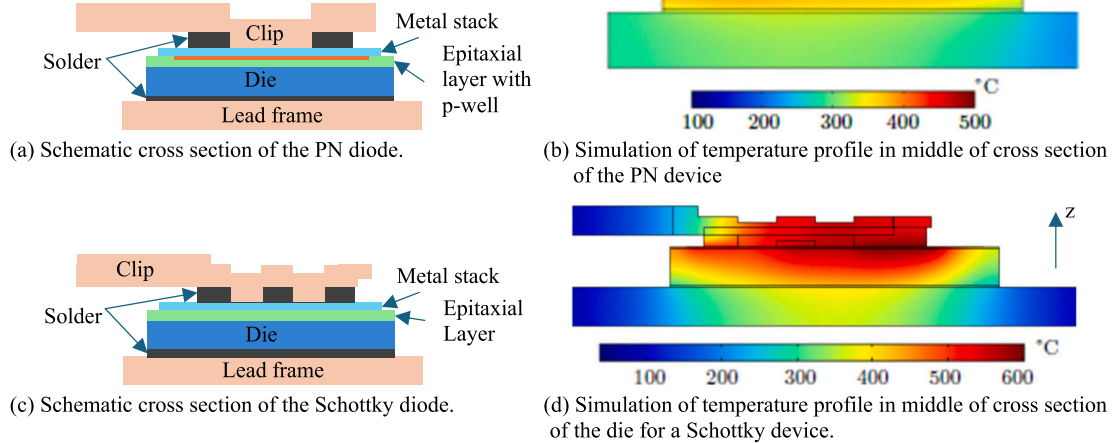


Fig. 5. Electro-thermal simulation of peak temperature during IFSM pulse after $t = 5.3$ ms.

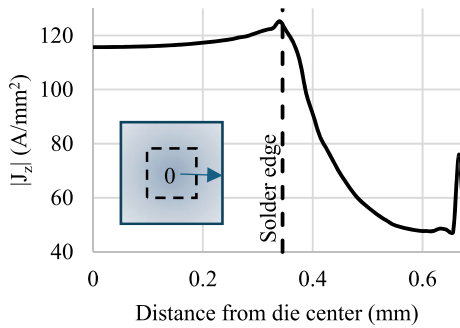


Fig. 6. Absolute current density in vertical direction in Si-metal interface of a Schottky diode at $t = 4.15$ ms.

$$\gamma = \frac{\mu_p n_i^2 j}{\mu_n N_d^2 j_{ns}} \quad (5)$$

This effect causes a rapid increase of minority charge carriers, i.e. holes, in the semiconductor epilayer contributing to the total current flow. It reduces the epilayer resistivity and causes a negative temperature coefficient of the forward voltage.

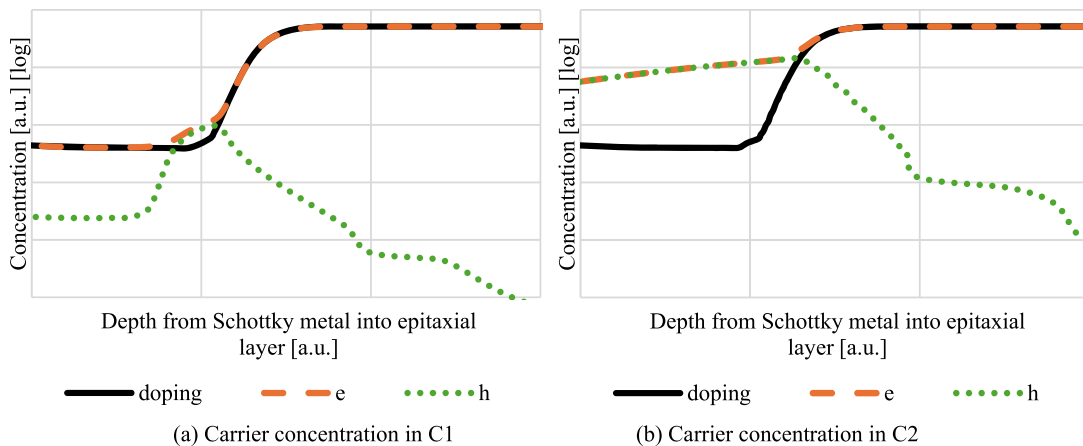


Fig. 7. Sentaurus simulation results of charge carriers in a Schottky junction thermally stable region (C1) (a) and thermal runaway region (C2) (b). The cutlines relative to the clip are indicated in Fig. 8, respectively.

Device simulations in Sentaurus confirm these assumptions as shown in Fig. 7, where the carrier concentration in the thermal runaway region h(C2) exceeds the doping concentration. In comparison, the carrier concentration (C2) in the thermal runaway regions exceeds carrier concentration (C1) in the thermally stable regions by orders of magnitude. This is possible due to the high-energy holes injected from the high-barrier Schottky contact at elevated temperature, modulating the overall current under large forward bias [7]. Accordingly, the simulations show a significantly increased current density in the hotter regions at the cross section C2 in Fig. 8 whilst in normal temperature regions under the clip (section C1), the current density remains reasonably uniform.

This current modulation in the epilayer increases the total current density in the thermally unstable regions above the saturation current density and leads to device destruction.

5. Conclusion and outlook

Using surge current measurements at elevated temperatures, the failure temperature of the PtSi Schottky and Pt killed PN rectifiers was determined by extrapolation. The determined failure temperature of 850 °C matched the melting point of PtSi for both device types. FEM

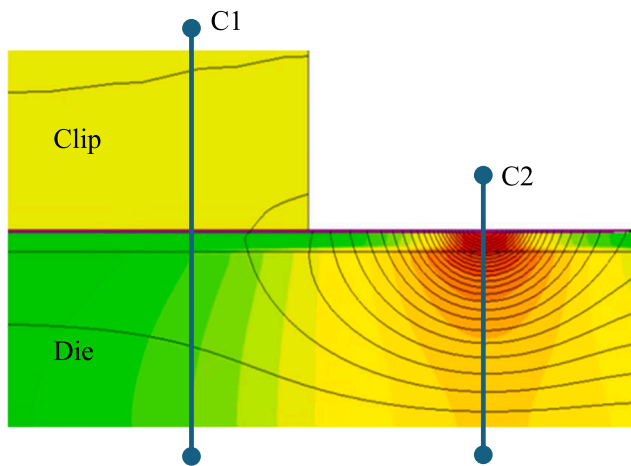


Fig. 8. Qualitative analysis of surge current density and temperature in TCAD simulation. Colours indicate current density, lines correspond to temperature, respectively.

simulations did not verify the failure temperature due to the difficulties of simulating the exact behaviour of semiconductor junctions. Therefore, the model was aligned to the device behaviour based on the measurements. However, the failure locations on the de-capped DUTs can be mapped to the hottest areas according to the simulations. Combining and comparing FEM and TCAD simulations, the failure can be explained by local thermal runaway for both device types. This is caused by negative temperature coefficient due to hole injection from the PN junction or the Schottky contact at high temperatures.

To improve the surge current capability of power diodes, one approach can be to decrease the current density gradient across the junction of the diode. This can be done by increasing the front metal thickness of the metal stack or increasing the dimple size of the clip. Both countermeasures also improve the thermal path between the junction and the copper clip. However, increasing the dimple size of the clip or increasing the solder coverage between the clip and the front metallization may give rise to other failure mechanisms not discussed in this paper.

CRediT authorship contribution statement

Ole Jonathan Bergmann: Methodology, Software, Validation,

Formal analysis, Investigation, Writing – original draft, Writing – review & editing, Visualization. **Tim Boettcher:** Conceptualization, Methodology, Resources, Writing – original draft, Supervision, Project administration. **Hoan Vu:** Conceptualization, Software, Resources, Supervision, Project administration. **Hoc Khiem Trieu:** Supervision.

Declaration of competing interest

The authors declare that they have no conflicts of interest or personal relationships that could have appeared to influence the work reported in this article.

Acknowledgement

This work has been supported by European public funding via Xecs (project reference: 2022013) in context of the e²LEAD project. Xecs is part of the EUREKA Clusters.

Data availability

The data that has been used is confidential.

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