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Low-power Relaxation Oscillator with Temperature-compensated Thyristor Decision Elements

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Abstract
This paper presents a low-power 140 kHz relaxation oscillator (ROSC) for low-frequency clock generators and timers. In voltage-mode ROSCs, unavoidable shunt current consumption results from voltage slewing at the integration capacitor. The proposed circuit employs CMOS thyristor-based decision elements which effectively reduce shunt currents by exploiting internal positive feedback. A complementary-to-absolute temperature (CTAT) current reference compensates for the frequency's temperature sensitivity. In order to achieve high negative temperature coefficient with small area and power overhead, the circuit reuses parts of the positive-to-absolute temperature (PTAT) bias generation block. Moreover, a modified start-up circuit with 3 times faster oscillator power-on is presented. The 0.09 mm^2 oscillator consumes 6.5 nW/kHz at 1.5 V to 2.5 V supply if only the CTAT source is considered, resulting in a power consumption of 907.4 nW at 140 kHz. The measured temperature coefficient of −514.7 ppm/K in the range of −40 °C to 85 °C shows an improvement of 5.5 times compared to the uncompensated case. A supply sensitivity of 2.62 %/V, a frequency resolution of 2.67 kHz/step, and an average clock jitter of 6.02 ns are achieved. The oscillator is embedded in an ultra-low power system-on-chip for autonomous environmental sensing.

Keywords Relaxation oscillator · CMOS thyristor · Low power

1 Introduction

System-on-chips (SoCs) employed in biomedical implants or autonomous Internet-of-Things sensor nodes have to operate from days to years with one battery charge, which puts tight requirements on the integrated components [1]. The information processing of slow biomedical or environmental signals usually takes place in the range of a single to few thousand samples per second. Stable low-frequency clock sources and always-on timers operating within a power budget of only few nanowatts are strongly desired [2]. At the same time, fast system start-up shortens the expensive active time of wireless sensor nodes, which are called remotely out of a sleep state [1].

Conventional discrete crystal oscillators offer pure spectral properties, but modern highly-integrated systems with rigid price and size constraints need alternatives. Hence, integrated clock sources, which come cheap, CMOS-compatible, and energy-efficient, become increasingly popular. Ring oscillators, *RC* oscillators, and relaxation oscillators (ROSCs) are the most common types, but suffer from increased inaccuracies such as clock jitter and sensitivity to process, voltage and temperature (PVT) variations [3].

In the last decade, substantial improvements to the voltage-mode ROSC topology have been presented: A decision element (DE), i. e. a comparator, compares a reference voltage with the voltage across an integration capacitor which

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is charged by a current source or via a resistor. Modern ROSC designs are an appropriate choice for low-power SoCs because of superior PVT tolerance, 50% duty cycle, acceptable jitter, and excellent power-efficiency [4, 5]. On the other hand, biomedical and IoT applications need timers and real-time clock generators with low oscillation frequencies, which brings up two major challenges:

(I) The relaxation principle results in voltage slewing at the input of the DE [1]. Fast high-gain comparators are desired for low shunt currents and low timing error, but require increased power consumption. The trade-off between shunt currents and comparator speed, power and area becomes a burden for oscillation frequencies below several kilohertz. As an outlook, long-time delay circuits utilize CMOS-compatible thyristor structures formed of gate-coupled PMOS and NMOS, which effectively reduce shunt currents [6]. Large delay times can be achieved with very low switching power [7]. Several thyristors have already been combined to low-power ring oscillators [8, 9], raising interest for employment in ROSCs.

(II) Varying temperature affects the oscillator's accuracy during operation. While supply- and process-dependent frequency deviations can be handled by regulated supplies and additional trimming circuits adjusted during production test, temperature stability requires on-chip compensation circuitry. Digital feedback loops and look-up tables can support the circuit at the expense of increased system complexity [10]. Analog methods such as stabilized current references can reduce the temperature coefficient (TC) substantially, but the loop delay variation associated to comparators and logic remains [3]. Tsubaki et al. [11] propose an additional reference voltage generation cycle, which cancels out the delay variation differentially. Another compensation method is the employment of a current reference with temperature behavior matched to the loop TC [12]. A complementary-to-absolute temperature (CTAT) current reference shows quite effective, but the additional analog source component increases total area and power of the oscillator circuit [13].

In this paper, which is an extension of work originally presented in 2021 IEEE Nordic Circuits and Systems Conference (NorCAS) [14], we present a voltage-mode ROSC with three novel contributions: First, we propose CMOS thyristor circuits as power- and area-efficient DEs for critical voltage slewing. Second, a matched CTAT current reference handles the thyristor temperature variation. An increased negative TC is generated with low area and power by reusing one V_{BE} of the positive-to-absolute temperature (PTAT) generator typically existing in SoCs. Finally, the presented ROSC is especially aimed for heavily duty-cycled low-power SoCs in IoT and biomedical applications. In order to enable precise wake-up of entire systems, we propose a modified current source start-up circuit. Compared to the original work from [14], we provide additional details on the thyristor DEs operation and investigate the sources of non-ideal temperature behavior. We review the compensation and calibration mechanisms including TC enhancement and fast start-up circuit. Additional detailed analysis and measurement results are presented.

This paper is organized as follows. In Sect. 2, the conventional ROSC architecture is reviewed. The proposed circuit is introduced in Sect. 3 and implementation details of thyristor DEs, current source with V_{BE}-reuse, and TC compensation are discussed in Sect. 4. Section 5 shows experimental results and Sect. 6 presents conclusions.

2 Architecture of conventional relaxation oscillator

The simplified block diagram of a conventional ROSC suitable for low-frequency clock generation is shown in Fig. 1. Voltage-mode ROSCs are composed of one or two identical integration capacitors C_0 and C_1, voltage reference V_{ref} and DEs, which are typically realized as dynamic CMOS comparators. The differential output clock with frequency $f_{clk} = 1/t_{clk}$ is the difference of switch signals ϕ_0 and ϕ_1 produced by a digital RS latch. The charging current can be provided from a resistor forming an *RC* element, but low-power and low-speed designs require I_{osc} in the range of several nanoamperes. In order to prevent excessive resistor noise and area, a combination of capacitors and current reference I_{osc} is the preferred solution [2].

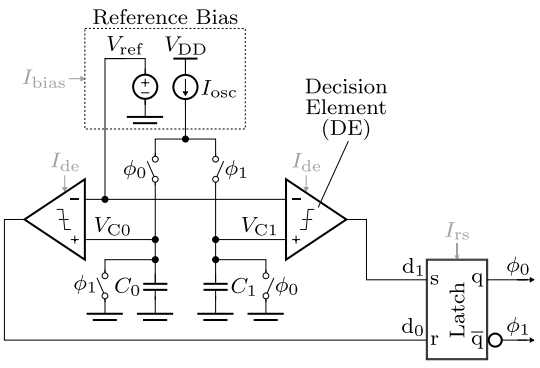


Fig. 1 Simplified block diagram of conventional relaxation oscillator

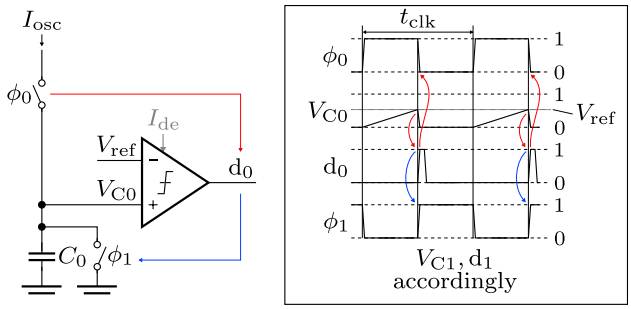


Fig. 2 Waveforms in conventional relaxation oscillator [14]

2.1 Conventional oscillation mechanism

The waveforms in a conventional ROSC are shown in Fig. 2. The path of I_{osc} is changed periodically with $t_{clk}/2$, which is controlled by alternating ϕ_0 and ϕ_1. The operation principle is explained assuming $\phi_0 = 1$ and $\phi_1 = 0$: The current source charges C_0, while C_1 is discharged. The voltage V_{C0} at the positive comparator terminal is determined by charge equality and increases linearly with slew rate dV_{C0}/dt,

$$V_{C0}C_0 = \frac{I_{osc}t_{clk}}{2} \tag{1}$$

$$\frac{dV_{C0}}{dt} = \frac{I_{osc}}{2C_0}\,. \tag{2}$$

Eventually, the charging node V_{C0} reaches the decision threshold of the comparator at V_{ref} and the output signal d_0 resets the RS latch. As a result, ϕ_0 switches to 0 and ϕ_1 to 1, which repeats the operation likewise for C_1 branch. C_0 is switched to ground. The relaxation time period depends on capacitor sizes, I_{osc} and V_{ref},

$$t_{relax} = \frac{(C_0 + C_1)V_{ref}}{I_{osc}}\,. \tag{3}$$

Second order terms $t_{2^{nd}}$ such as comparator offset V_{os}, comparator delay $t_{d,comp}$ and logic delay $t_{d,logic}$ play a larger role with increasing frequency,

$$t_{clk,conv} = t_{relax} + \frac{(C_0 + C_1)V_{os}}{I_{osc}} + 2\,t_{d,comp} + 2\,t_{d,logic} \tag{4}$$

$$= t_{relax} + t_{2^{nd}}\,. \tag{5}$$

The influence of PVT variations on t_{relax} can be reduced sufficiently with trimming and temperature compensation methods applied to I_{osc} and V_{ref} [15]. The second-order terms can show complex PVT dependencies and require more sophisticated compensation methods, which increase complexity, area and power consumption [10]. Fortunately, in low-frequency designs with output frequencies in range of several kilohertz, the overall clock period equals in good approximation t_{relax}, which requires no compensation of second-order terms. Note that the circuit of Fig. 1 demands perfectly matched comparator offsets and capacitors for a duty-cycle of 50%.

2.2 Shunt currents at decision threshold

The average power consumption of a voltage-mode ROSC can be noted down as

$$P_{osc} = V_{DD}(I_{osc} + 2I_{de} + I_{rs} + I_{bias})\,. \tag{6}$$

In (6), I_{de} and I_{rs} are dynamic currents associated to DEs and latch, respectively, and I_{bias} result from bias generator block. Figure 3 provides a closer view of the integration voltage V_{C0} in the moment of decision making. The operation at the V_{C1} branch is likewise. Capacitor C_0 is charged within $t_{clk}/2$ to V_{ref} with a visible slewing according to (1). Assuming a low clock frequency, the integration voltage slowly increases and it drives the DE in meta-stable region around decision threshold V_{ref} during t_{meta}, before the output is actually switched. Exactly at the threshold, I_{de} is at its maximum. The dynamic comparator draws shunt current I_{sh}, resulting in high power consumption [16]. Especially in low-frequency clock sources and timers employed in low-power SoCs, designers are forced to implement high-speed, high-gain comparators to cope with slewing. The increased static power consumption and complexity of such circuits burden the overall power and area budget. According to literature, conventional ROSCs following the principle of Fig. 1 achieve FoMs up to 15 nW/kHz and areas up to 0.11 mm^2 [2, 11].

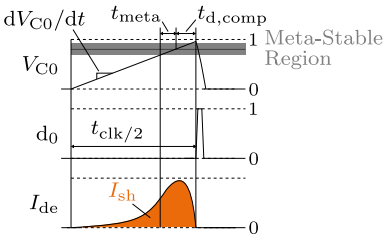


Fig. 3 Shunt current in DE as V_{C0} approaches decision threshold

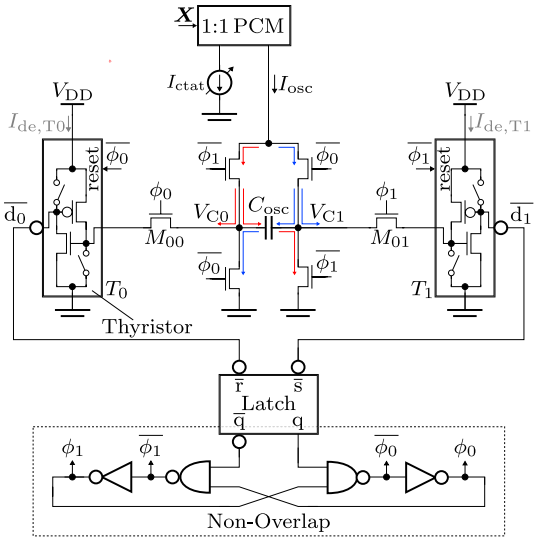


Fig. 4 Block diagram of proposed relaxation oscillator with simplified CMOS thyristor decision elements [14]

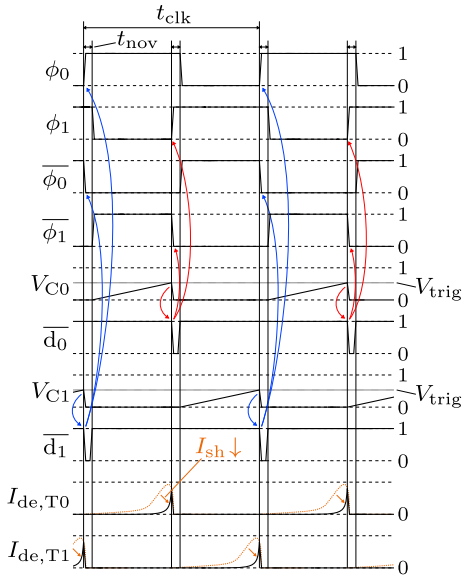


Fig. 5 Waveforms and shunt current in CMOS thyristor-based ROSC

3 Proposed thyristor-based relaxation oscillator

Compared to the conventional architecture, the thyristor-based ROSC proposed in Fig. 4 employs (i) CMOS thyristor decision elements instead of classical dynamic comparators, (ii) only one integration capacitor, (iii) a non-overlapping clock generator producing four clock phases ϕ_0, $\overline{\phi_0}$, ϕ_1 and $\overline{\phi_1}$, (iv) no voltage reference, and (v) a programmable 1:1 current mirror (PCM).

3.1 Operation principle

The operation of the proposed circuit is depicted in Fig. 5. It is in general similar to the conventional one. Simply said, the thyristor DEs T_0 and T_1 behave like inverters and toggle their state if the input voltage equals trigger voltage V_{trig}. Assume the non-overlapping signals $\phi_0 = 1$, $\overline{\phi_0} = 0$, $\phi_1 = 0$ and $\overline{\phi_1} = 1$. Pass-gate transistor M_{00} connects the left terminal of C_{osc} and I_{osc} to the input of thyristor T_0. The right terminal of C_{osc} is connected to ground. With this configuration, V_{C0} rises with a slew rate defined by (1). When T_0's trigger voltage V_{trig} is reached, its output $\overline{d_0}$ toggles and resets the RS latch. The V_{C1} branch is activated with $\phi_0 = \overline{\phi_1} = 0$ and $\overline{\phi_0} = \phi_1 = 1$. The positive feedback mechanism and the small transistor sizes inside the thyristor shorten the transition time, which reduce peak magnitude and duration of $I_{de,T0}$ and $I_{de,T1}$ compared to high-gain dynamic comparators. With (4), the clock period can be calculated to

$$t_{clk,prop} = \frac{2C_{osc}V_{trig}}{I_{osc}} + 2\,t_{thyr} + 2\,t_{d,logic} \approx \frac{2C_{osc}V_{trig}}{I_{osc}} + 2\,t_{thyr}\,, \tag{7}$$

where thyristor delay t_{thyr} is a non-linear, temperature-dependent term [17].

4 Implementation details

The proposed ROSC is implemented in a 180 nm partially-depleted silicon-on-insulator (PD-SOI) CMOS technology. I_{osc} is chosen to be 50 nA and C_{osc} = 300 fF, resulting in oscillation frequency of 140 kHz and a simulated average core power consumption of only 90 nW.

4.1 Thyristor decision element

The proposed N-type thyristor decision element is based on the conventional CMOS thyristor delay element, which is known for its large and reliable time constants suitable for low-power timing circuits [17]. Figure 6 shows the basic block diagram. The thyristor circuit is the CMOS equivalent of a classical semiconductor PNPN thyristor behaving like a surge relay between nodes a and b. The normally-off device is turned on by a single pulse at the ctrl node. The bottom part of Fig. 6 shows the core thyristor formed by gate-drain coupled M_P and M_N and complemented by additional reset switches, output inverter, and *IC* integrator circuit, resulting

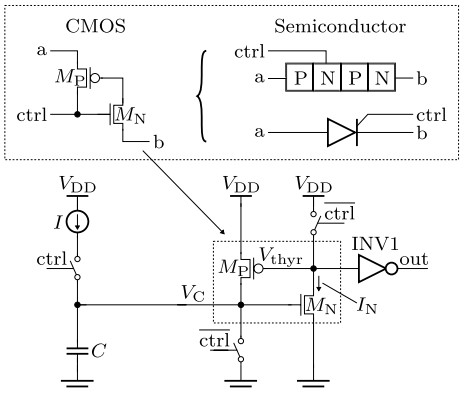


Fig. 6 Block diagram of one-stage thyristor delay element

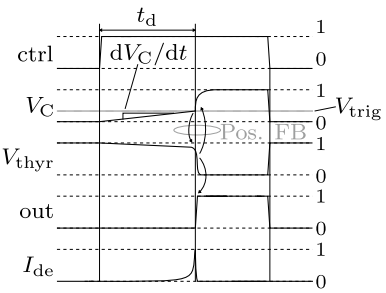


Fig. 7 Waveforms in one-stage thyristor delay element

in a thyristor delay element frequently employed in literature [18, 19].

The operation of a thyristor delay element is shown in Fig. 7. Initially, ctrl = 0 and nodes V_C and V_{thyr} are reset to ground and V_{DD}, respectively. A rising edge of ctrl starts the charging of capacitor C with slew rate dV_C/dt, while the thyristor remains first in a stable off-state. Floating V_{thyr} stays around V_{DD}, but it is slowly discharged by small M_N drain current. The thyristor trigger voltage equals approximately the NMOS threshold voltage V_{THN},

$$V_{trig} \approx V_{THN} . \tag{8}$$

In the proposed thyristor-based ROSC, V_{THN} acts like the reference voltage in a conventional design. With $V_C \approx V_{THN}$, a sharp transition occurs when the exponentially increasing I_N pulls down the gate of M_P. In turn, the open M_P pulls up V_C in a positive feedback loop and the output signal switches to 1. The mechanism is sped up by choosing small transistor sizes, increasing aspect ratio W/L of M_N, and decreasing W/L of M_P. However, certain minimum length and area must be sustained for V_{TH} matching and noise. Note that no path between V_{DD} and ground exists at any moment, which means except for small leakage, no direct shunt current can occur in this configuration. The CMOS thyristor is hence tolerant to small slew rates and a popular device for generating

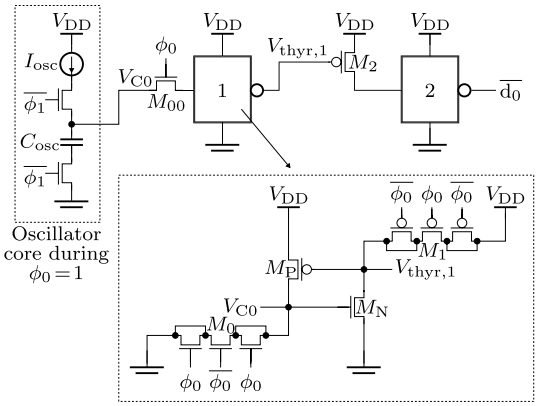


Fig. 8 Schematic of two-stage thyristor decision element

micro- and milisecond delays efficiently [8]. The time delay between ctrl and out is calculated to

$$t_d = \frac{CV_{THN}}{I} + t_{thyr} , \tag{9}$$

where the intrinsic delay t_{thyr} can be mathematically expressed as [17]

$$t_{thyr} = \sqrt[3]{\frac{6\,n\,C_N^2 C_P V_{THP}}{I_{osc}}} + t_{reg} . \tag{10}$$

C_N and C_P are the parasitic capacitances associated to the gates of M_N and M_P, respectively. n is the slope factor. The effects of the fractional and root term can be generally minimized by small transistor sizes and optimized routing. The regeneration time t_{reg} plays a minor role until very high clock frequencies [6]. Since (10) depends on technology-dependent parameters, it has to be determined in simulation or measurements. In our case, t_{thyr} is in the range of few nanoseconds.

There are striking similarities between (9) and the operation of an ROSC noted down in (4). The utilization of CMOS thyristors as DEs appears natural. The final thyristor DE used in the proposed ROSC is depicted in Fig. 8. For simplification, only one DE is shown. The integration capacitor C_{osc} is shared between T_0 and T_1. The basic DE circuit is composed of two CMOS thyristor stages formed by M_P, M_N and reset switches M_0, M_1 implemented as PMOS and NMOS, which are compensated for charge-injection by dummy transistors with half W/L. M_2 acts as a current source for the second stage thyristor and inverts $V_{thyr,1}$. Since the slew rate of $V_{thyr,1}$ is limited by intrinsic gain, a following inverter INV1 would still show excessive shunt current. The second thyristor is added instead of INV1 in order to reduce total ROSC power consumption [8].

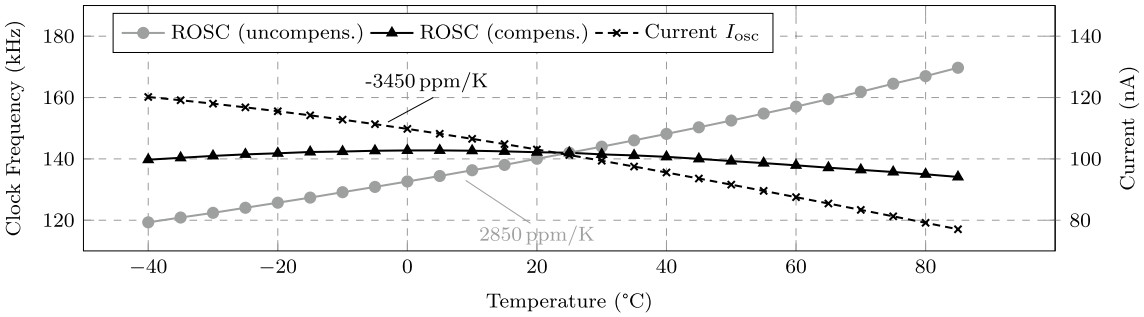


Fig. 9 Simulated temperature behavior of ROSC frequency (uncompensated and compensated) and compensation current I_{osc}

During design, the proposed oscillator was compared to a conventional ROSC with inverter-trees as the simplest form of decision elements. In simulation, the shunt power consumption was lowered by magnitudes from 706 to 0.8 pW/kHz. Moreover, conventional dynamic comparators include large matching pairs, which contribute heavily to the overall area. With 22 µm x 19 µm in 180 nm technology, the area of the thyristor DE is minor.

4.2 Single relaxation capacitor and non-overlapping clock generator

As a second feature and in contrast to the conventional architecture, Fig. 4 uses simple NMOS switches and only one integration capacitor C_{osc} [20]. This is enabled by the fact that one of the capacitors C_0 and C_1 (refer to Fig. 1) remains shorted for half a period and is therefore redundant. Both plates of single integration capacitor C_{osc} are used for storing the integration voltages in different phases, which results in theory in an accurate 50% duty cycle, reduced branch mismatch, and circuit area. This enhancement comes with the drawback that signals ϕ_0 and ϕ_1 must be produced by a non-overlapping clock generator. It ensures that I_{osc} is always connected to at least one low-ohmic switch. Otherwise, I_{osc} pinches off and produces additional PVT-sensitive loop delay. A second disadvantage is that in reality, the non-overlapping delay t_{nov} distorts the duty cycle, as shown in Fig. 5. Due to the long clock period, this effect is minor in the design, but it must be considered for higher frequencies.

4.3 Temperature compensation

Another known challenge is the temperature sensitivity of the clock frequency. In (7), the NMOS and PMOS threshold voltages $V_{THN}(T)$ and $V_{THP}(T)$ appear in the relaxation term and in the t_{thyr} term, respectively:

$$t_{clk,prop}(T) = \frac{2C_{osc}V_{THN}(T)}{I_{osc}} + 2\,t_{thyr}(T) \tag{11}$$

With $t_{clk,prop} \gg t_{thyr}$ as a good approximation, the function is linearly proportional to $V_{THN}(T)$. The temperature dependency of the NMOS threshold voltage is defined as

$$V_{THN}(T) \approx V_{THN}(T_0)(1 + \alpha_N(T - T_0)) \propto T\,, \tag{12}$$

where $V_{THN}(T_0)$ is the NMOS threshold voltage at room temperature and α_N is the first order TC [20]. For long-channel devices in 180 nm technology, α_N is simulated to be around -1200 ppm/K, i. e., V_{THN} and $t_{clk,prop}$ decrease with temperature and the oscillation frequency shows a PTAT behavior. Simulation results for ROSC frequency versus temperature are shown in Fig. 9. Without compensation, a TC of about 2850 ppm/K is achieved, resulting in more than 50 kHz deviation over temperature range from − 40 °C to 85 °C. The first order compensation mechanism works as follows: A CTAT source injects the current I_{ctat} with matched TC $\alpha_{CTAT} \approx -3450$ ppm/K via a PCM into the ROSC. Increasing temperature results in decreasing I_{ctat} and, in a linear approximation, compensates the circuit for the increasing V_{THN}. The resulting frequency curve of the total ROSC shows -350 ppm/K deviation, achieving an effective TC reduction of factor 8. As explained, only the linear TC (first derivative) is compensated and the second-order term resulting from $t_{thyr}(T)$ is ignored. Hence a slight overcompensation for temperatures above 50 °C is visible in Fig. 9, which was acceptable in our application.

4.4 Current source with current source recycling and modified start-up circuit

The I_{osc} is generated by the CTAT circuit as shown in Fig. 10. The challenge of obtaining high α_{CTAT} of -3450 ppm/K is overcome by using bipolar junction transistors (BJTs) and resistors. In order to reduce the complexity of the circuit, the CTAT is supported by V_B from the on-chip PTAT bias reference, which helps to maintain the voltage across the resistor $R_2 = R_{2,fix} + R_{2,trim}$ equal to the forward voltage drop of the diode D_1, as shown later. PTAT generators are standard

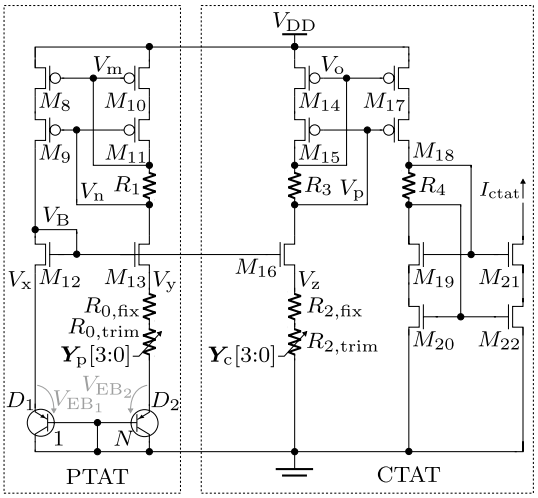


Fig. 10 CTAT current source recycling PTAT generator

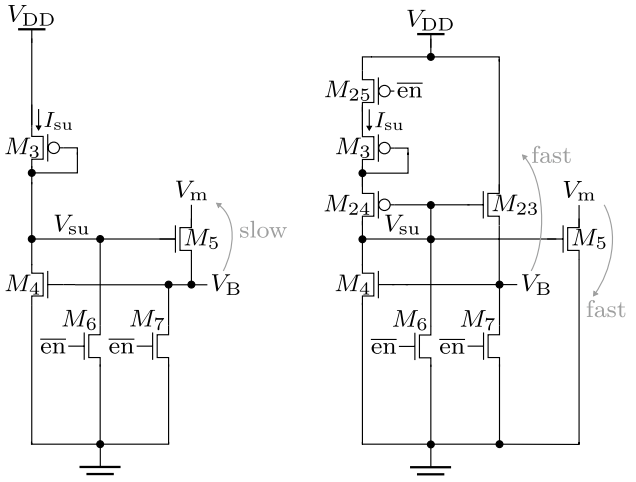


Fig. 11 Modified start-up circuit (right) versus conventional (left)

components typically employed in mixed-signal SoCs to bias the analog blocks such as amplifiers, filters, analog-to-digital converters, etc. In the context of a complete SoC, high α_{CTAT} is achieved with low additional power consumption and minor area for V_B routing. The overall chip area and power is hence not increased by the proposed PTAT recycling method rimming resistors

The current source uses self-biased low voltage cascode current mirrors. The loop across M_8, M_{10}, M_{12}, M_{13} forces the node voltages $V_x = V_y = V_{EB_1}$, where V_{EB_1} is the emitter–base voltage of diode-connected BJT D_1. The PTAT voltage and current, respectively, are expressed as [21]

$$V_{PTAT} = V_{EB_1} - V_{EB_2} = V_T \cdot \ln(N) \tag{13}$$

and

$$I_{PTAT} = \frac{V_{PTAT}}{R_0} = \frac{V_T \cdot \ln(N)}{R_0}, \tag{14}$$

where V_{EB_2} is the emitter–base voltage of D_2, V_T is the thermal voltage, and R_0 is a series combination of fixed and programmable parts $R_{0,fix}$ and $R_{0,trim}$. Likewise, the CTAT current can be noted down as

$$I_{ctat} = \frac{V_{ctat}}{R_2} = \frac{V_{EB_1}}{R_2}. \tag{15}$$

Neglecting the body effect for simplicity, the voltages V_x, V_y and V_z can be approximately calculated to

$$V_x = V_{DD} - |V_{OV,8}| - |V_{OV,9}| - V_{OV,12} - V_{TH,12}, \tag{16}$$

where V_{DD} is the supply voltage and $|V_{OV,8}|$, $|V_{OV,9}|$, $V_{OV,12}$ are the overdrive voltages ($V_{OV} = V_{GS} - V_{TH}$) of M_8, M_9, M_{12}, respectively;

$$V_y = V_{DD} - V_n - V_{OV,13}, \tag{17}$$

where cascode node voltage $V_n = |V_{OV,8}| + |V_{OV,9}| + |V_{TH,9}|$ and $|V_{TH,9}|$, $V_{OV,13}$ are the threshold and overdrive voltage of M_9, M_{13} respectively; and

$$V_z = V_{DD} - V_p - V_{OV,16}, \tag{18}$$

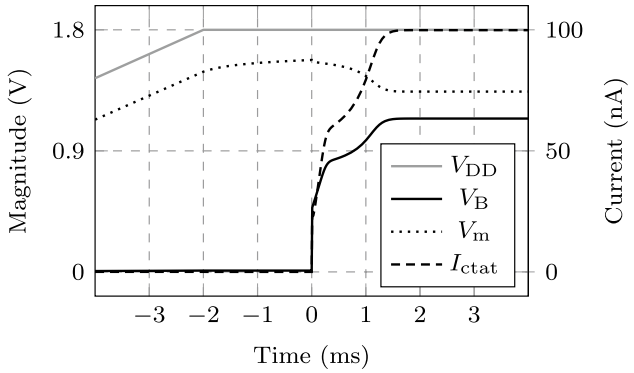
where cascode node voltage $V_p = |V_{OV,17}| + |V_{OV,18}| + |V_{TH,18}|$ and $V_{OV,16}$, $|V_{OV,17}|$, $|V_{OV,18}|$ are the overdrive voltages of M_{16}, M_{17}, M_{18}, respectively, and $|V_{TH,18}|$ is the threshold voltage of M_{18}.

Assuming all the transistors have the same threshold voltage $V_{TH} = |V_{TH}|$ and overdrive voltage $V_{OV} = |V_{OV}|$, (16), (17) and (18) can be written as

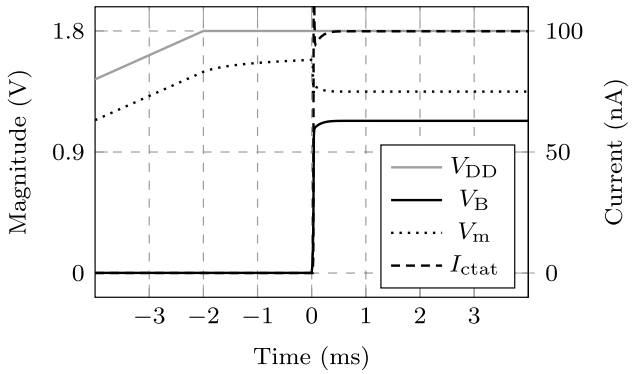
$$V_x = V_y = V_z = V_{DD} - 3V_{OV} - V_{TH}. \tag{19}$$

After manufacturing, random mismatch affects V_{TH}, and hence the V_{OV} differ for all transistors. However, layout techniques, proper sizing, and maintaining the same aspect ratios of the current mirrors (M_8, M_{10}, M_{14}, M_{17}), (M_9, M_{11}, M_{15}, M_{18}), (M_{12}, M_{13}, M_{16}) achieve a sufficient equalization the voltages $V_x = V_y = V_z = V_{EB_1}$.

The modified start-up circuit for the current reference is shown on the right in Fig. 11. The conventional start-up circuit on the left side is made up of M_3, M_4, M_5, while M_6 and M_7 are power-off switches. The operation is as follows: If the current source nodes are discharged, low V_B turns off M_4 and V_{su} enables M_5 for shorting the PMOS current mirror node V_m to V_B. The circuit starts operating as soon as



(a) With conventional start-up circuit



(b) With modified start-up crcuit

Fig. 12 Simulated starting sequence under nominal conditions, en = 1 at 0 ms

$$V_B \geq V_{TH,12} + V_{EB_1}, \tag{20}$$

where $V_{TH,12}$ is the threshold voltage of M_{12} and M_{13}. It takes a long time to charge the gates of NMOS current mirror M_{12} and M_{13}, until the current source reaches stable state and the oscillator produces target frequency.

In our application, a quick ROSC start-up is desired for short sensor node response. For this purpose, the classical start-up circuit is modified by the addition of M_{23} to charge V_B faster directly to V_{DD}. Further, M_5's source terminal is connected to ground instead of V_B. The stacked diode M_{24} helps to reduce the static start-up current I_{su}. Finally, in the conventional circuit, I_{su} flows even when en = 0. In the modified version, M_{25} acts as additional switch to provide a real power-off. Figure 12 shows the simulated starting sequence of the CTAT circuit with conventional and modified start-up circuit. Under nominal conditions, with a 10 ms rise-time of V_{DD}, and with en switching to logic high at zero time, the simulated start-up time is reduced by factor 3 from 1.63 ms to 0.45 ms.

A one-hot resistor trimming technique [22] is used across the resistors $R_{0,trim}$ and $R_{2,trim}$ in order to reduce the process variation of I_{ptat} and I_{ctat}. The major portion

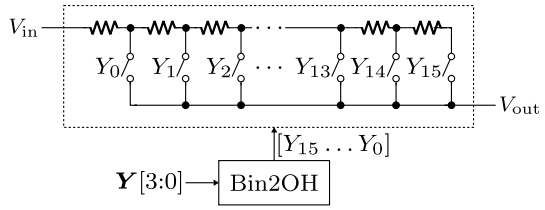


Fig. 13 One of the two one-hot coded

of required resistance is provided by fixed parts $R_{0,fix}$ and $R_{2,fix}$. The variation is handled with resistor-chains $R_{0,trim}$ and $R_{2,trim}$ controlled by two 4 bit vectors $\boldsymbol{Y}_p[3:0]$ and $\boldsymbol{Y}_c[3:0]$. They are converted to 16 one-hot coded digital signals each by binary-to-one-hot decoder blocks (Bin2OH), as shown in Fig. 13. The measured PTAT and CTAT currents with respect to the decimal trimming vectors are plotted in Fig. 14. The measurement results match the simulation results well.

4.5 Programmable current mirror

Process variations affect the oscillation frequency not only through I_{osc}, but as well via C_{osc} and V_{THN}. With nominal V_{DD} and nominal temperature, the uncalibrated output frequency shows a simulated spread from 95.0 kHz to 217.3 kHz versus process corners and a simulated standard deviation of 4.91 kHz in 1000 points Monte Carlo mismatch simulation. In conventional designs, static variations are handled by trimming during production test. For this purpose, we suggest an additional wide-range 1:1 programmable current mirror between CTAT current source and oscillator core, which can be adjusted for all process variations.

The schematic of the 7 bit PCM is shown in Fig. 15. It is implemented as partly-binary array of parallel and stacked current mirror transistors with weights [16, 8, 4, 2, 1, 0.5, 0.25] and switched cascode transistors controlled by vector $\boldsymbol{X}$. The output I_{osc} is assembled as

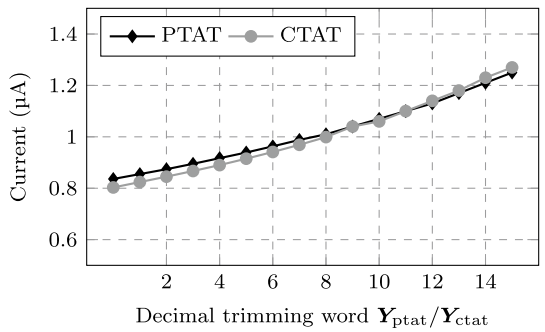


Fig. 14 Measured CTAT and PTAT currents versus trimming vector

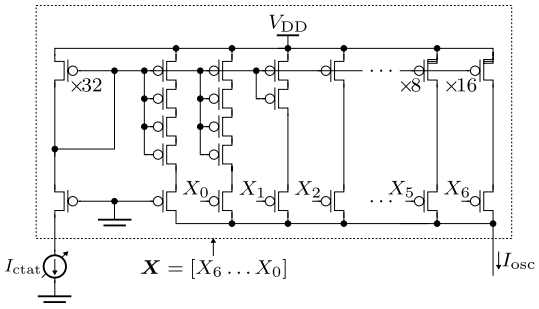


Fig. 15 Programmable 1:1 partly-binary current mirror relaying I_{ctat} towards oscillator core

$$\frac{I_{osc}}{I_{ctat}} = \frac{16}{32}X_6 + \frac{8}{32}X_5 + \ldots + \frac{0.25}{32}X_0 + \frac{0.25}{32} = \sum_{k=0}^{6} \frac{2^k}{128}X_k + \frac{1}{128}. \tag{21}$$

The PCM range starts at $I_{ctat}/128$ for $\boldsymbol{X} = [0, 0, \ldots, 0]$ and ends at I_{ctat} for $\boldsymbol{X} = [1, 1, \ldots, 1]$, i. e., $I_{osc} = I_{ctat}$. The corresponding trimming range of the oscillator frequency is simulated to be sufficient between 4.37 kHz and 264.2 kHz under nominal conditions, which refers to a theoretical frequency resolution of ±2.05 kHz. In simulations including process, voltage and temperature variations, the oscillator could be trimmed towards the target of 140 kHz with a maximum absolute error of 1.8 kHz in all cases. Compared to a conventional 7 bit binary-weighted array using 128 unit transistors, the presented circuit achieves the same output range with only 73 devices and saves 57 % of area. As a drawback, its linearity is more sensitive to parasitic layout resistors and matching. During trimming procedure, the monotonicity of the frequency curve versus vector $\boldsymbol{X}$ is a critical concern. In simulations, its differential non-linearity (DNL) [23] has been evaluated. The DNL does not exceed 1.70 kHz, i. e. it is a strictly monotonic curve.

Note, that during production test of the proposed ROSC, both current reference and PCM are trimmed in cascade. The initial trimming of I_{ctat} with $\boldsymbol{Y}$ towards 100 nA achieves a rough frequency resolution of around 16 kHz per step, which is not sufficient for our application. The additional PCM enables better frequency adjustment in the range of two kilohertz per step. However, the zoom-like trimming with $\boldsymbol{X}$ and $\boldsymbol{Y}$ is necessary, since a wider programming range of I_{CTAT} would alter its TC too much.

5 Experimental results

Twenty-two samples of the ROSC were fabricated in a 180 nm PD-SOI CMOS technology and measured in laboratory. The circuit is part of a low-power sensor readout SoC

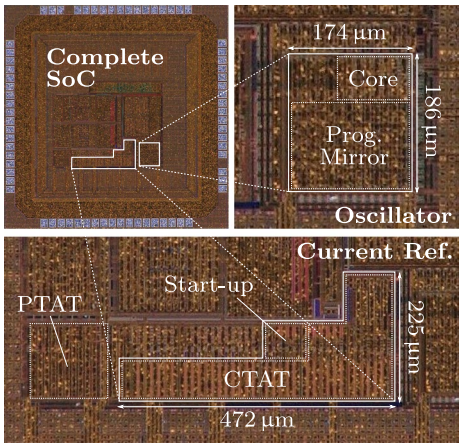


Fig. 16 Die micro-photograph of compelete SoC with proposed ROSC

[24]. A more compact layout can be achieved with PD-SOI because the oscillator and other noisy blocks can be placed closer to sensitive circuits. Less substrate noise is coupled through the fully isolated wells. Figure 16 shows a die micro-photograph. The oscillator core and current reference cover an area of 0.03 mm^2 and 0.08 mm^2 (0.06 mm^2 without PTAT), respectively. The CTAT's fixed and programmable resistors $R_{2,fix}$ and $R_{2,trim}$ occupy about 0.026 mm^2. Combined with PCM and CTAT current mirrors, all analog components require more than 95% of the total ROSC area, as depicted in Fig. 17.

The stand-alone oscillator core consumes 641.6 nW, while the current reference, without and with recycled PTAT, consumes 265.8 nW and 562.8 nW, respectively. The total ROSC power consumption is 907.4 nW excluding the recycled PTAT and 1.20 µW including PTAT, respectively. In the best case, we achieve 6.5 nW/kHz with the proposed circuit oscillating at target frequency around 140 kHz.

A histogram of the frequency distribution at nominal temperature is depicted in Fig. 18 showing a mean of 140.03 kHz. About 68% of the non-calibrated samples occur within (140 ± 3.38) kHz (one-sigma), achieving a process stability σ/μ of 2.41%. For further analysis, five samples were randomly selected and characterized deeper. The frequency deviation over a temperature range of − 40 °C to 85 °C is plotted in Fig. 19 for the compensated case. The samples show in average −514.7 ppm/K, which matches the simulated value of -350 ppm/K if layout parasitics are considered. Compared to the uncompensated simulated case, the TC improvement is 5.5times. If increased circuit area and complexity are acceptable, these results can be further improved by additional trimming structures, which adjust the TC of I_{ctat}. For completeness, Fig. 20 shows measured oscillator output waveforms of one chip sample. At different temperatures, well behaved signal integrity is achieved.

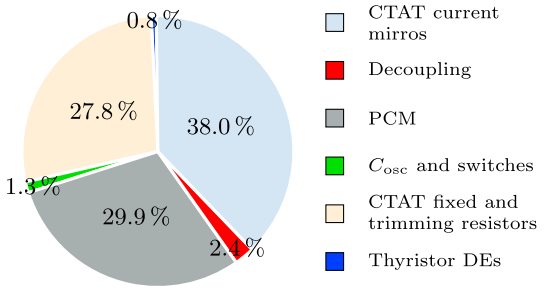


Fig. 17 Area break-down of proposed ROSC

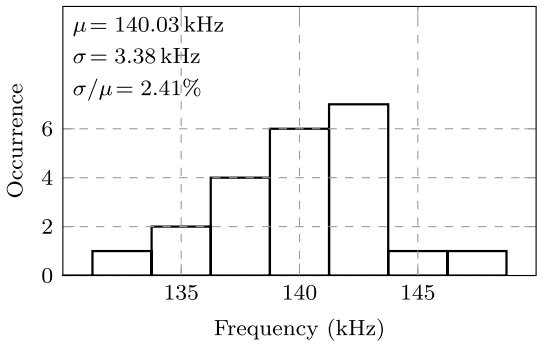


Fig. 18 Frequency distribution of 22 samples (non-calibrated, $T = 27$ °C)

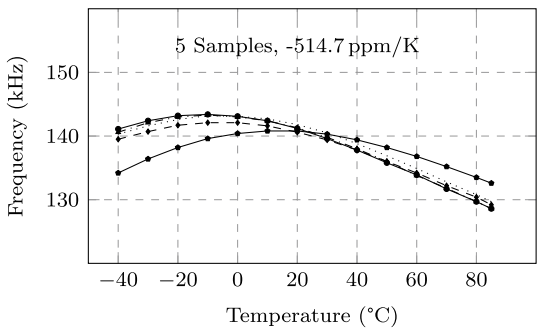


Fig. 19 Measured frequency versus temperature with compensation

The supply voltage sensitivity is $\{-0.84, +1.79\}$% over the range of 1.5 V to 2.5 V, i. e. 2.62%/V, as depicted in Fig. 21. Figure 22 shows the frequency versus trimming vector setting. The transfer curve is not linear, but strictly monotonic, which is sufficient for the final application. Finally, the cycle-to-cycle rising edge jitter is plotted in Fig. 23. The proposed ROSC achieves an average jitter of 6.02 ns across supply voltage levels from 1.5 V to 2.5 V.

In Table 1, the CMOS thyristor-based ROSC is compared to state-of-the-art relaxation oscillators. The proposed ROSC achieves competitive numbers for TC, supply sensitivity and

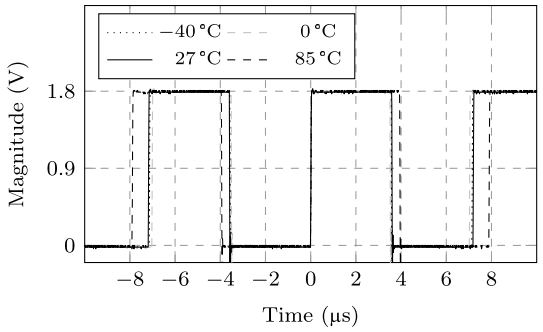


Fig. 20 Measured transient output waveform obtained at different temperatures

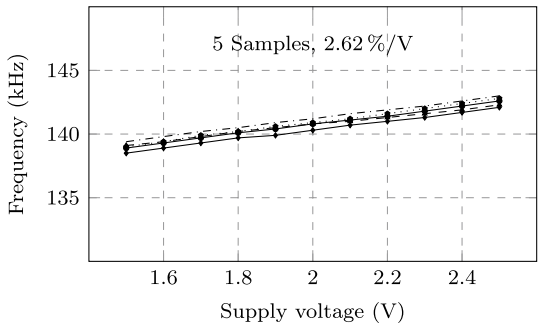


Fig. 21 Measured frequency versus supply voltage

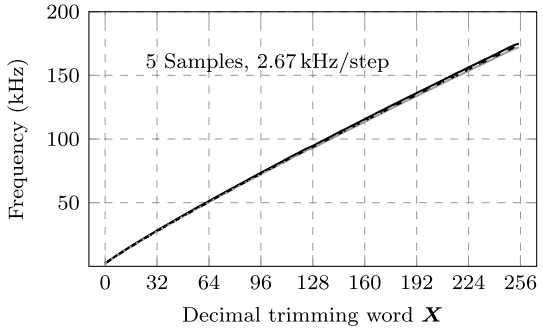


Fig. 22 Measured frequency versus trimming vector

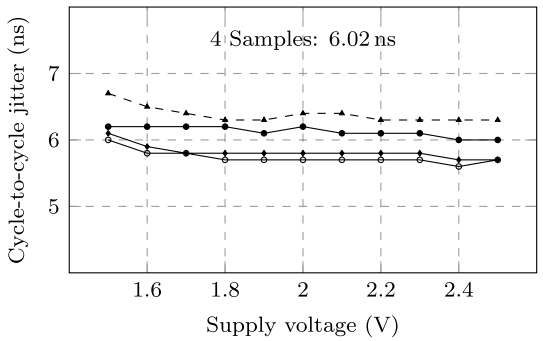


Fig. 23 Measured jitter versus supply voltage

Table 1 Performance of the proposed ROSC in comparison to prior art

	This Work[1]	[25]	[26]	[2]	[20]	[4]	[5]	[11]
Year	2021	2021	2020	2020	2019	2019	2016	2013
Tech. (nm)	180	250 BCD	180 BCD	40	180	180	180	180
Supply (V)	1.8	2.7	3.3	0.6	1.2	0.9	1.8	1.0
Area (mm^2)	0.09[2]	0.06	0.026	0.127	0.117	0.1	0.1	0.105
Frequency (kHz)	140	1370	24000	32.7	1340	943.1	32.0	32.6
TC (ppm/K)	−514.7	323.9	± 77.6	35.5	193.2	93.9	± 30	120
Supply sensitivity (%/V)	2.62	NA	0.1	0.5	NA	4.7	± 0.05 to 0.7	1.1
Process stability σ/μ (%)	2.41	NA	NA	NA	NA	NA	NA	1.4
Jitter (ns)	6.02	NA	NA	NA	NA	NA	2.0	NA
Power (nW)	907.4[2] (1204.5[3])	8910	3300	40	156000	5200	150	472
FoM (nW/kHz)	6.5[2] (8.6[3])	65.0	13.8	1.2	11.8	5.5	4.7	14.5

[1] Orginally published in [14]

[2] Recycled PTAT bias generator excluded

[3] Recycled PTAT bias generator included

process stability, and shows higher FoM at higher supply voltage of 1.8 V. The other designs operate below 1.2 V except for [20, 25, 26]. When compared to the only conventional ROSC from [11] which is exemplified in Fig. 1, a two times better FoM is achieved with an area of 0.09 mm^2, excluding the recycled PTAT, which is competitive. Circuits in [2, 4, 5] show better efficiency, nevertheless they employ non-conventional architectures. Only [25] and [26] show a smaller area, but as well a much worse FoM.

6 Conclusion

This paper presents a relaxation oscillator with novel architecture of low power decision elements. It is known from conventional designs that shunt current consumption in the comparators is increased when low oscillation frequencies generate slewing at the integration capacitor. The proposed circuit overcomes this issue by employing CMOS thyristor circuits with sharp transition due to internal positive feedback. The current consumption associated with slew rates is reduced up to 50% compared to conventional designs. The clock frequency's temperature deviation is compensated with an on-chip CTAT current source by factor 5.5. Its required highly-negative temperature coefficient is generated efficiently by reusing parts of the on-chip bias current reference resulting in minimal area and power overhead. A modified start-up circuit achieves three times faster wake-up of the oscillator, which reduces the active time duration and hence power consumption of wireless systems with remote wake-up. The proposed circuit is utilized in a system-on-chip as part of an autonomous Internet-of-Things sensor node.

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Data Availability The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declarations

Conflict of interest All authors declare that they have no conflicts of interest.

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