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Dead time optimization method for power converter

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Abstract. This paper introduces a method for dead time optimization in variable speed motor drive systems. The aim of this method is to reduce the conduction time of the freewheeling diode to a minimum without generation of cross conduction. This results in lower losses, improved EMC, and less overshooting of the phase voltage. The principle of the method is to detect beginning cross currents without adding additional components in the half bridge like resistors or inductances. Only the wave shape of the phase voltage needs to be monitored during switching. This is illustrated by an application of the method to a real power converter.

1 Introduction

Power converter systems are used today in many applications. In particular, in the context of battery supplied vehicles and similar areas the improvement of Electromagnetic Compatibility (EMC) and the reduction of power losses become increasingly important. One approach to improve power converter systems in this respect is to reduce the dead time during switching. To illustrate the concept of dead time, the following Fig. 1 shows a typical half bridge, which is used in power converter systems:

In the operation of the half bridge the Highside- and Lowside-MOSFET are mutually switched. The dead time is here defined as the time delay between the falling edge of the control signal of one MOSFET and the rising edge of the control signal of the opposite MOSFET.

With the reduction of the dead time, the time in which the freewheeling diode conducts and the stored charge in this diode, which is responsible for the Reverse Recovery Effect (Polenov et al., 2009), can be reduced. This effect increases switching losses (Polenov et al., 2009; Reiter et al., 2010) and the snap off of the reverse current results in overvoltage and oscillation of the phase voltage (Semikron, 1998, p. 166).

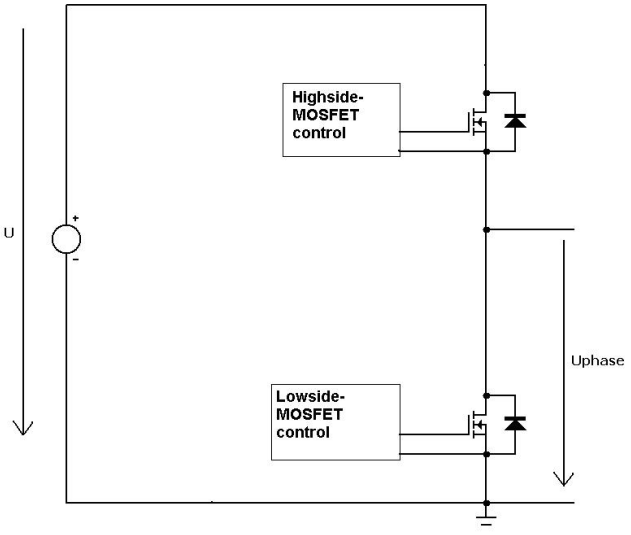

Fig. 1. Principal circuit diagram of a half bridge.

In this context an optimal dead time can prevent the diode from conducting without generating a cross current in the half bridge.

Several methods already have been introduced to reduce the dead time. Many are especially for DC/DC converter systems. For example Reiter et al. (2010) describes an approach which reduces the dead time in one phase and compares after every step the efficiency to a reference phase. An increasing efficiency in one phase will result in an increase of its current. A current balancing controller compensates the resulting deviation of the phase currents. This information can be used for the dead time optimization. As a result, this method uses the existing current balancing controller of a multiphase DC/DC-converter, which does not exist in power converters.

In Yousefzadeh and Maksimović (2005) a method that applies to DC/DC-converters is described which changes the dead time until the duty-cycle command is minimized, corresponding to maximized converter efficiency. This method uses the integrated voltage controller which doesn't exist in that form in a power converter.

Another approach measures the voltage drop across the freewheeling diode (Mappus, 2003). The dead time is reduced until this voltage drop no longer reaches the diodes forward voltage. But measuring this voltage drop is difficult during current commutation because of the influence of induced voltages in the parasitic inductances (Rose et al., 2009).

In addition to these approaches there are several methods which use Zero Voltage Switching (ZVS), compare (Trescaes et al., 2004; Acker et al., 1995; Lau and Sanders, 1997). Most of these methods involve measuring the voltage drop across the switching transistor and the gate-source voltage which is compared to the threshold voltage. However, these approaches can only be used in conjunction with ZVS. In contrast to this, the method described in this paper is focused on a hard switching converter.

Beside the approaches above, there are further methods which apply to hard switching three phase power converters. In Huselstein et al. (1993) an inductance is introduced in the half bridge. This allows detecting an occurring cross current from the change of voltage drop across this inductance: This change can be measured and then the dead time is reduced until a cross current occurs. Here, the main problem is the inclusion of the inductance into the half bridge which can result in a worsening of the switching behavior. An additional method described in Rose et al. (2009) measures the threshold voltage of the MOSFETs involved. The beginning and the end of the current commutation is detected by means of a small inductance introduced in the half bridge. Since the complexity of this method is relatively high, a new designed gate driver is used to reduce the dead time according to this information. This can be disadvantageous because often a simpler and more flexible method is desired which does not require a special Integrated Circuit (IC). Also an additional inductance is needed and it can be assumed that the measurement of the threshold voltage has to be very exact to prevent cross conduction.

In this paper a method is presented which does not require additional components in the half bridge. Only the wave shape of the phase voltage during switching has to be monitored. When a cross conduction occurs, this wave form changes, as it is also stated in (Yousefzadeh and Maksimović, 2005) in view of DC/DC converter systems. These changes have been verified by means of simulation of a half-bridge and measurement in an existing power converter. This power converter is designed for low voltage applications, such that Power-MOSFETs can be used. A measuring circuit has been designed to detect this variation without the need of special or extremely fast components. The measured phase voltage is the basic for the proposed dead time optimization process which successively reduces the dead time until the changes in the wave shape of the phase voltage, that are due to the cross current, are detected.

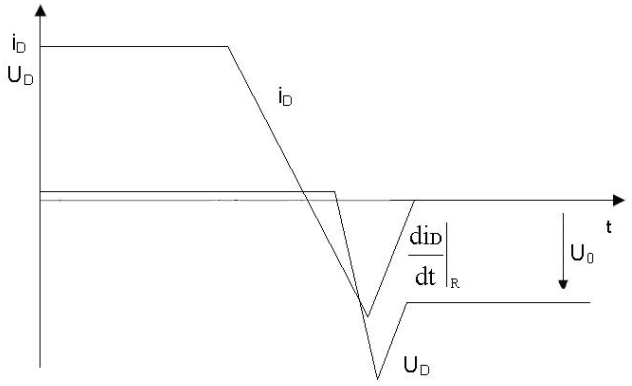

Fig. 2. Typical waveforms of the diode current i_D and the voltage drop over the diode u_D of a blocking diode, as adapted from (Baliga, 2008). The supply voltage is denoted by U_0.

The structure of the remainder of this paper is as follows: the origin of variation of the phase voltage, which is the basis for the proposed method, is discussed in the following Sect. 2, where also the measuring circuit is introduced and important results of simulations and measurements are presented. In Sect. 3 an actual implementation of the dead time optimization process is described and followed by a conclusion in Sect. 4.

2 Influence of the dead time on the switching behavior

2.1 Reverse Recovery Effect

When the MOSFET takes over the load current from the freewheeling diode of the opposite MOSFET during switch-on, the Reverse Recovery Effect occurs when this diode blocks. The following illustration shows typical current and voltage waveforms during the blocking of the freewheeling diode.

First, the MOSFET starts to take over the load current from the diode during switch-on. Eventually, the MOSFET also has to carry a reverse current of the diode because the stored charge of the diode has to be degraded before it blocks. This results in higher losses in this MOSFET (Baliga, 2008, p. 245). Once the stored charge is degraded the freewheeling diode blocks and the reverse current quickly reduces to zero. This current change induces a voltage in the parasitic inductances of the half bridge (Semikron, 1998, p. 166). If the Reverse Recovery Effect occurs at the transition low-high this voltage results in an overshoot of the phase voltage. The corresponding additional contribution U_{L_σ} to the phase voltage can be characterized by the equation

$$U_{L_\sigma} = L_\sigma \cdot \left.\frac{\mathrm{d}i_D}{\mathrm{d}t}\right|_{\mathrm{R}} \tag{1}$$

Here, the internal inductances of the MOSFETs and of the junction lines are combined in L_σ. The fast current change can also induce oscillations which have a negative impact on EMC (Rose et al., 2009; Semikron, 1998, p. 166).

2.2 Influence of reduced dead time on the Reverse Recovery Effect

The charge Q_R stored in the freewheeling diode can be reduced by decreasing the dead time because this leads to a decreased conducting time of the freewheeling diode (Polenov et al., 2009). The peak I_RM of the reverse current depends on this charge (Wang et al., 2004).

$$I_\mathrm{RM} = \sqrt{\frac{2 \cdot \mathrm{d}i_D/\mathrm{d}t \cdot Q_\mathrm{R}}{1+S}} \tag{2}$$

where S is the softness factor of the diode. With a reduced peak, the slope of the reduction of the reverse current, i.e. the term $\left.\mathrm{d}i_\mathrm{D}/\mathrm{d}t\right|_\mathrm{R}$, can be decreased as well (Baliga, 2008, p. 251). According to (1) this results in a lower voltage overshoot. It is also mentioned that the losses in the MOSFET during switch-on are reduced due to the lower reverse current and faster switching (Polenov et al., 2009).

2.3 Influence of the cross current on the phase voltage

In the same way as the decrease of the reverse current induces an overshoot of the phase voltage, the cross current can initiate an overshoot of the phase voltage, too. Particularly, the reduction of the cross current is directed in a way such that the voltage induced in the parasitic inductances adds to the phase voltage.

To investigate this behavior, a half bridge was simulated with the main parasitic inductances and resistors included. An existing power converter served as basis for the simulations and also was used for subsequent measurements described below. Figure 3 shows the simulated wave shape of the phase voltage at a dead time where a cross current occurs.

In Fig. 3, the second maximum is due to a decrease of the cross current, as has been confirmed by both simulation and measurement. The width of the peak that is associated to this second maximum depends on the magnitude of the cross current: a larger magnitude implies a larger width and vice versa. This effect can be used to detect the cross current, as described next.

2.4 Setup of the measurement circuit for detecting cross currents

The effect described in the previous paragraph also appears at the transition from the Highside- to the Lowside-MOSFET.

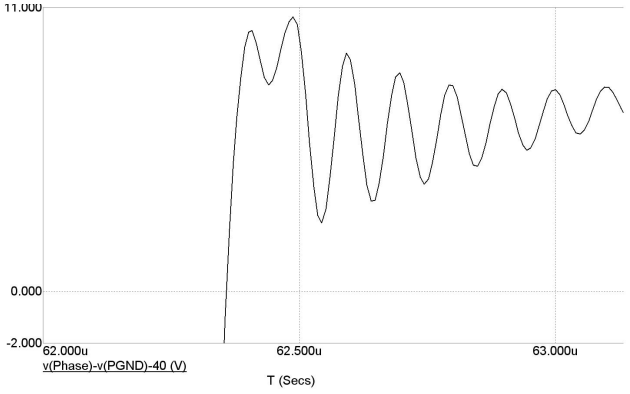

Fig. 3. Waveform of the phase voltage at a comparatively short dead time where a cross current occurs.

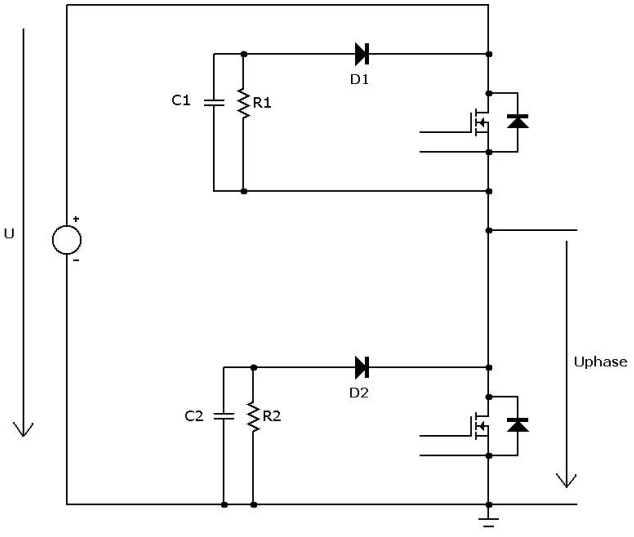

Fig. 4. Measurement circuits for detecting the over- and undershoot of the phase voltage.

The sign of the induced voltage is such that it results in an additional decrease of the phase voltage. This leads to a second undershoot. As a consequence two measurement circuits are necessary: one for detecting the overshoots of the phase voltage and one for detecting the undershoots at the other transition. In Fig. 4 a possible design of these circuits is shown.

First the circuit for detecting the voltage overshoot is described. When the phase voltage becomes larger than the supply voltage plus the forward bias of the diode D1, this diode starts to conduct and the capacitor C1 is charged. To discharge the capacitor for detecting a smaller overshoot after a larger one has occurred, the resistor R1 is connected in parallel. R1 and C1 have to be dimensioned in a way such that the first voltage overshoot is charging the capacitor only to a small fraction and, as a consequence, the second voltage overshoot still can charge the capacitor as well.

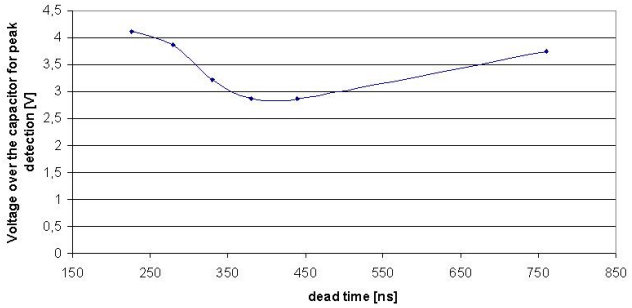

Fig. 5. Voltage across the capacitor for peak detection.

The voltage measured at the capacitor will be characterized by a charging and discharging process and thus approximately have a triangular shape. Then a possibility is to measure only the peak value of this voltage. An option to realize this is to use a capacitor with a diode put in series. This peak detecting capacitor then will be loaded until the maximum voltage will be reached. To discharge this capacitor, a MOSFET put in parallel can be used. This MOSFET can be controlled by the microprocessor that realizes the dead time optimization.

It must be noted that the reference potential of the voltage across the capacitor C1 is given by the phase voltage while the microprocessor who measures this voltage has in most cases a ground reference potential. However, for converting the voltage across the capacitor C1, special ICs can be used, which are e.g. designed for current measurement with a resistor. The peak detection circuit can be set at the output of this IC such that the microprocessor can directly control the discharging MOSFET and measure the voltage over the peak detecting capacitor.

The circuit for detecting undervoltage behaves in the same way. In this case the measurement capacitor is charged when the voltage is below the ground potential plus the forward bias voltage of the diode D2. Here the usage of a peak detection circuit in combination with a voltage transferring IC is also reasonable.

2.5 Influence of the dead time on the measured signal

To investigate the behavior of the measurement circuit of Fig. 4 it is integrated in the half bridge of an actual power converter, which can switch currents up to 400 A. With a successively reduced dead time, the ground referenced voltage across the capacitor for peak detection, as described in the previous section, is measured.

Starting from a large dead time of 750 ns, the absolute value of this voltage decreases because of the reduced Reverse Recovery Effect of the freewheeling diode which leads, according to Eq. (1), to a decreased overvoltage. It is then observed that at a dead time of approximately 350 ns the voltage starts to increase. At this dead time a beginning cross current

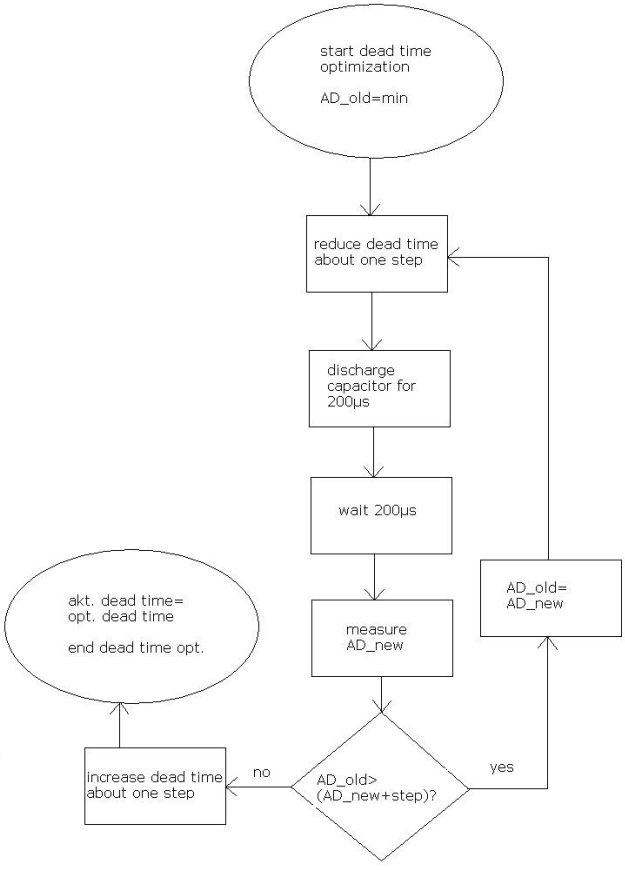

Fig. 6. Principle of the dead time optimization process. The variable AD corresponds to the measured peak voltage.

was detected in several measurements and simulations. Also, beginning from this dead time, increasing losses were measured due to the developing cross current.

At dead times around 350 ns the amplitude of the first overvoltage is strongly reduced in comparison to the larger dead time of 750 ns. But as the simulation result of Fig. 3 shows, the second overshoot becomes larger with increasing cross current. This change of wave shape can also be measured at the half bridge with decreasing dead time. Due to this wider second overshoot the measurement capacitor is stronger charged, which results in the increasing voltage drop. This rise can be detected by a dead time optimization method which is described in the following section.

3 Dead time optimization method

3.1 Process of the dead time optimization method

In general the dead time optimization process only has to be started once at the beginning of the drive. But in some cases it might be useful to repeat this process, e.g. due to an increased

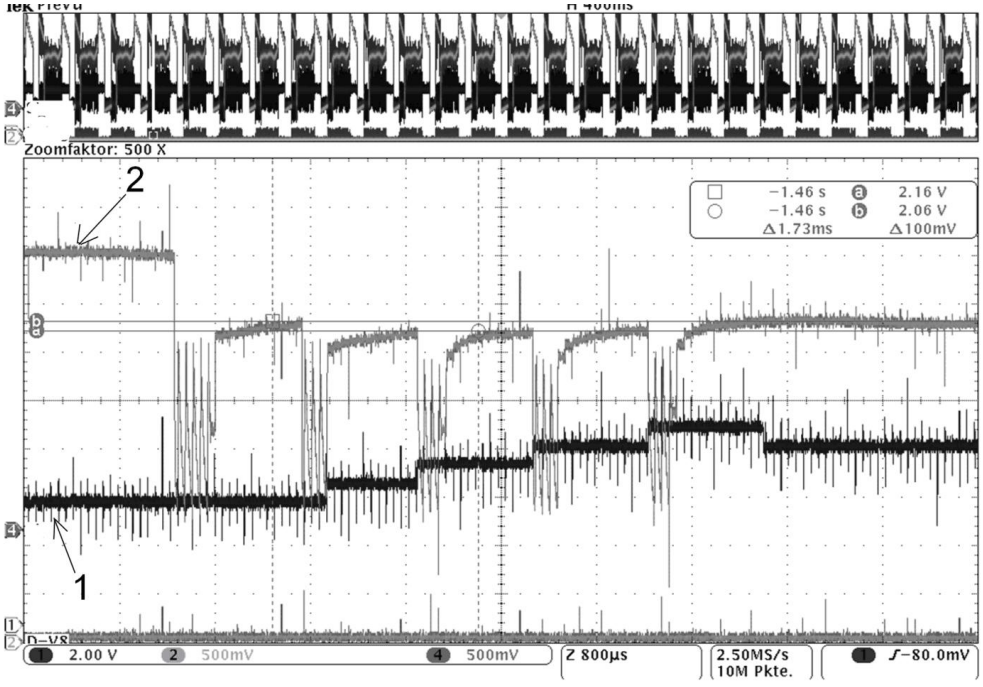

Fig. 7. Dead time optimization process. Curve 1: output of the DA-converter, proportional to dead time: an increase of the DA output voltage corresponds to a decrease of the dead time. Curve 2: measured voltage over the peak detection capacitor C3.

temperature of the converter. This has to be analyzed for a given power converter system.

The PWM-controlling microprocessor has to measure the voltage over the peak detecting capacitors. These signals can directly be transmitted to the AD-converter. It is necessary that the microprocessor can influence the dead time, which is often the case. The dead time is now gradually decreased and after every step the actual voltage over a peak detecting capacitor has to be measured. As an initial condition of this process it is necessary that the capacitor is discharged via the MOSFET which is also controlled by this microprocessor. The discharge has to last until the capacitor C1 or C2 has adapted the new value, which usually takes about 200 µs to 400 µs. After this period, the peak detecting capacitor has to attain the peak voltage. This time depends on the IC used for the voltage transfer. For the cases considered, this time turned out to be about 200 µs.

In the actual process, first the measured peak voltage will decrease as it can be seen in Fig. 5. When the dead time approaches the range where a cross current occurs an increase will be detectable. Figure 6 exemplifies this process.

This process has been integrated in the control of an actual half bridge. For exemplification a voltage was generated via a DA-converter which was chosen to be proportional to the dead time. In Fig. 7 a screenshot of the measured voltages illustrates this process.

First a reduction of the dead time leads to a decrease of the measured voltage. After every dead time reduction, which here is about 50 ns, the peak detection capacitor is discharged until the measurement capacitor C1 has reached the new value. After the fourth step it is seen that the measured voltage starts to increase. This is detected by the controller which then stops the dead time reduction. Since after the fourth step a small cross current exists, the controller increases the dead time about one step. As a result an optimal dead time is found to be about 380 ns.

3.2 Setting of the optimal dead time

Basically four switching transitions have to be distinguished, which are illustrated in Fig. 8.

When the load current is directed out of the half-bridge the Reverse Recovery Effect can be monitored at the transition low-high and in case that the load current runs in the half-bridge the Reverse Recovery Effect can be monitored at the transition high-low. For these two transitions a dead time optimization is useful, as described above, to reduce losses and to improve EMC. The dead time at the other transitions can be chosen relatively high such that no cross current occurs. But it has to be mentioned that the described effect of second overshoot also appears at these transitions. Here it can also be useful to find the optimal, lowest dead time to increase the dynamic range of modulation.

To summarize, four different dead times have been determined. These are, depending on the direction of the load current, two dead times for each switching transition. Therefore the dead times have to be adjusted at each switching tran-

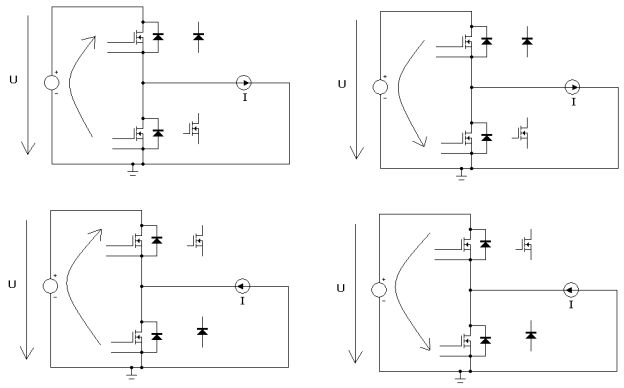

Fig. 8. Switching transitions in a half-bridge, indicated by curved arrows, as adapted from Huselstein et al. (1993).

sition in the zero-crossing of the load current. In many applications the controlling microprocessor measures or calculates the actual current direction, such that this adjustment can easily be achieved.

4 Conclusions

The presented dead time optimization method provides a new alternative to existing approaches. In contrast to the majority of these methods this approach does not need additional components in the main current tracks of the half bridge, which would produce additional losses. A suitable measurement circuit has been proposed to detect the changes in the wave shape of the phase voltage when a cross current occurs. This measured value is the basic variable of the dead time optimization process. The proposed method also has been successfully tested in an actual half-bridge.

With this dead time reduction both the overshoot of the phase voltage and the switching losses are reduced. Also a considerable improvement in the EMC of the power converter has been observed.

So far this method has only been tested with MOSFETs but it should also be applicable to transistors such as IGBTs. Also the application in other contexts, such as the optimization of DC/DC-converters, is conceivable.

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