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A 10-b 5-GS/s Passive T/H Assisted Time-Interleaved Pipelined-SAR ADC With Pre-Quantization and Background Offset Calibration

Qiang Yu[1,2] | Qiang Li[1,3]

[1]Institute of Integrated Circuits and Systems, University of Electronic Science and Technology of China, Chengdu, China | [2]Chengdu MECS Microelectronics Technology, Chengdu, China | [3]Hamburg University of Technology, Hamburg, Germany

Correspondence: Qiang Li (qli@uestc.edu.cn)

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ABSTRACT

This letter presents a 10-bit 5-GS/s time-interleaved (TI) pipelined successive-approximation-register (SAR) analogue-to-digital converter (ADC). By utilizing a full-speed passive track-and-hold circuit (T/H), pre-quantization can be performed in parallel, alleviating the timing constraint in the first stage. The chopped switches in the passive T/H enable input-independent background offset calibration for comparators and residue amplifiers. Fabricated in a 28-nm CMOS process, the prototype ADC achieves 51.8-dB SNDR and 67.9-dB SFDR at the Nyquist input.

1 | Introduction

The nontrivial skew calibration can be avoided with an energy-efficient passive track-and-hold circuit (T/H) [1]. However, the sampling rate is limited by the relatively slow two-stage pipelined successive-approximation-register (SAR) analogue-to-digital converter (ADC), particularly due to the tight timing of the first stage. Although speed enhancement techniques such as 2b/cycle [2] and loop-unrolled [3] can ease the constraint, they incur significant area and calibration overhead due to the use of multiple comparators. The parallel-operation techniques [4, 5] allow quantization to be performed during residue amplification, thereby easing the timing pressure on the subsequent stages. However, they do not resolve the speed bottleneck in the first stage. For reliable operation in an advanced process, background offset calibration (BOC) for both comparators and residue amplifiers (RAs) becomes essential. Several calibration schemes have been proposed for pipelined-SAR ADCs, each with its own limitations. One approach inserts dedicated cycles for comparator self-calibration [3], but this reduces conversion speed. Another method decouples the comparator from the main signal path, enabling parallel self-calibration during the amplification phase [6]. However, this approach requires additional handling of gain, offset, and timing mismatches between the two paths. Moreover, neither of the above methods can correct the offset introduced by the RAs. To address these issues, pre-quantization and BOC are proposed based on the chopped passive T/H. The first bit is pre-quantized during the passive transfer, enhancing conversion speed. The chopped switches modulate all types of input signals to zero-mean signals, thereby facilitating input-independent BOC. With these techniques, the 5-GS/s 10-bit TI ADC achieves robust operation without the need for skew calibration.

2 | TI Pipelined-SAR ADC Architecture

Figure 1 shows the architecture of the proposed TI pipelined-SAR ADC. The passive T/H operates at the full sampling rate to realize skew calibration free. With the elimination of bandwidth mismatch error, the inter-channel gain mismatch becomes independent of both sampling bandwidth and input frequency, as it is determined by charge redistribution during passive transfer. Consequently, the gain mismatch is insensitive to voltage and temperature (VT) variations. Moreover, the chopping

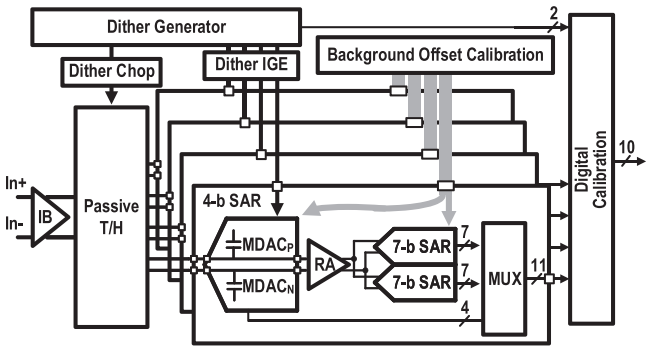

FIGURE 1 | Top-level 10-b 5-GS/s TI Pipelined-SAR ADC architecture.

technique enables signal-independent calibration of the VT-sensitive offset of both the comparators and the RA after the chopping switches. The residual offset originates from the chopping switches themselves, significantly reducing VT sensitivity [1]. Four single-channel two-stage pipelined-SAR ADCs, each operating at 1.25 GS/s, are interleaved to realize a total sampling rate of 5 GS/s. The first stage resolves 4 bits with pre-quantization to ensure a relaxed timing budget. The second stage is a 7-bit SAR ADC, with the first bit serving as inter-stage redundancy to tolerate mismatches. To further ease timing constraints in the second stage, partial interleaving reduces conversion speed to 625 MS/s. Two types of dither are generated for chopped switches and inter-stage-gain error (IGE) calibration. On-chip background calibration addresses comparator and RA offset, chopped offset, IGE, as well as TI gain and offset mismatches. The coefficients for TI gain and offset mismatch calibration are extracted in the foreground.

The full-scale input swing of ADC is 0.8 V_{PP}. The passive transfer reduces the swing by half. After 4-bit quantization, the ideal residual voltage swing of the first stage is 25 mV_{PP}. Since the inter-stage redundancy is defined to have the same weight as the first-stage LSB, the total redundancy range in our design is 25 mV_{PP}. The dither injected for IGE calibration occupies approximately 12.5 mV_{PP} of this range. Thanks to the BOC scheme, the total offset from the comparators and the RA consumes less than 8 mV_{PP} of the redundancy. The voltage settling before pre-quantization is very fast. Therefore, the settling error introduced is extremely small (well below 1 mV_{PP}). As a result, the redundancy is adequate to ensure proper operation.

3 | Pre-Quantization

Based on the redundancy analysis and the linearity requirement of the open-loop RA, the first stage must resolve 4 bits to ensure the residual voltage is below 50 mV_{PP}. This leads to a tight timing constraint in the first stage of a conventional pipelined-SAR ADC. The period of the first-stage ADC is 800 ps. The timing budget allocates approximately 100 ps for passive transfer, 150 ps for amplification and 50 ps for DAC reset. The remaining time for four comparison cycles is 500 ps, which is insufficient to guarantee reliable operation under VT variations and a weak SS corner. Fortunately, the passive T/H enables pre-quantization to accelerate the conversion. The schematic of the passive T/H and

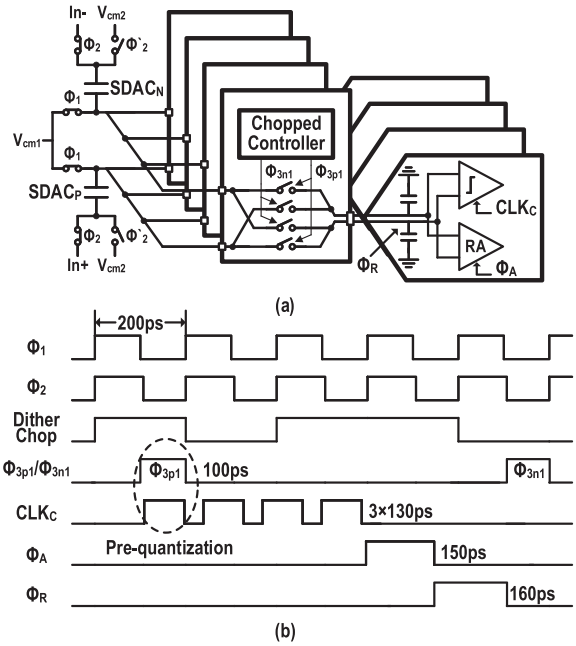

FIGURE 2 | (a) Schematic of the passive T/H and the first stage ADC. (b) Timing diagram of passive transfer and pre-quantization.

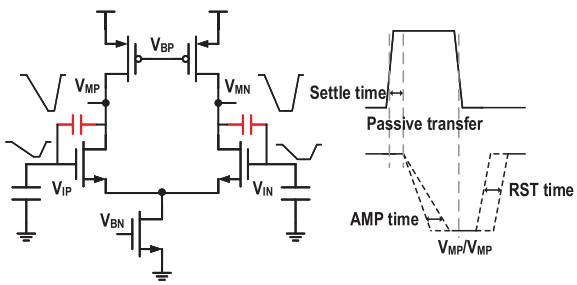

FIGURE 3 | Comparator coupling during pre-quantization.

the first-stage ADC with pre-quantization is shown in Figure 2a. The passive T/H employs bottom-plate sampling for high linearity. The input signal is then passively transferred to the DAC of the sub-ADC. Since the passive transfer is fundamentally a DC voltage transfer, pre-quantization can operate in parallel during this transfer. According to the improved timing budget shown in Figure 2b, each of the last three comparisons is allocated 130 ps. The remaining time budget for DAC resetting is 160 ps under a typical condition (1 V power supply, 55°C junction temperature, and TT corner), while the allocated budget is 80 ps under a bad case corner (0.95 V power supply, 125°C junction temperature, and weak SS corner). The 55 °C typical junction temperature is derived from 25°C ambient temperature plus a measured 30°C self-heating (via on-chip diode), while the 125°C bad case junction temperature is determined by the process technology's maximum operating limit. It should be noted that the positive switches are controlled by ϕ_{3px} when the dither chop is '1', while the negative switches are controlled by ϕ_{3nx} when the dither chop is '0'.

As shown in Figure 3, the preamplifier outputs (V_{MP}/V_{MN}) in the comparator swing from supply to ground during pre-quantization. This voltage swing couples into the DAC through the parasitic MOS capacitances of the input pair, resulting in

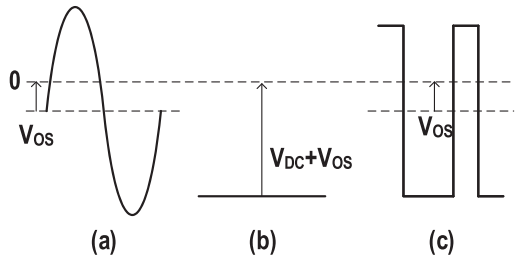

FIGURE 4 | The statistical properties of (a) zero-mean signal, (b) DC signal, and (c) chopped DC signal.

performance degradation. If V_{MP}/V_{MN} are reset to VDD, pre-quantization proceeds identically to a normal quantization. However, pre-quantization must wait for the DAC to settle to the correct initial voltage. The duration of the amplification (AMP) and reset (RST) phases depends on the input voltage level. Consequently, the total pre-quantization time becomes significantly longer than transfer time. To minimize this timing overhead and the decoupling effect, the optimal timing for the falling edge of the transfer control signal is when both V_{MP}/V_{MN} have stabilized at their low levels. Moreover, the coupling capacitors are nonlinear MOS devices, which inject signal-dependent charge into the DAC and degrade linearity. Therefore, the size of the first-stage comparator should be kept small.

4 | Background Offset Calibration

Due to the small transistor sizes and the use of core devices in a 28-nm process, the offset voltages of the comparators and RAs are sensitive to PVT variations and also drift over time due to device aging [7]. Therefore, BOC is necessary. Leveraging statistical properties can extract the offset. As shown in Figure 4a, when the analogue input signal is zero-mean, the average of the output codes can reflect the comparator's offset voltage, enabling adjustments based on this value. However, this method fails under certain conditions. When the ADC input is a DC signal, or in a TI ADC when the input signal is at a frequency equal to nF_S/N (where n is a positive integer, F_S is the sampling rate and N is the number of channels), each sub-channel samples a DC signal. As shown in Figure 4b, the average of the output codes deviates significantly from the comparator's actual offset voltage. This causes the residue voltage generated by the first stage to exceed the quantization range of subsequent stages, leading to conversion errors.

To resolve these limitations, this design employs BOC based on a chopping technique. As shown in Figure 4c, after chopping, the average value of a DC input can still reflect the comparator's offset. Furthermore, the residue voltage of the first stage also becomes a zero-mean signal. Building on this, the average value of the second-stage quantization results can be extracted to reflect the combined offset of the RA and the second-stage comparators. The average value is computed over 2^{16} consecutive samples. The control word of the analogue offset correction circuit is incremented or decremented according to the sign of the average value. To avoid performance degradation due to offset variations, correction is enabled only when the absolute value of the average exceeds a detection threshold. Based on measurements, the

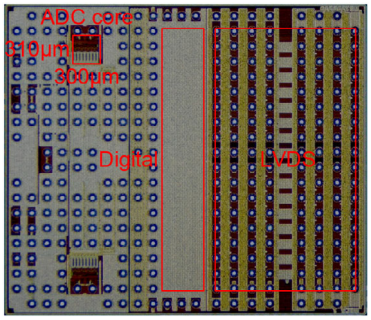

FIGURE 5 | Die micrograph.

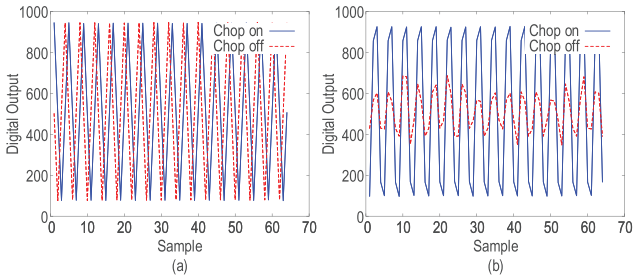

FIGURE 6 | Measured waveform at: (a) 1249.5 MHz and (b) 1250 MHz input.

threshold is set to 4 LSB for the first stage and 4 LSB for the second stage. For the implementation of offset correction, the offset of the first-stage comparators is adjusted by adding an extra calibration input pair. The offset of the RAs and the second-stage comparators is compensated by injecting a cancellation voltage into the DAC of the second stage after the amplification phase [8].

5 | Measurement Result

Figure 5 shows the die micrograph. The prototype 10-bit 5-GS/s ADC is fabricated in a 28-nm CMOS process, with the analogue core occupying 0.093 mm^2. Digital calibration is integrated on-chip. LVDS interfaces are used for data output. The ADC core, including the passive T/H network, dither generator, and sub-ADCs, consumes 57.4 mW from a 1 V supply, while the input buffer draws 22.8 mW from a 1.9 V supply. Digital calibration circuit consumes 107.2 mW from a 0.9 V supply. As shown in Figure 6a, the ADC performs correctly at a 1249.5 MHz input frequency regardless of whether chopping is enabled. However, at a 1250 MHz input, the ADC fails when chopping is turned off due to the breakdown of BOC, whereas it continues to operate correctly with chopping on as shown in Figure 6b. Figure 7 shows the measured output spectra at 5 GS/s for input frequencies of 347 MHz and near Nyquist, respectively. The measured SNDR and SFDR are 52.8 and 72.8 dB with a 347 MHz input. The SNDR and SFDR are 51.8 dB and 67.9 dB with a 2382 MHz input. The ADC achieves a Nyquist FoM_W of 118.0 fJ/conversion-step and a Nyquist FoM_S of 153.1 dB. Out of 60 tested ADCs, 57 ADCs demonstrate 5 GS/s capability under a 0.95 V supply and 105°C ambient temperature, leading to a high yield of 95%.

Table 1 compares this work with state-of-the-art ADCs of similar performance. Benefiting from the high-speed pipelined-

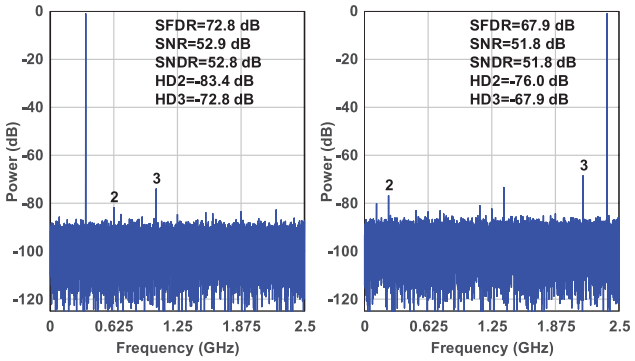

FIGURE 7 | The output spectra with 347 MHz and Nyquist input signals at 5 GS/s.

TABLE 1 | Performance summary and comparison with the state-of-the-art ADCs.

Parameter	This work	JSSC 2020 [9]	VLSI 2018 [10]	VLSI 2019 [11]	TCAS I 2017 [12]
Architecture	TI pipe-SAR			TI SAR	
Process [nm]	28	28	16	28	28
FS [GS/s]	5	5	5	5	5
Resolution [bits]	10	12	13	10	10
$SFDR_{Nyq}$ [dB]	67.9	65.4	61.9	59.6	54.4
$SNDR_{Nyq}$ [dB]	51.8	58.5	57	48.5	41.7
Power [mW]	187.4[a]	158.6[a]	641[a]	29.0	76
$FoM_{W,Nyq}$ [fJ/c.-s.]	118.0	46.1	221.6	26.7	165
$FoM_{S,Nyq}$ [dB]	153.1	160.5	152.9	157.9	147.2
Analogue area [mm^2]	0.093	0.63[b]	0.76[b]	0.103	0.57
Skew-free?	Y	N	N	N	N
BOC?	Y	N	N	No need	No need

[a]Include digital calibration.
[b]Estimated from die micrograph.

SAR architecture, this design achieves 5 GS/s with a small number of interleaved channels, resulting in a compact analogue area. It is the only design featuring both skew-free and BOC, ensuring robust performance regardless of input signal characteristics.

6 | Conclusion

The passive T/H assisted TI pipelined-SAR ADC offers advantages not only in power efficiency and area, but also in several other aspects provided by the chopped passive T/H. First, it inherently achieves skew-free and supports foreground-calibratable interleaving mismatch calibration for both gain and offset. Second, its DC-transfer characteristic allows pre-quantization to improve timing margin. Third, chopping converts arbitrary input signals into zero-mean sequences, allowing BOC via code averaging. The proposed ADC reliably operates at 5 GS/s, and all implemented calibrations are signal-independent.

Author Contributions

Qiang Yu: modeling, design, simulation, data curation, formal analysis, investigation, validation, visualisation, writing – original draft and revised draft. **Qiang Li:** initial discussion, formal analysis, methodology, writing – review and editing.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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